

Single 8-Ch/Differential 4-Ch CMOS Analog Multiplexers

Features

- Low On-Resistance: 240 Ω
- TTL and CMOS Logic Compatible
- Low Power: 30 mW
- Break-Before-Make Switching
- 44-V Power Supply Rating
- Transition Time: 600 ns

Benefits

- Easily Interfaced
- Low Power Consumption
- Low System Crosstalk
- Wide Analog Signal Range

Applications

- Communication Systems
- ATE
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing
- Medical Instrumentation

Description

The DG508A, an 8-channel single-ended analog multiplexer, is designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2).

The DG509A, a dual 4-channel analog multiplexer, is designed to connect one of four differential inputs to a common output as determined by its 2-bit binary address (A_0, A_1) logic. Break-before-make switching action protects against momentary shorting of the input signals.

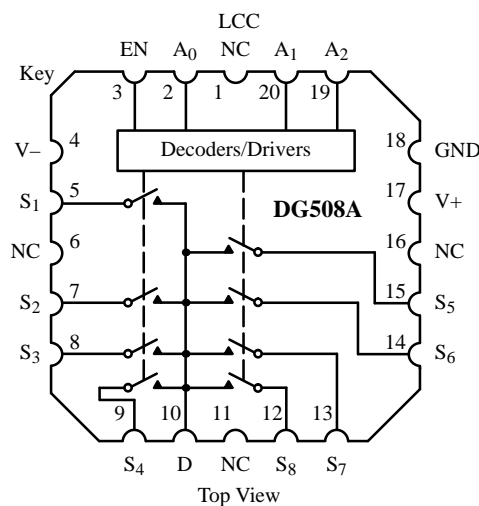
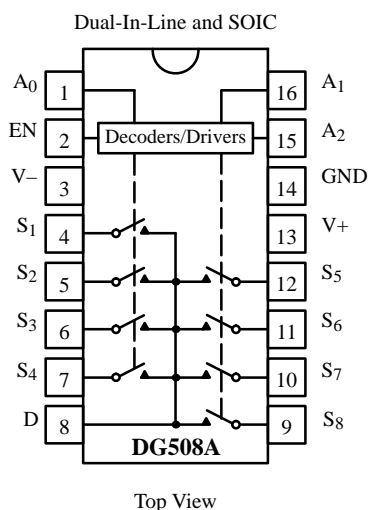
A channel in the on state conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows for device selection when several multiplexers are used. All control

inputs, address (A_X) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

Fabricated in the Siliconix Plus-40 process, the absolute maximum voltage rating is extended to 44 V, allowing increased operating headroom for standard ± 15 -V signal swings and operation with ± 20 -V supplies. An epitaxial layer prevents latch up.

For applications requiring address data latching, the DG528/529 is recommended. DG408/409 is recommended for higher precision applications. For wideband/video routing and multiplexing, the DG538A is recommended.

Functional Block Diagrams and Pin Configurations



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70067.

Functional Block Diagrams and Pin Configurations (Cont'd)

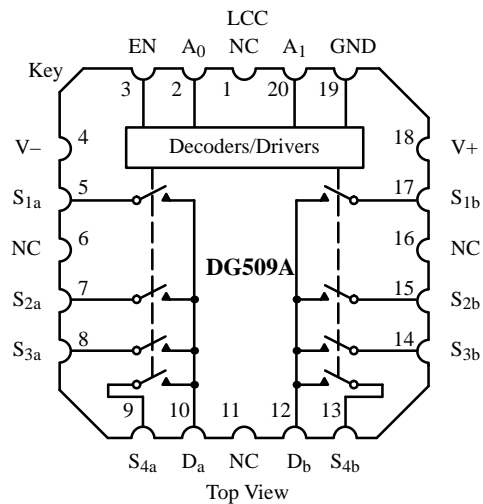
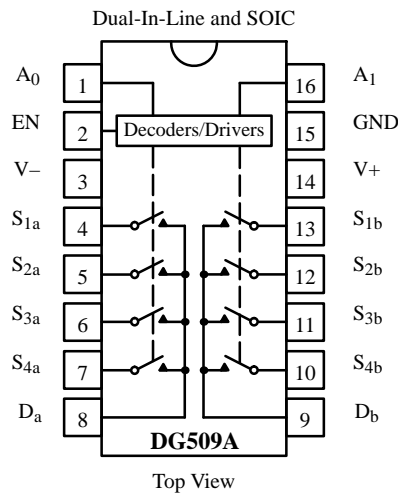
Ordering Information – DG508A

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG508ACJ
-25 to 85°C	16-Pin CerDIP	DG508ABK
-40 to 85°C	16-Pin Narrow SOIC	DG508ADY
-55 to 125°C	16-Pin CerDIP	DG508AAK
		DG508AAK/883
	LCC-20	DG508AAZ/883
	16-Pin Sidebrazed	7705201EA
		7705201EC
	16-Pin Flat Pack	7705201FA
		7705201FC
	16-Pin Sidebrazed	JM38510/19007BEA
JM38510/19007BEC		

Truth Table — DG508A

A ₂	A ₁	A ₀	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = V_{AL} ≤ 0.8 V
 Logic "1" = V_{AH} ≥ 2.4 V
 X = Don't Care



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-40 to 85°C	16-Pin Narrow SOIC	DG509ADY
-55 to 125°C	16-Pin CerDIP	DG509AAK
		DG509AAK/883
	LCC-20	DG509AAZ/883
	16-Pin Sidebrazed	JM38510/19008BEA
		JM38510/19008BEC

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Logic "0" = V_{AL} ≤ 0.8 V
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 X = Don't Care

Absolute Maximum Ratings

Voltage Referenced to V-	
V+	44 V
GND	25 V
Digital Inputs ^a , V _S , V _D	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal, Except S or D)	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA
Storage Temperature (K Suffix)	-65 to 150°C
(J and Y Suffix)	-65 to 125°C

Power Dissipation (Package) ^b	
16-Pin Plastic DIP ^c	470 mW
16-Pin Narrow SOIC ^c	600 mW
16-Pin CerDIP ^d	900 mW
LCC-20 ^d	900 mW

Notes:

- Signals on S_X, D_X or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 6.3 mW/°C above 75°C.
- Derate 12 mW/°C above 75°C.

Specifications^a

Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, V ₋ = -15 V V _{IN} = 2.4 V, 0.8 V ^f		Temp ^b	Typ ^c	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
						Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}			Full		-15	15	-15	15	V
Drain-Source On-Resistance	r _{DS(on)}	V _D = ±10 V, I _S = -200 μA		Room Full	240		400 500		450 550	Ω
r _{DS(on)} Match	Δr _{DS(on)}	-10 V < V _S < 10 V		Room	6					%
Source Off Leakage Current	I _{S(off)}	V _{EN} = 0 V, V _S = ±10 V V _D = ∓10 V		Room Full		-1 -50	1 50	-5 -50	5 50	nA
Drain Off Leakage Current	I _{D(off)}	V _{EN} = 0 V V _D = ±10 V V _S = ∓10 V	DG508A	Room Full		-10 -200	10 200	-20 -200	20 200	
			DG509A	Room Full		-10 -100	10 100	-20 -100	20 100	
Drain On Leakage Current	I _{D(on)}	V _S = V _D = ±10 V	DG508A	Room Full		-10 -200	10 200	-20 -200	20 200	
			DG509A	Room Full		-10 -100	10 100	-20 -100	20 100	
Digital Control										
Logic Input Current Input Voltage High	I _{AH}	V _A = 2.4 V		Room Full	-0.002	-10 -30		-10 -30		μA
		V _A = 15 V		Room Full	0.006		10 30		10 30	
Logic Input Current Input Voltage Low	I _{AL}	V _{EN} = 0 V, 2.4 V, V _A = 0 V		Room Full	-0.002	-10 -30		-10 -30		
Dynamic Characteristics										
Transition Time	t _{TRANS}	See Figure 2		Room	0.6		1			μs
Break-Before-Make Time	t _{OPEN}	See Figure 4		Room	0.2					
Enable Turn-On Time	t _{ON(EN)}	See Figure 3		Room	1		1.5			
Enable Turn-Off Time	t _{OFF(EN)}			Room	0.4		1.0			
Charge Injection	Q	See Figure 5		Room	6					pC
Off Isolation	OIRR	V _{EN} = 0 V, R _L = 1 kΩ, C _L = 15 pF V _S = 7 V _{RMS} , f = 500 kHz		Room	68					dB
Logic Input Capacitance	C _{in}	f = 1 MHz		Room	8					pF
Source Off Capacitance	C _{S(off)}	V _{EN} = 0 V, V _S = 0 V, f = 140 kHz		Room	6					
Drain Off Capacitance	C _{D(off)}	V _{EN} = 0 V, V _D = 0 V f = 140 kHz	DG508A	Room	25					
			DG509A	Room	12					

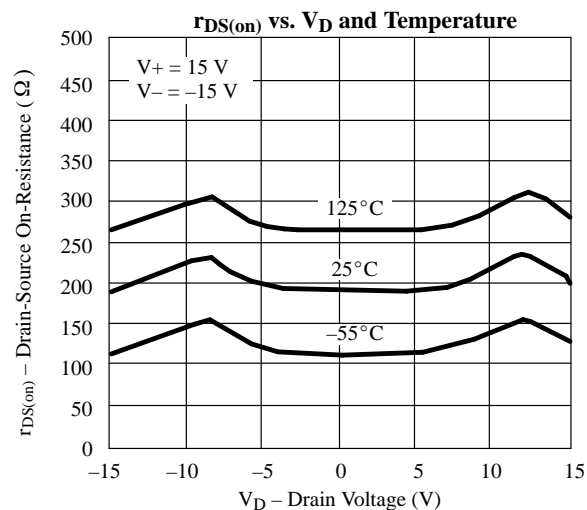
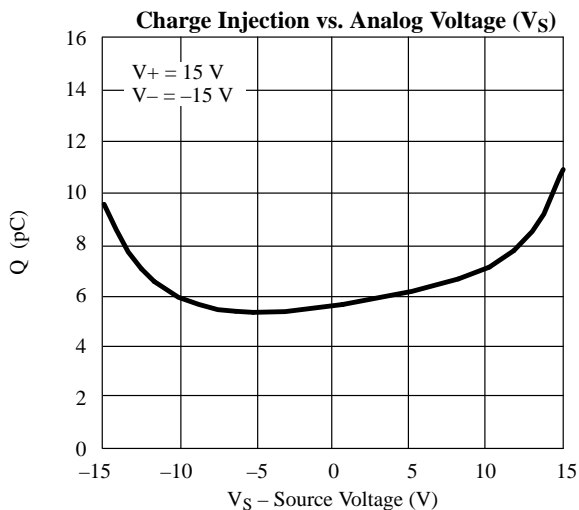
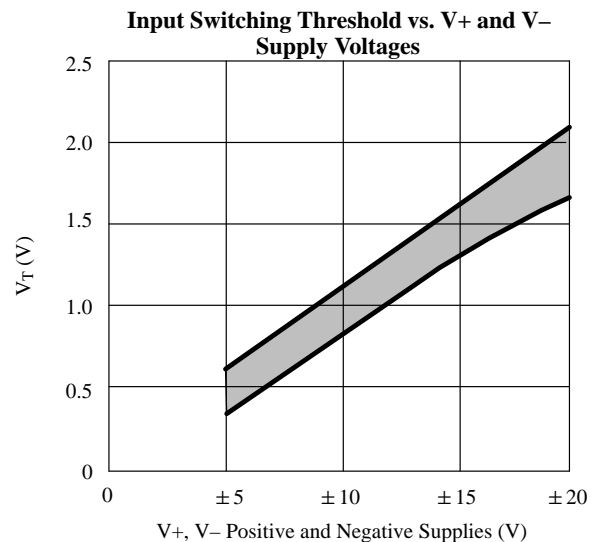
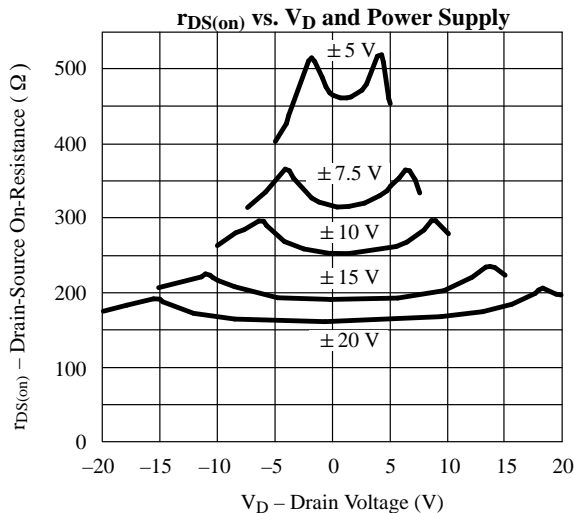
Specifications^a (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}$, 0.8 V^f	Temp ^b	Typ ^c	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Power Supplies									
Positive Supply Current	I+	$V_{EN} = 0\text{ V}$ or 2.4 V	Room	1.3		2.4		2.4	mA
Negative Supply Current	I-		Room	-0.7	-1.5		-1.5		

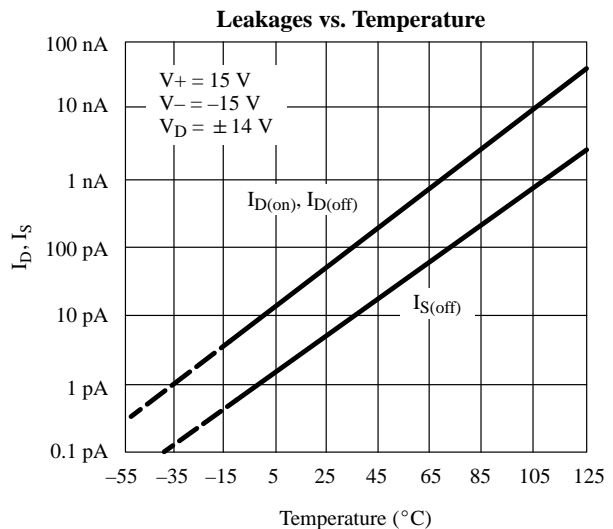
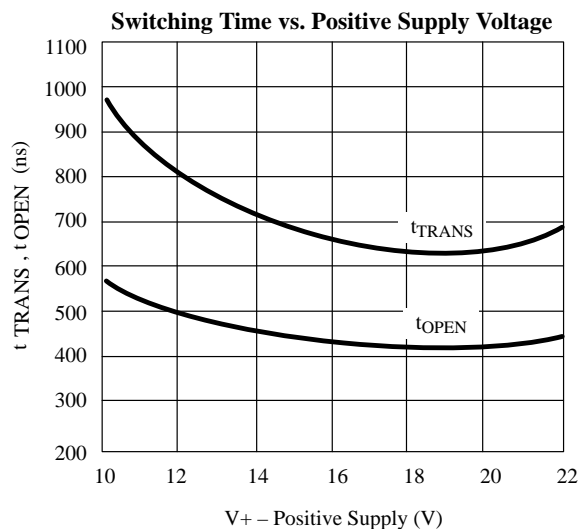
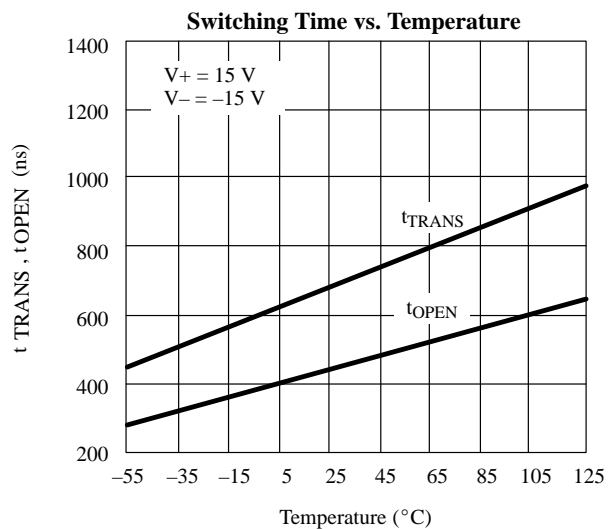
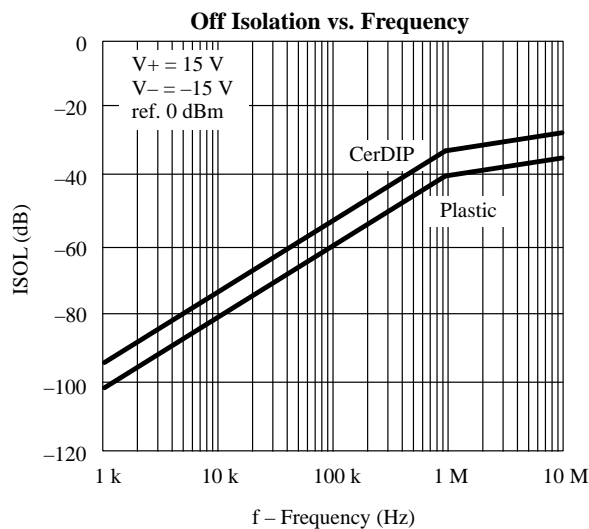
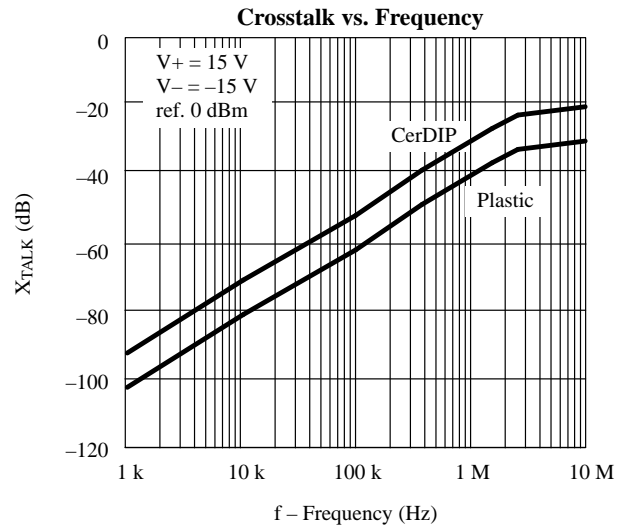
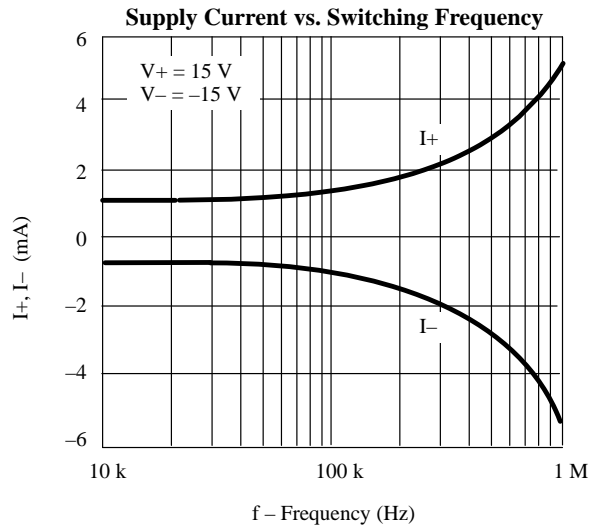
Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

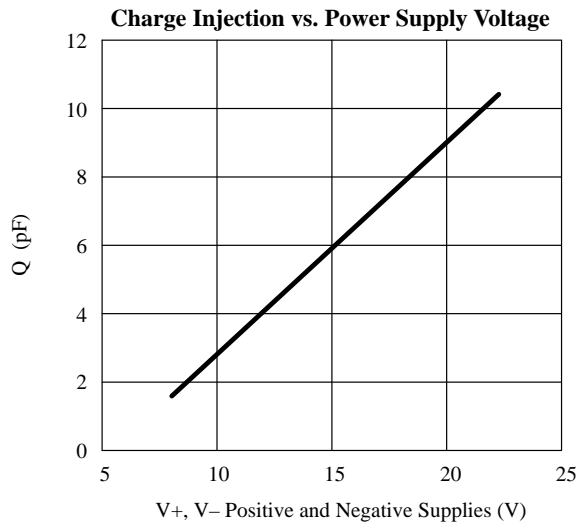
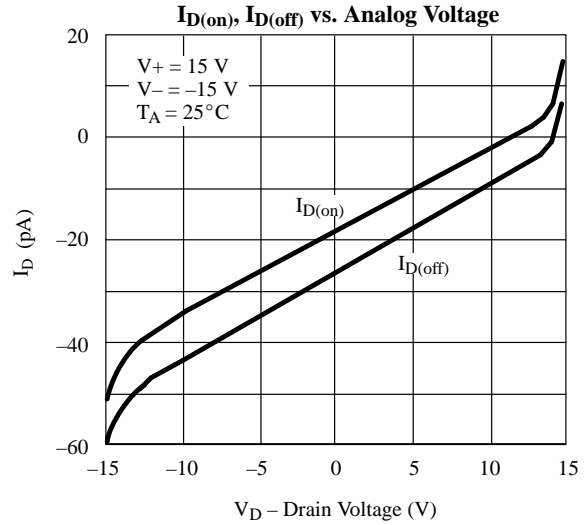
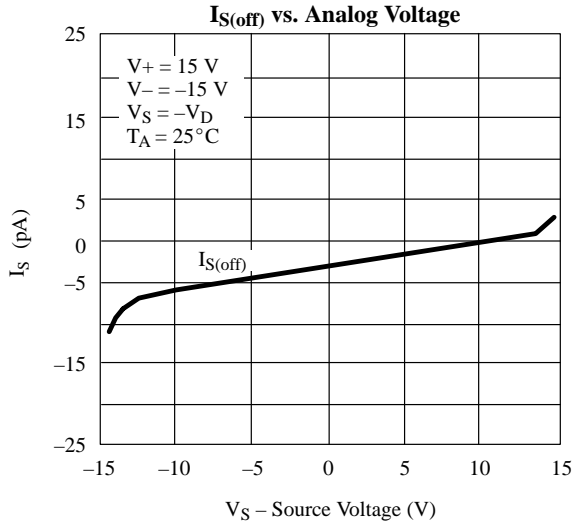
Typical Characteristics



Typical Characteristics (Cont'd)



Typical Characteristics (Cont'd)



Schematic Diagram (Typical Channel)

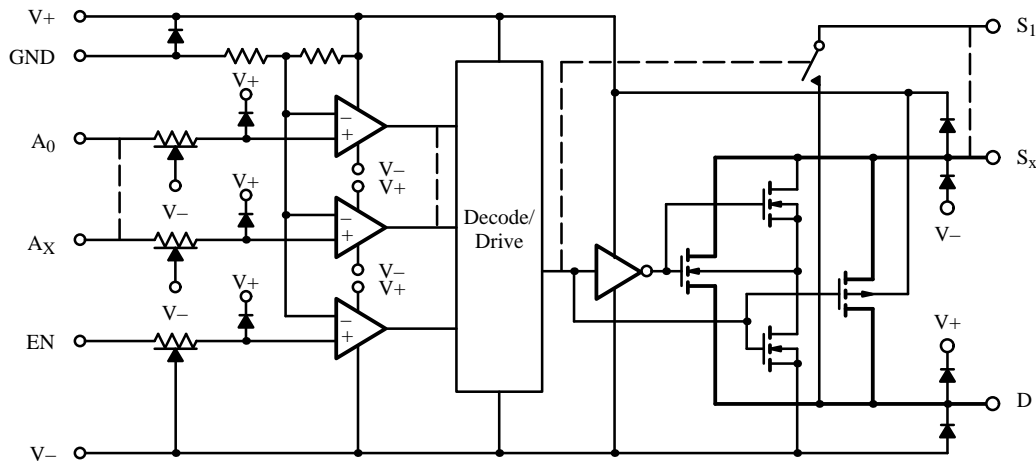


Figure 1.

Test Circuits

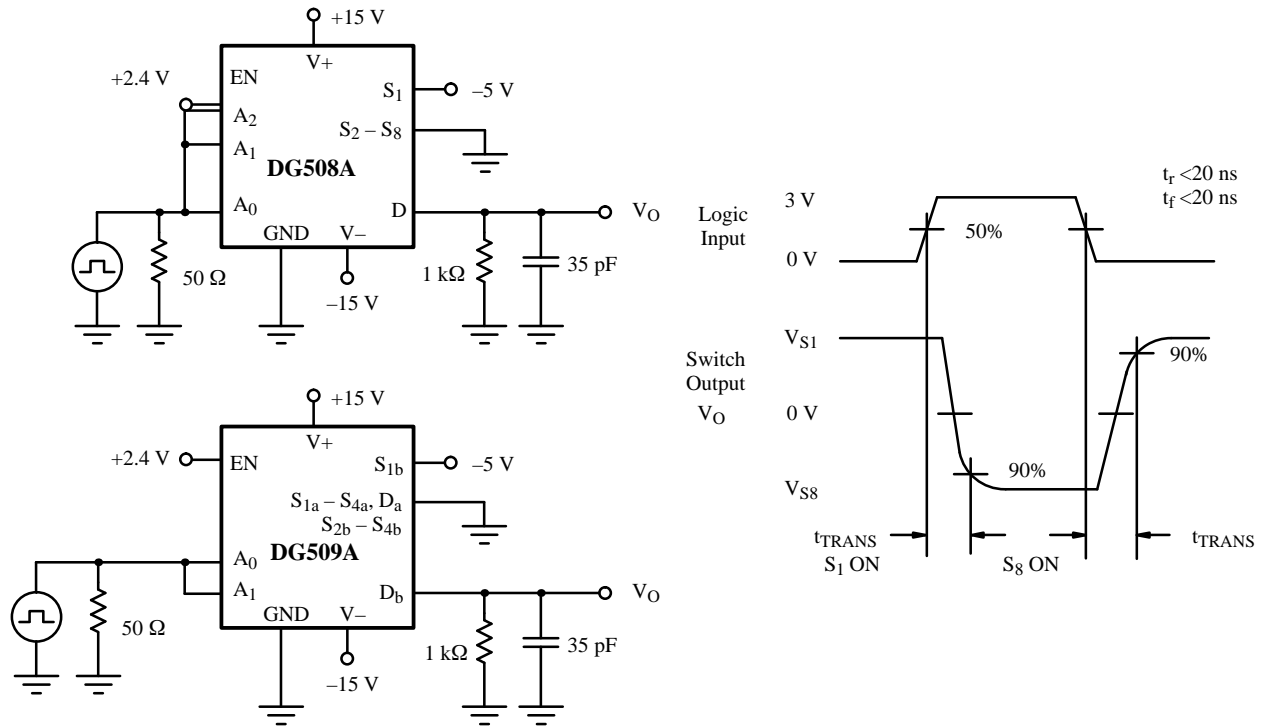


Figure 2. Transition Time

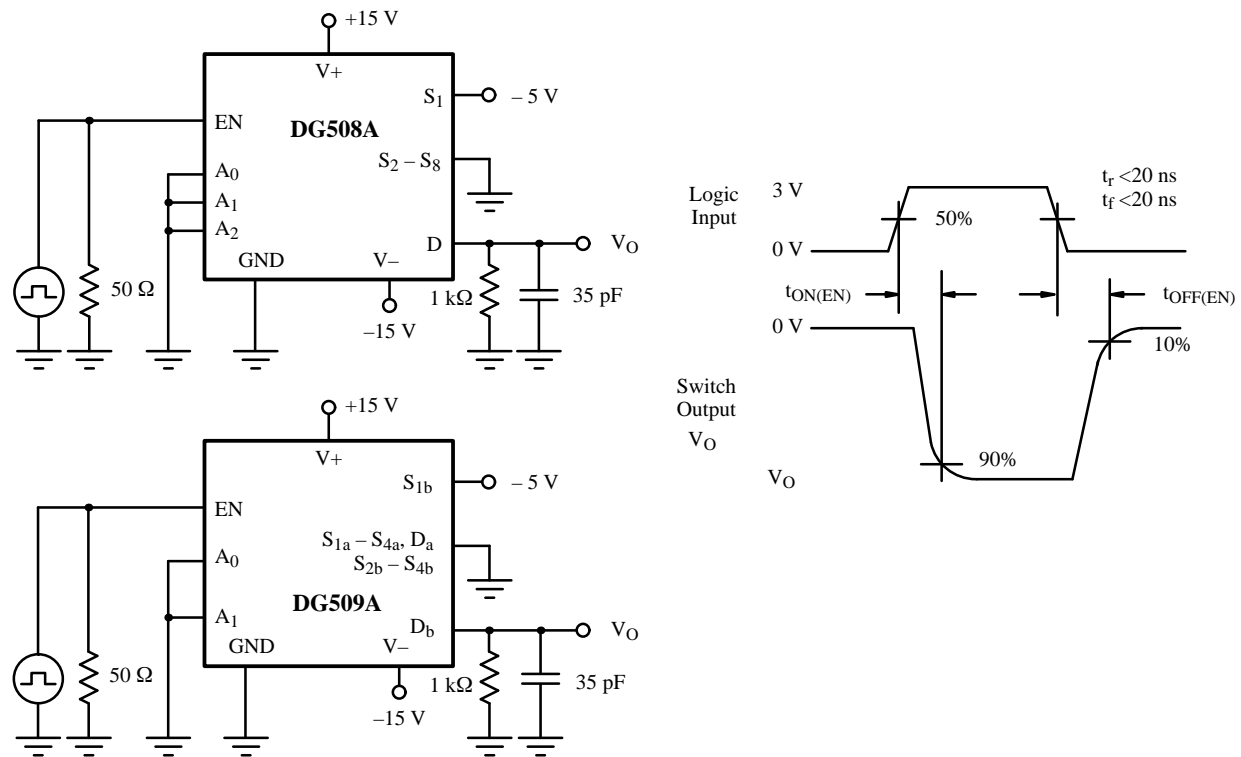


Figure 3. Enable Switching Time

Test Circuits (Cont'd)

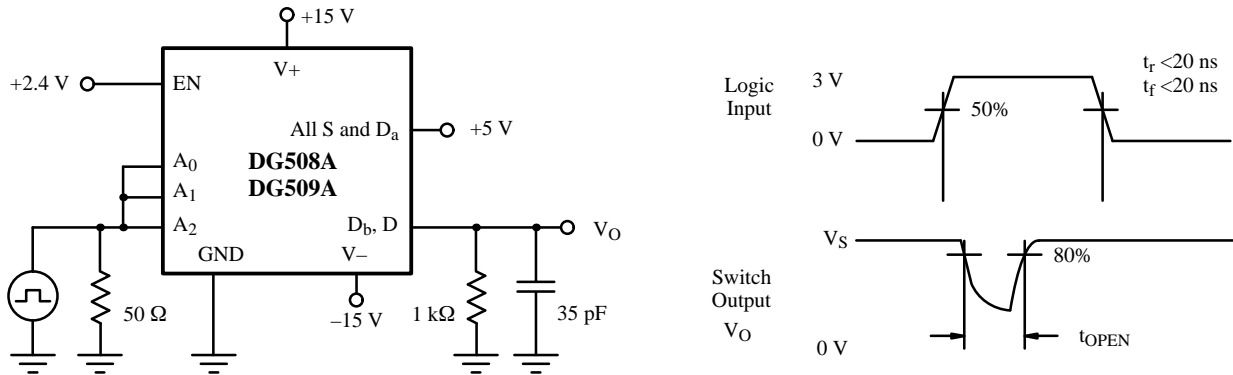


Figure 4. Break-Before-Make Interval

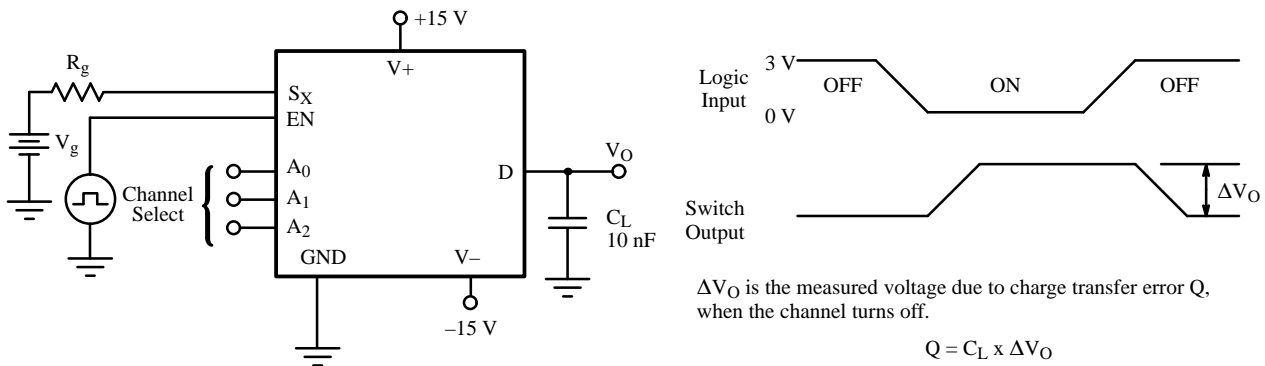


Figure 5. Charge Injection

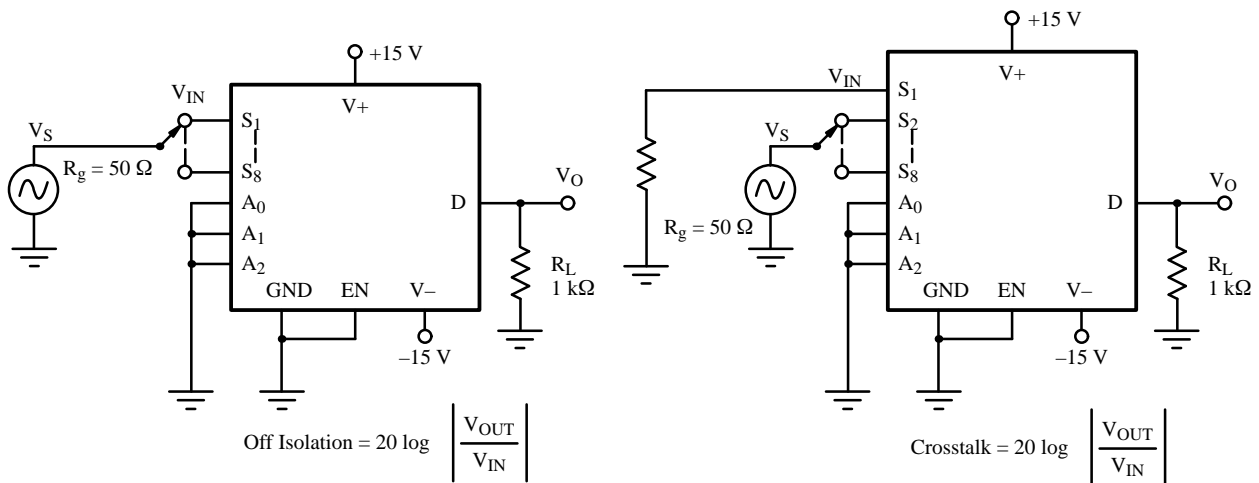


Figure 6. Off Isolation

Figure 7. Crosstalk

Test Circuits (Cont'd)

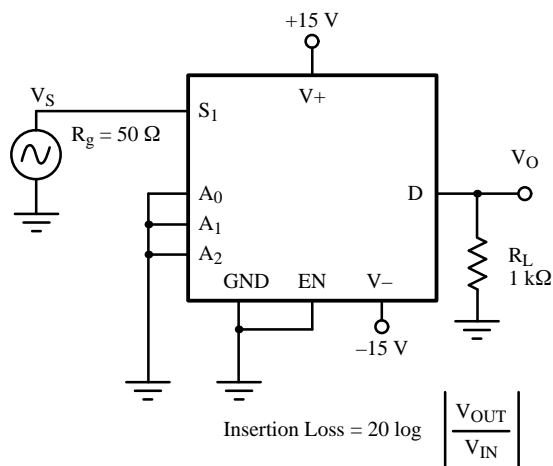


Figure 8. Insertion Loss

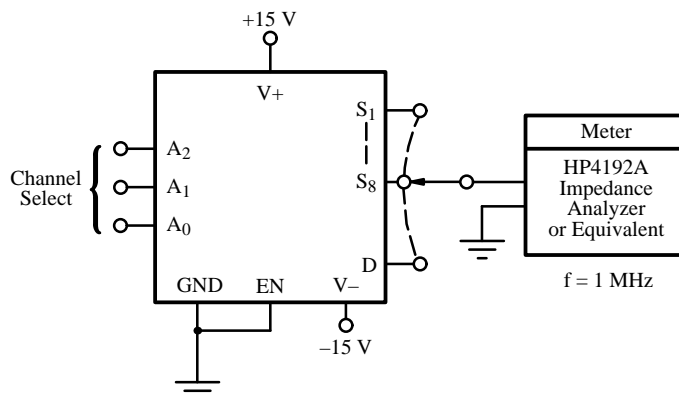


Figure 9. Source Drain Capacitance

Applications^a

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V _{IN} Logic Input Voltage V _{INH(min)} /V _{INL(max)} (V)	V _S or V _D Analog Voltage Range (V)
15	-15	2.4/0.8	-15 to 15
10	-12	2.4/0.8	-12 to 12
12	-10	2.4/0.6	-10 to 10
8 ^b	-8	2.4/0.4	-8 to 8

Notes:

- Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- Operation below ± 8 V is not recommended.

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 11). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V_S and the V- rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

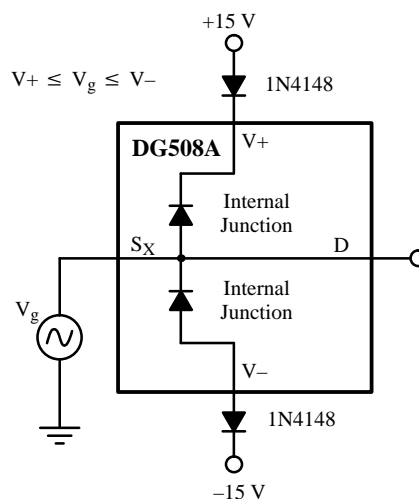


Figure 10. Overvoltage Protection Using Blocking Diodes

Overvoltage Protection (Cont'd)

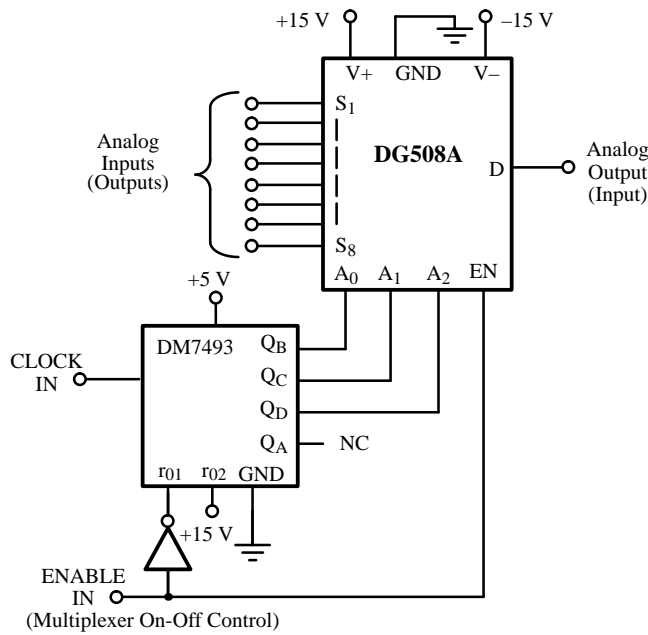


Figure 11. 8-Channel Sequential Multiplexer/ Demultiplexer

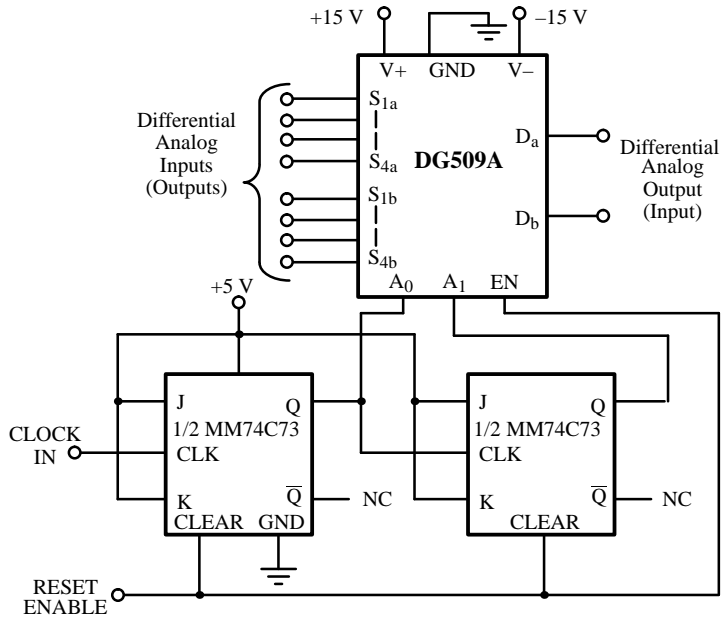


Figure 12. Differential 4-Channel Sequential Multiplexer/ Demultiplexer