CS5112

1.4 A Switching Regulator with 5.0 V, 100 mA Linear Regulator with Watchdog, $\overline{\text{RESET}}$ and $\overline{\text{ENABLE}}$

The CS5112 is a dual output power supply integrated circuit. It contains a 5.0 V ± 2%, 100 mA linear regulator, a watchdog timer, a linear output voltage monitor to provide a Power On Reset (POR) and a 1.4 A current mode PWM switching regulator.

The 5.0 V linear regulator is comprised of an error amplifier, reference, and supervisory functions. It has low internal supply current consumption and provides 1.2 V (typical) dropout voltage at maximum load current.

The watchdog timer circuitry monitors an input signal (WDI) from the microprocessor. It responds to the falling edge of this watchdog signal. If a correct watchdog signal is not received within the externally programmable time, a reset signal is issued.

The externally programmable active reset circuit operates correctly for an output voltage (V_{LIN}) as low as 1.0 V. During power up, or if the output voltage shifts below the regulation limit, $\overline{\text{RESET}}$ toggles low and remains low for the duration of the delay after proper output voltage regulation is restored. Additionally a reset pulse is issued if the correct watchdog is not received within the programmed time. Reset pulses continue until the correct watchdog signal is received. The reset pulse width and frequency, as well as the Power On Reset delay, are set by one external RC network.

The current mode PWM switching regulator is comprised of an error amplifier with selectable feedback inputs, a current sense amplifier, an adjustable oscillator, and a 1.4 A output power switch with anti–saturation control. The switching regulator can be configured in a variety of topologies.

The CS5112 is load dump capable and has protection circuitry which includes current limit on the linear and switcher outputs, and an overtemperature limiter.

Features

- Linear Regulator
  - 5.0 V ± 2% @ 100 mA
- Switching Regulator
  - 1.4 A Peak Internal Switch
  - 120 kHz Maximum Switching Frequency
  - 5.0 V to 26 V Operating Supply Range
- Smart Functions
  - Watchdog
  - $\overline{\text{RESET}}$
  - $\overline{\text{ENABLE}}$
- Protection
  - Overtemperature
  - Current Limit
- Internally Fused Leads in SO–24L Package

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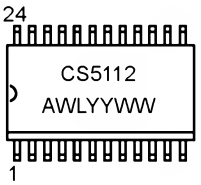
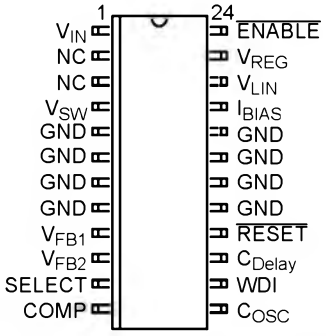
SO–24L
DWF SUFFIX
CASE 751E

MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
CS5112YDWF24	SO–24L	31 Units/Rail
CS5112YDWFR24	SO–24L	1000 Tape & Reel

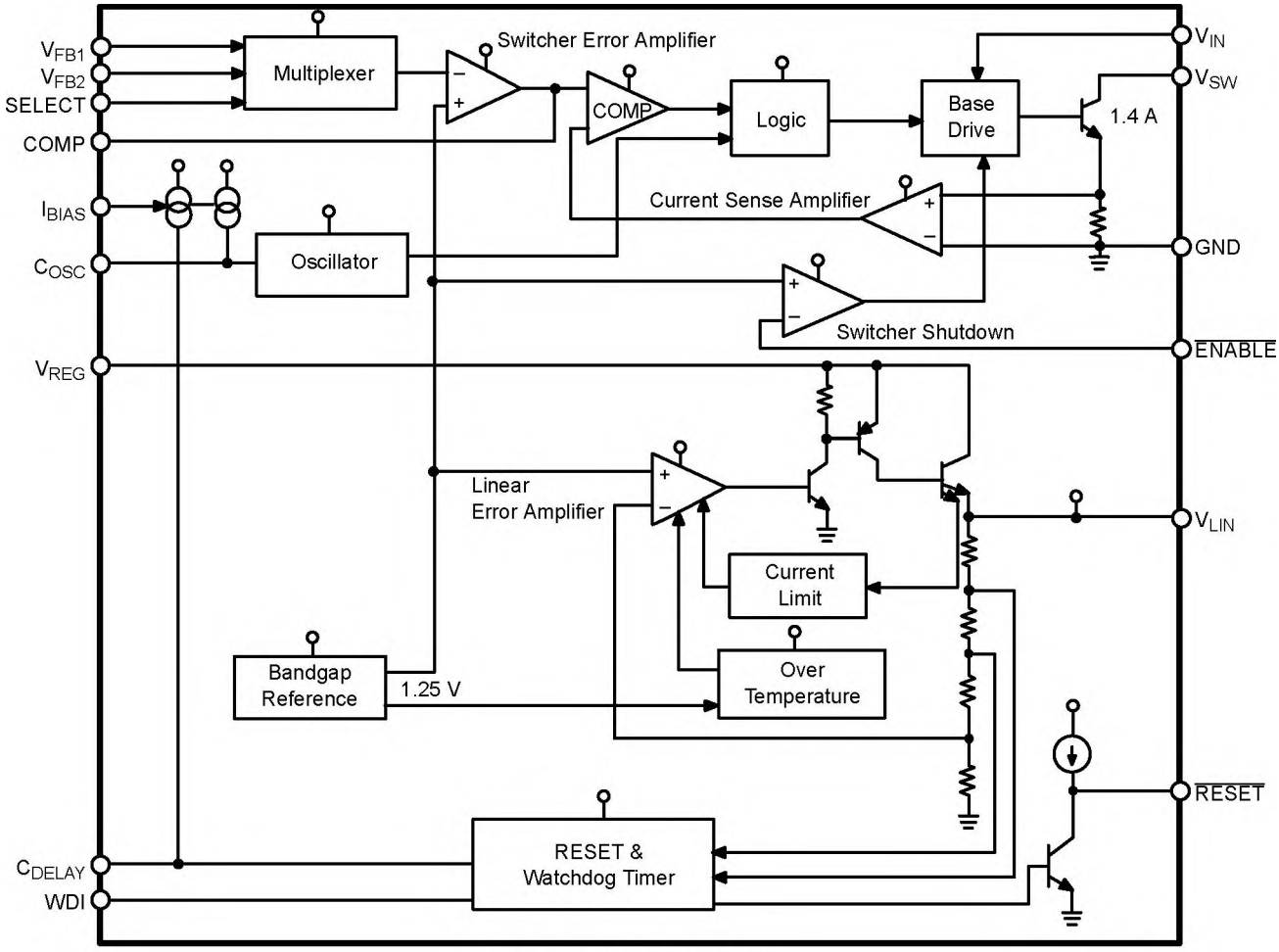


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
Logic Inputs/Outputs ($\overline{\text{ENABLE}}$, SELECT, WDI, $\overline{\text{RESET}}$)	–0.3 to V_{LIN}	V
V_{LIN}	–0.3 to 10	
V_{IN}, V_{REG}: DC Input Voltage Peak Transient Voltage (26 V Load Dump @ 14 V V_{IN})	–0.3 to 26 –0.3 to 40	V V
V_{SW} Peak Transient Voltage	54	V
C_{OSC}, C_{Delay}, COMP, V_{FB1}, V_{FB2}	–0.3 to V_{LIM}	V
Power Dissipation	Internally Limited	–
V_{LIN} Output Current	Internally Limited	–
V_{SW} Output Current	Internally Limited	–
$\overline{\text{RESET}}$ Output Sink Current	5.0	mA
ESD Susceptibility (Human Body Model)	2.0	kV
ESD Susceptibility (Machine Model)	200	V
Storage Temperature	–65 to 150	°C
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (5.0 V ≤ V_{IN} ≤ 26 V and –40°C ≤ T_J ≤ 150°C, C_{OUT} = 100 μF (ESR ≤ 8.0 Ω), C_{Delay} = 0.1 μF, R_{BIAS} = 64.9 kΩ, C_{OSC} = 390 pF, C_{COMP} = 0.1 μF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
General					
I_{IN} Off Current	6.6 V ≤ V_{IN} ≤ 26 V, I_{SW} = 0 A	–	–	2.0	mA
I_{IN} On Current	6.6 V ≤ V_{IN} ≤ 26 V, I_{SW} = 1.4 A	–	30	70	mA
I_{REG} Current	I_{LIN} = 100 mA, 6.6 V ≤ V_{IN} ≤ 26 V	–	–	6.0	mA
Thermal Limit	Guaranteed by Design	160	–	210	°C
5.0 V Regulator Section					
V_{LIN} Output Voltage	6.6 V ≤ V_{REG} ≤ 26 V, 1.0 mA ≤ I_{LIN} ≤ 100 mA	4.9	5.0	5.1	V
Dropout Voltage	(V_{REG} – V_{LIN}) @ I_{LIN} = 100 mA	–	1.2	1.5	V
Line Regulation	6.6 V ≤ V_{REG} ≤ 26 V, I_{LIN} = 5.0 mA	–	5.0	25	mV
Load Regulation	V_{REG} = 19 V, 1.0 mA ≤ I_{LIN} ≤ 100 mA	–	5.0	25	mV
Current Limit	6.6 V ≤ V_{REG} ≤ 26 V	120	–	–	mA
DC Ripple Rejection	14 V ≤ V_{REG} ≤ 24 V	60	75	–	dB
$\overline{\text{RESET}}$ Section					
Low Threshold (V_{RTL})	V_{LIN} Decreasing	4.05	4.25	4.45	V
High Threshold (V_{RTH})	V_{LIN} Increasing	4.2	4.45	4.7	V
Hysteresis	V_{RTH} – V_{RTL}	140	190	240	mV
Active High	V_{LIN} > V_{RTH}, I_{RESET} = –25 μA	V_{LIN} – 0.5	–	–	V
Active Low	V_{LIN} = 1.0 V, 10 kΩ Pull–Up from $\overline{\text{RESET}}$ to V_{LIN}	–	–	0.4	V
	V_{LIN} = 4.0 V, I_{RESET} = 1.0 mA	–	–	0.7	V
Delay	Invalid WDI	6.25	8.78	11	ms
Power On Delay	V_{LIN} Crossing V_{RTH}	6.25	–	–	ms
Watchdog Input (WDI)					
VIH	Peak WDI Needed to Activate $\overline{\text{RESET}}$	–	–	2.0	V
VIL	–	0.8	–	–	V
Hysteresis	Note 2	25	50	–	mV
Pull–Up Resistor	WDI = 0 V	20	50	100	kΩ
Low Threshold	–	6.25	8.78	11	ms
Floating Input Voltage	–	3.5	–	–	V
WDI Pulse Width	–	–	–	5.0	μs
Switcher Section					
Minimum Operating Input Voltage	–	–	–	5.0	V
Switching Frequency	Refer to Figure 5	80	95	110	kHz
Switch Saturation Voltage	I_{SW} = 1.4 A	0.7	1.1	1.6	V
Output Current Limit	–	1.4	–	2.5	A
Max Switching Frequency	V_{SW} = 7.5 V with 50 Ω Load, Refer to Figure 5	120	–	–	kHz
V_{FB1} Regulation Voltage	–	1.206	1.25	1.294	V

2. Guaranteed by design, not 100% tested in productions.

ELECTRICAL CHARACTERISTICS (continued) (5.0 V ≤ V_{IN} ≤ 26 V and –40°C ≤ T_J ≤ 150°C, C_{OUT} = 100 μF (ESR ≤ 8.0 Ω), C_{Delay} = 0.1 μF, R_{BIAS} = 64.9 kΩ, C_{OSC} = 390 pF, C_{COMP} = 0.1 μF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Switcher Section (continued)					
V_{FB2} Regulation Voltage	–	1.206	1.25	1.294	V
V_{FB1}, V_{FB2} Input Current	V_{FB1} = V_{FB2} = 5.0 V	–	–	1.0	μA
Oscillator Charge Current	C_{OSC} = 0 V	35	40	45	μA
Oscillator Discharge Current	C_{OSC} = V40	270	320	370	μA
C_{Delay} Charge Current	C_{Delay} = 0 V	35	40	45	μA
Switcher Max Duty Cycle	V_{SW} = 5.0 V with 50 Ω Load, V_{FB1} = V_{FB2} = 1.0 V	72	85	95	%
Current Sense Amp Gain	I_{SW} = 2.3 A	–	7.0	–	V/V
Error Amp DC Gain	–	–	67	–	dB
Error Amp Transconductance	–	–	2700	–	μA/V
$\overline{\text{ENABLE}}$ Input					
VIL	–	0.8	1.24	–	V
VIH	–	–	1.3	2.0	V
Hysteresis	–	–	60	–	mV
Input Impedance	–	10	20	40	kΩ
Select Input					
VIL (Selects V_{FB1})	4.9 ≤ V_{LIN} ≤ 5.1	0.8	1.25	–	V
VIH (Selects V_{FB2})	4.9 ≤ V_{LIN} ≤ 5.1	–	1.25	2.0	V
SELECT Pull–Up	SELECT = 0 V	10	24	50	kΩ
Floating Input Voltage	–	3.5	4.5	–	V

PIN FUNCTION DESCRIPTION

PACKAGE PIN # SO–24L	PIN SYMBOL	FUNCTION
1	V_{IN}	Supply voltage.
2, 3	NC	No connection.
4	V_{SW}	Collector of NPN power switch for switching regulator section.
5, 6, 7, 8, 17, 18, 19, 20	GND	Connected to the heat removing leads.
9	V_{FB1}	Feedback input voltage 1 (referenced to 1.25 V).
10	V_{FB2}	Feedback input voltage 2 (referenced to 1.25 V).
11	SELECT	Logic level input that selects either V_{FB1} or V_{FB2}. An open selects V_{FB2}. Connect to GND to select V_{FB1}.
12	COMP	Output of the transconductance error amplifier.
13	C_{OSC}	A capacitor connected to GND sets the switching frequency. Refer to Figure 5.
14	WDI	Watchdog input. Active on falling edge.
15	C_{Delay}	A capacitor connected to GND sets the Power On Reset and Watchdog time.
16	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ output. Active low if V_{LIN} is below the regulation limit. If watchdog timeout is reached, a reset pulse train is issued.
21	I_{BIAS}	A resistor connected to GND sets internal bias currents as well as the C_{OSC} and C_{Delay} charge currents.

PIN FUNCTION DESCRIPTION (continued)

PACKAGE PIN # SO–24L	PIN SYMBOL	FUNCTION
22	V_{LIN}	Regulated 5.0 V output from the linear regulator section.
23	V_{REG}	Input voltage to the linear regulator and the internal supply circuitry.
24	$\overline{ENABLE}$	Logic level input to shut down the switching regulator.

TYPICAL PERFORMANCE CHARACTERISTICS

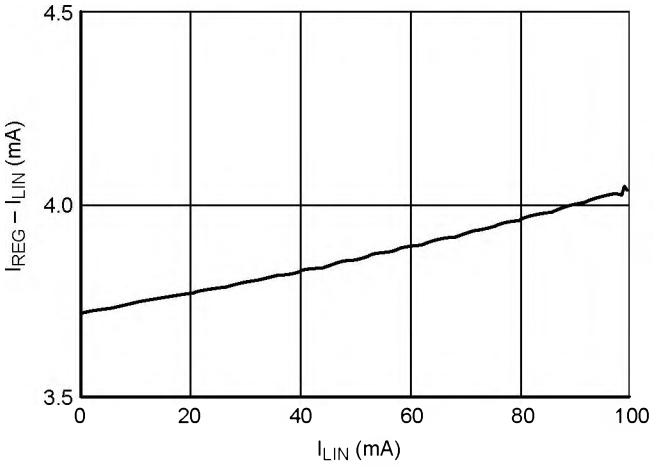


Figure 2. 5.0 V Regulator Bias Current vs. Load Current

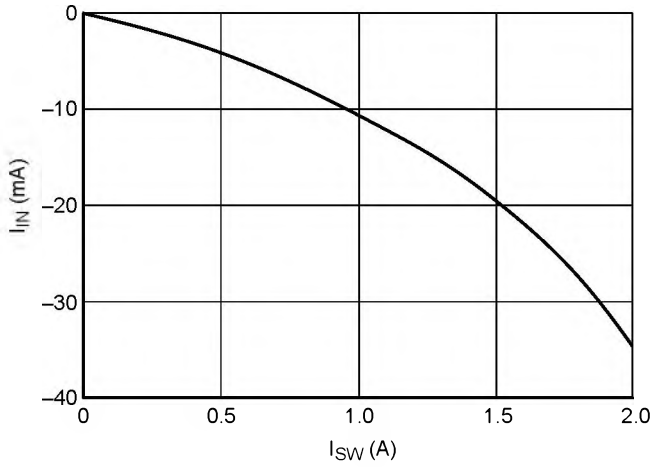


Figure 3. Supply Current vs. Switch Current

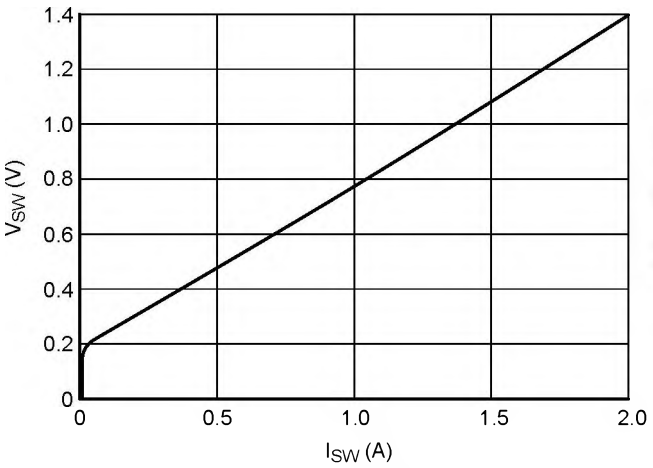


Figure 4. Switch Saturation Voltage

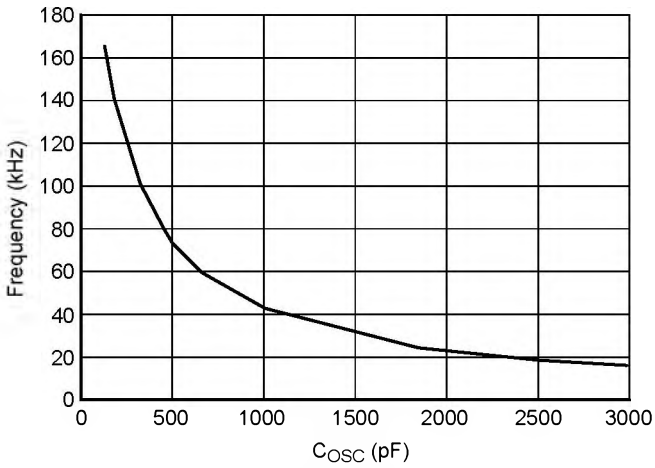


Figure 5. Oscillator Frequency (kHz) vs. C_{OSC} (pF), Assuming R_{BIAS} = 64.9 kΩ

CIRCUIT DESCRIPTION

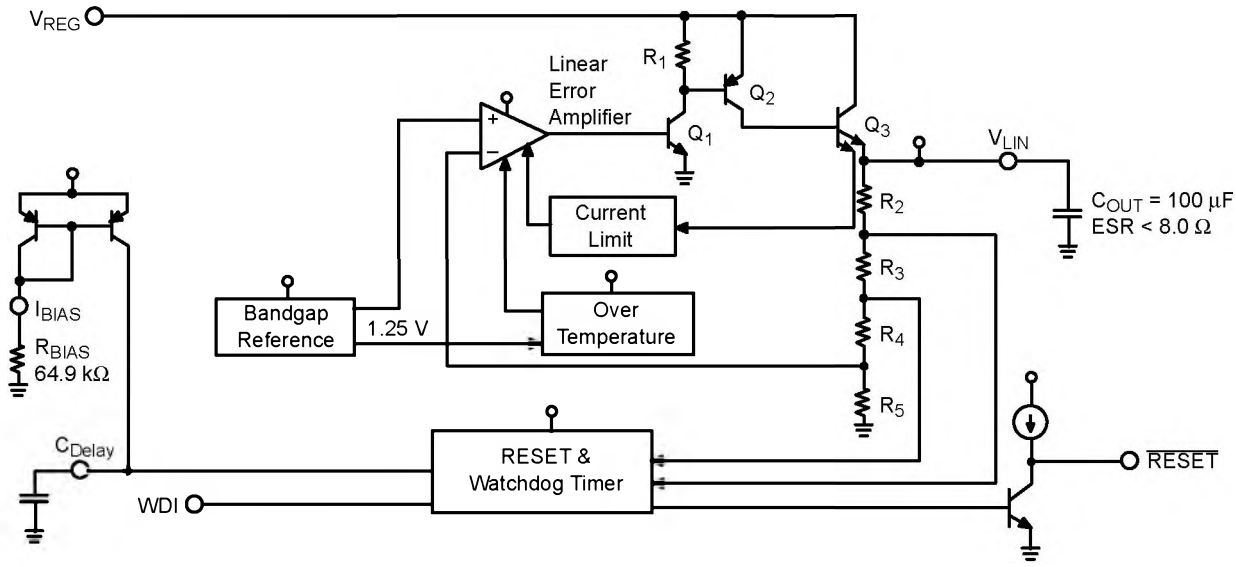


Figure 6. Block Diagram of 5.0 V Linear Regulator Portion of the CS5112

5.0 V LINEAR REGULATOR

The 5.0 V linear regulator consists of an error amplifier, bandgap voltage reference, and a composite pass transistor.

The 5.0 V linear regulator circuitry is shown in Figure 6. When an unregulated voltage greater than 6.6 V is applied to the V_{REG} input, a 5.0 V regulated DC voltage will be present at V_{LIN}. For proper operation of the 5.0 V linear regulator, the I_{BIAS} lead must have a 64.9 kΩ pull down resistor to ground. A 100 µF or larger capacitor with an ESR < 8.0 Ω must be connected between V_{LIN} and ground. To operate the 5.0 V linear regulator as an independent regulator (i.e. separate from the switching supply), the input voltage must be tied to the V_{REG} lead.

As the voltage at the V_{REG} input is increased, Q_1 is turned on. Q_1 provides base drive for Q_2 which in turn provides base current for Q_3. As Q_3 is turned on, the output voltage, V_{LIN}, begins to rise as Q_3's output current charges the output capacitor, C_{OUT}. Once V_{LIN} rises to a certain level, the error amplifier becomes biased and provides the appropriate amount of base current to Q_1. The error amplifier monitors the scaled output voltage via an internal voltage divider, R_2 through R_5, and compares it to the bandgap voltage reference. The error amplifier output or error signal is an output current equal to the error amplifier's input differential voltage times the transconductance of the amplifier. Therefore, the error amplifier varies the base current to Q_1, which provides bias to Q_2 and Q_3, based on the difference between the reference voltage and the scaled V_{LIN} output voltage.

CONTROL FUNCTIONS

The watchdog timer circuitry monitors an input signal (WDI) from the microprocessor. It responds to the falling edge of this watchdog signal which it expects to see within an externally programmable time (see Figure 7).

The watchdog time is given by:

$$t_{WDI} = 1.353 \times C_{Delay}R_{BIAS}$$

Using C_{Delay} = 0.1 µF and R_{BIAS} = 64.9 kΩ gives a time ranging from 6.25 ms to 11 ms assuming ideal components. Based on this, the software must be written so that the watchdog arrives at least every 6.25 ms. In practice, the tolerance of C_{Delay} and R_{BIAS} must be taken into account when calculating the minimum watchdog time (t_{WDI}).

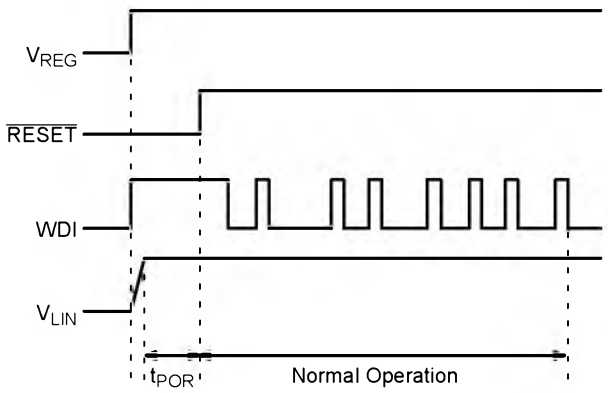
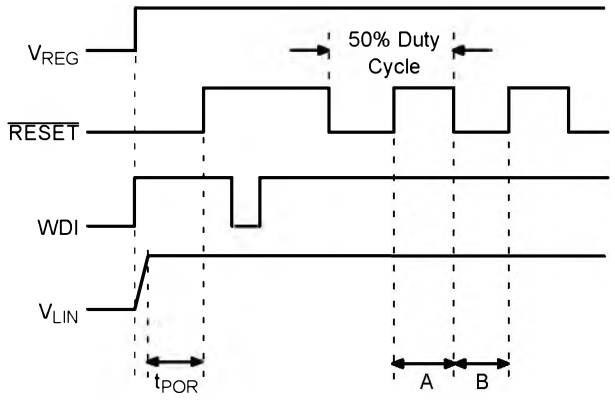


Figure 7. Timing Diagram for Normal Regulator Operation

If a correct watchdog signal is not received within the specified time a reset pulse train is issued until the correct watchdog signal is received. The nominal reset signal in this case is a 5 volt square wave with a 50% duty cycle as shown in Figure 8.



A: Watchdog waiting for low–going transition on WDI
B: $\overline{\text{RESET}}$ stays low for t_{WDI} time

Figure 8. Timing Diagram When WDI Fails to Appear Within the Preset Time Interval, t_{WDI}

The $\overline{\text{RESET}}$ signal frequency is given by:

$$f_{RESET} = \frac{1}{2(t_{WDI})}$$

The Power On Reset (POR) and low voltage $\overline{\text{RESET}}$ use the same circuitry and issue a reset when the linear output voltage is below the regulation limit. After V_{LIN} rises above the minimum specified value, $\overline{\text{RESET}}$ remains low for a fixed period t_{POR} as shown in Figures 9 and 10.

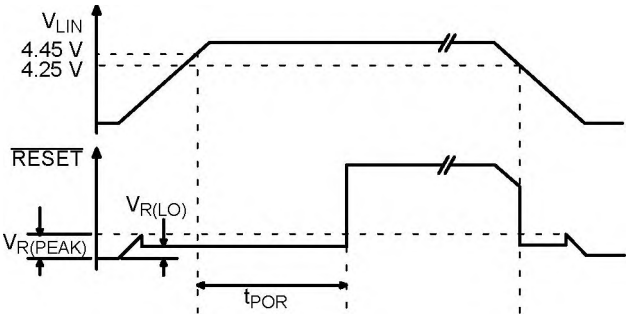


Figure 9. The Power On Reset Time Interval (t_{POR}) Begins When V_{LIN} Rises Above 4.45 V (Typical)

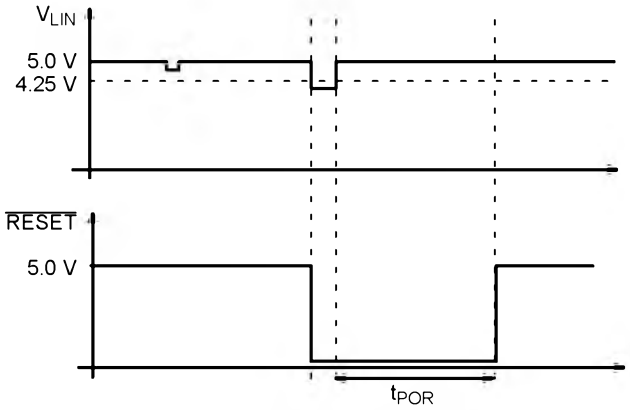


Figure 10. $\overline{\text{RESET}}$ Signal Is Issued Whenever V_{LIN} Falls Below 4.25 V (Typical)

The POR delay (t_{POR}) is given by:

$$t_{POR} = 1.353 \times C_{Delay}R_{BIAS}$$

CURRENT MODE PWM SWITCHING CIRCUITRY

The current mode PWM switching voltage regulator contains an error amplifier with selectable feedback inputs, a current sense amplifier, an adjustable oscillator and a 1.4 A output power switch with antisaturation control. The switching regulator and external components, connected in a boost configuration, are shown in Figure 11.

The switching regulator begins operation when V_{REG} and V_{IN} are raised above 5 volts. V_{REG} is required since the switching supply's control circuitry is powered through V_{LIN}. V_{IN} supplies the base drive to the switcher output transistor.

The output transistor turns on when the oscillator starts to charge the capacitor on C_{OSC}. The output current will develop a voltage drop across the internal sense resistor (R_S). This voltage drop produces a proportional voltage at the output of the current sense amplifier, which is compared to the output of the error amplifier. The error amplifier generates an output voltage which is proportional to the difference between the scaled down output boost voltage (V_{FB1} or V_{FB2}) and the internal bandgap voltage reference. Once the current sense amplifier output exceeds the error amplifier's output voltage, the output transistor is turned off.

The energy stored in the inductor during the output transistor on time is transferred to the load when the output transistor is turned off. The output transistor is turned back

on at the next rising edge of the oscillator. On a cycle by cycle basis, the current mode controller in a discontinuous mode of operation charges the inductor to the appropriate amount of energy, based on the energy demand of the load. Figure 12 shows the typical current and voltage waveforms for a boost supply operating in the discontinuous mode.

Notes:

1. Refer to Figure 5 to determine oscillator frequency.
2. The switching regulator can be disabled by providing a logic high at the $\overline{\text{ENABLE}}$ input.
3. The boost output voltage can be controlled dynamically by the feedback select input. If select is open, V_{FB2} is selected. If select is low, then V_{FB1} is selected.

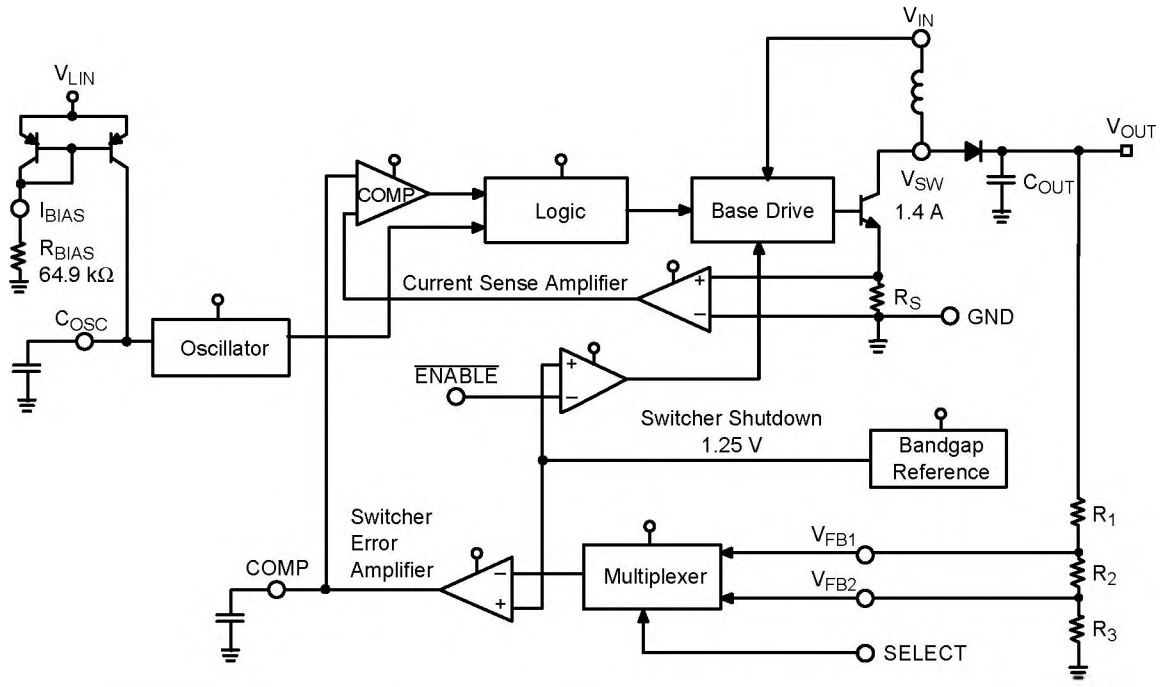


Figure 11. Block Diagram of the 1.4 A Current Mode Control Switching Regulator Portion of the CS5112 in a Boost Configuration

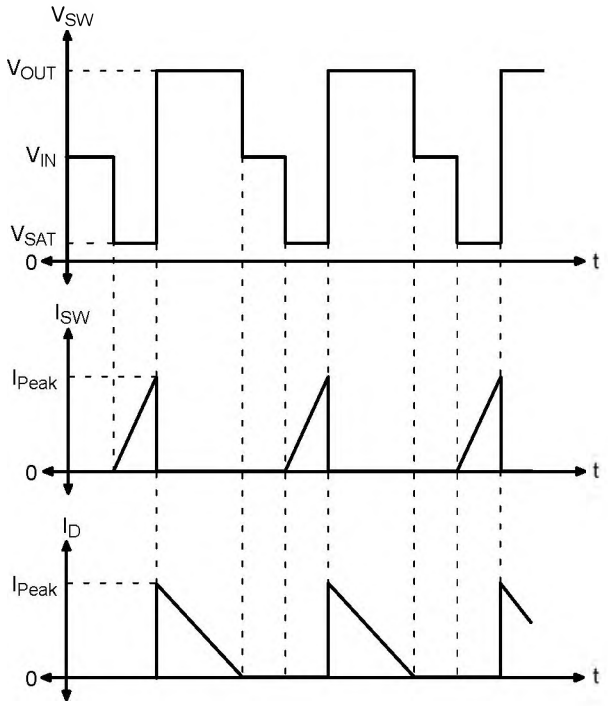


Figure 12. Voltage and Current Waveforms for Boost Topology in CS5112

PROTECTION CIRCUITRY

The current out of V_{LIN} is sensed in order to limit excessive power dissipation in the linear output transistor over the output range of 0 V to regulation. Also, the current into V_{SW} is sensed in order to provide the current limit function in the switcher output transistor.

If the die temperature is increased above 160°C, either due to excessive ambient temperature or excessive power dissipation, the drive to the linear output transistor is reduced proportionally with increasing die temperature. Therefore, V_{LIN} will decrease with increasing die temperature above 160°C. Since the switcher control circuitry is powered through V_{LIN}, the switcher performance, including current limit, will be affected by the decrease in V_{LIN}.

APPLICATION NOTES

DESIGN PROCEDURE FOR BOOST TOPOLOGY

This section outlines a procedure for designing a boost switching power supply operating in the discontinuous mode.

Step 1

Determine the output power required by the load.

$$P_{OUT} = I_{OUT}V_{OUT} \quad (1)$$

Step 2

Choose C_{OSC} based on the target oscillator frequency with an external resistor value, R_{BIAS} = 64.9 kΩ (See Figure 5).

Step 3

Next select the output voltage feedback sense resistor divider as follows (Figure 13).

For V_{FB1} active, choose a value for R_1 and then solve for R_{EQ} where:

$$R_{EQ} = \frac{R_1}{\frac{V_{OUT}}{V_{FB1}} - 1} \quad (2)$$

For V_{FB2} active, find:

$$V_{FB1} = V_{OUT}\left(\frac{R_{EQ}}{R_1 + R_{EQ}}\right) \quad (3)$$

and then calculate R_2 where:

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{V_{FB1} - V_{FB2}}{V_{FB1}/R_{EQ}} \quad (4)$$

Then find R_3, where:

$$R_3 = R_{EQ} - R_2 \quad (5)$$

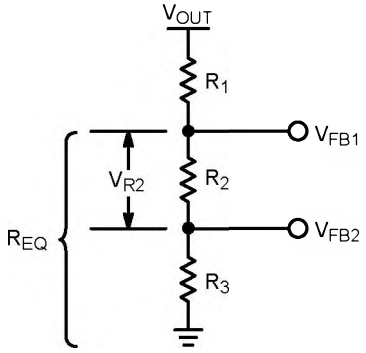


Figure 13. Feedback Sense Resistor Divider Connected Between V_{OUT} and Ground

Step 4

Determine the maximum on time at the minimum oscillator frequency and V_{IN}. For discontinuous operation, all of the stored energy in the inductor is transferred to the load prior to the next cycle. Since the current through the inductor cannot change instantaneously and the inductance is constant, a volt–second balance exists between the on time and off time. The voltage across the inductor during the on cycle is V_{IN} and the voltage across the inductor during the off cycle is $V_{OUT} - V_{IN}$. Therefore:

$$V_{IN}t_{ON} = (V_{OUT} - V_{IN})t_{OFF} \quad (6)$$

where the maximum on time is:

$$t_{ON(MAX)} \approx \left[1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)}}\right]\left[\frac{1}{f_{SW(MIN)}}\right] \quad (7)$$

Step 5

Calculate the maximum inductance allowed for discontinuous operation:

$$L_{(MAX)} = \frac{f_{SW(MIN)}V_{IN}^2{}_{(MIN)}t_{ON}^2{}_{(MAX)}}{2P_{OUT}/\eta} \quad (8)$$

where η = efficiency.

Usually η = 0.75 is a good starting point. The IC's power dissipation should be calculated after the peak current has been determined in Step 6. If the efficiency is less than originally assumed, decrease the efficiency and recalculate the maximum inductance and peak current.

Step 6

Determine the peak inductor current at the minimum inductance, minimum V_{IN} and maximum on time to make sure the inductor current doesn't exceed 1.4 A.

$$I_{PK} = \frac{V_{IN(MIN)}t_{ON(MAX)}}{L_{(MIN)}} \quad (9)$$

Step 7

Determine the minimum output capacitance and maximum ESR based on the allowable output voltage ripple.

$$C_{OUT(MIN)} = \frac{I_{PK}}{8f\Delta V_{RIPPLE}} \quad (10)$$

$$ESR_{(MIN)} = \frac{\Delta V_{RIPPLE}}{I_{PK}} \quad (11)$$

In practice, it is normally necessary to use a larger capacitance value to obtain a low ESR. By placing capacitors in parallel, the equivalent ESR can be reduced.

Step 8

Compensate the feedback loop to guarantee stability under all operating conditions. To do this, we calculate the modulator gain and the feedback resistor network attenuation and set the gain of the error amplifier so that the overall loop gain is 0 dB at the crossover frequency, f_{CO}. In addition, the gain slope should be –20 dB/decade at the crossover frequency.

The low frequency gain of the modulator (i.e. error amplifier output to output voltage) is:

$$\frac{\Delta V_{OUT}}{\Delta V_{EA}} = \frac{I_{PK(MAX)}}{V_{EA(MAX)}}\sqrt{\frac{R_{LOAD}L_f}{2}} \quad (12)$$

where:

$$I_{PK(MAX)} = \frac{V_{EA(MAX)}/G_{CSA}}{R_S} = \frac{2.4\ V/7}{150\ m\Omega} = 2.3\ A \quad (13)$$

The V_{OUT}/V_{EA} transfer function has a pole at:

$$f_p = 1/(\pi R_{LOAD} C_{OUT}) \quad (14)$$

and a zero due to the output capacitor's ESR at:

$$f_z = 1/(2\pi ESR(C_{OUT})) \quad (15)$$

Since the error amplifier reference voltage is 1.25 V, the output voltage must be divided down or attenuated before being applied to the input of the error amplifier. The feedback resistor divider attenuation is:

$$\frac{1.25\ V}{V_{OUT}}$$

The error amplifier in the CS5112 is an operational transconductance amplifier (OTA), with a gain given by:

$$G_{OTA} = gmZ_{OUT} \quad (16)$$

where:

$$gm = \frac{\Delta I_{OUT}}{\Delta V_{IN}} \quad (17)$$

For the CS5112, gm = 2700 μA/V typical.

One possible error amplifier compensation scheme is shown in Figure 14. This gives the error amplifier a gain plot as shown in Figure 15.

For the error amplifier gain shown in Figure 15, a low frequency pole is generated by the error amplifier output impedance and C_1. This is shown by the line AB with a −20 dB/decade slope in Figure 15. The slope changes to zero at point B due to the zero at:

$$f_z = 1/(2\pi R_4 C_1) \quad (18)$$

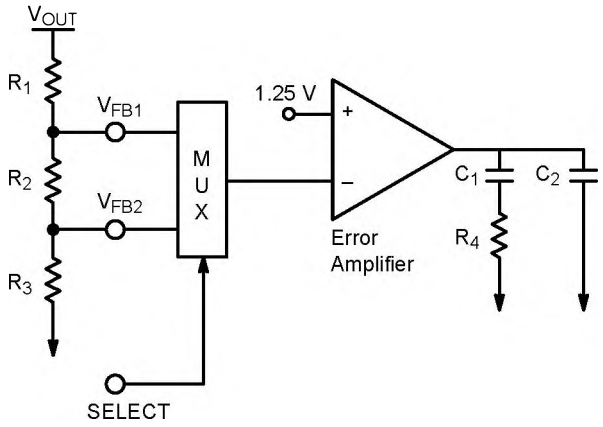


Figure 14. RC Network Used to Compensate the Error Amplifier (OTA)

A pole at point C:

$$f_p = 1/(\pi R_4 C_2) \quad (19)$$

offsets the zero set by the ESR of the output capacitors.

An alternative scheme uses a single capacitor as shown in Figure 16, to roll the gain off at a relatively low frequency.

Step 9

Finally the watchdog timer period and Power on Reset time is determined by:

$$t_{Delay} = 1.353 \times C_{Delay} R_{BIAS} \quad (20)$$

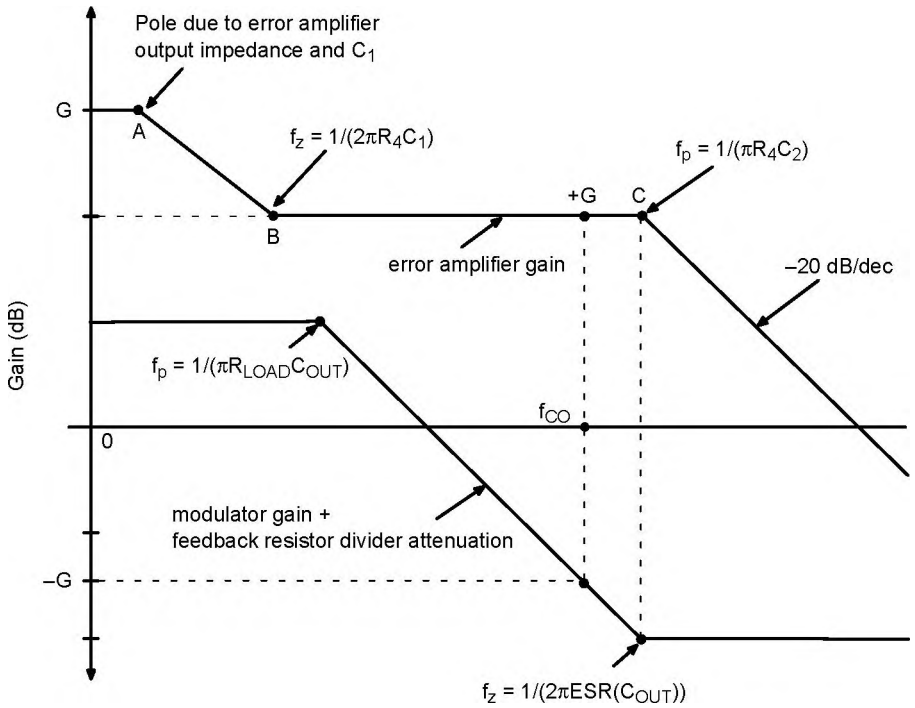


Figure 15. Bode Plot of Error Amplifier (OTA) Gain and Modulator Gain Added to the Feedback Resistor Divider Attenuation

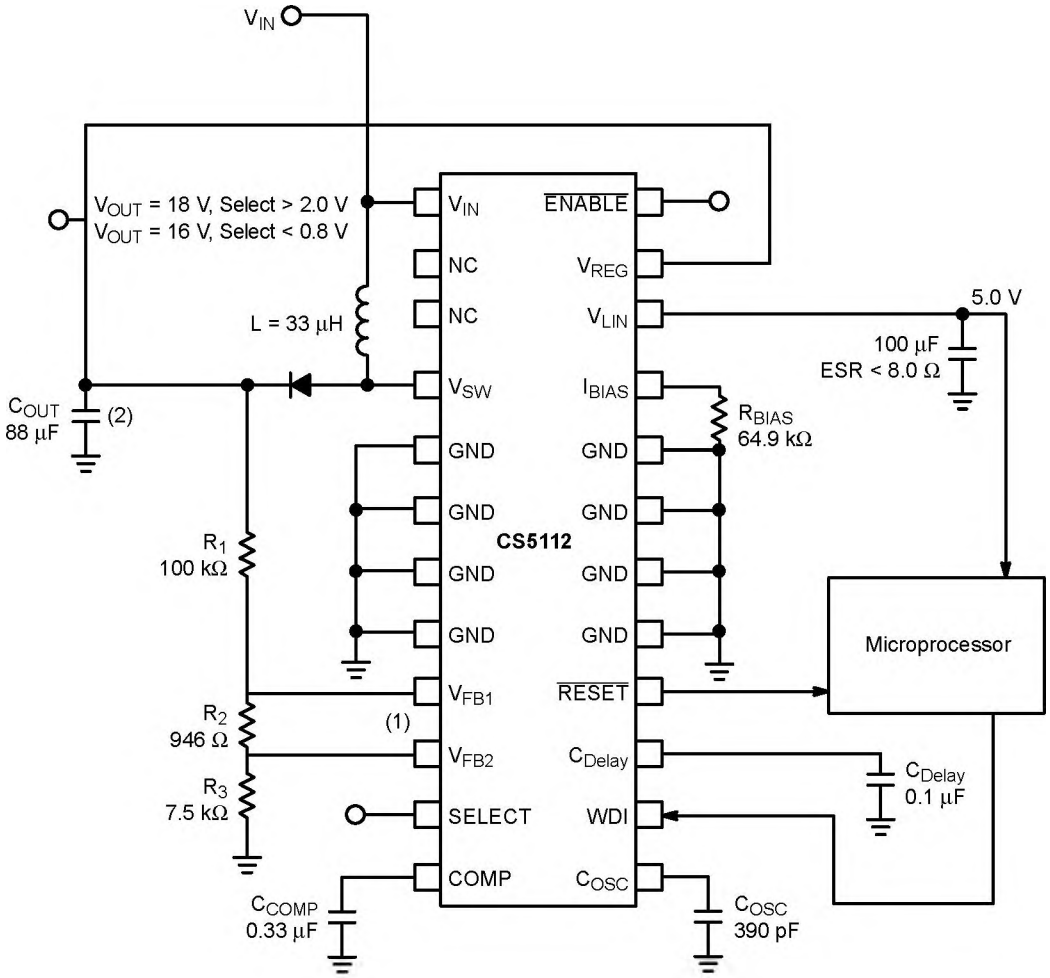


Figure 16. A Typical Application Diagram with External Components Configured in a Boost Topology

LINEAR REGULATOR OUTPUT CURRENT VS. INPUT VOLTAGE

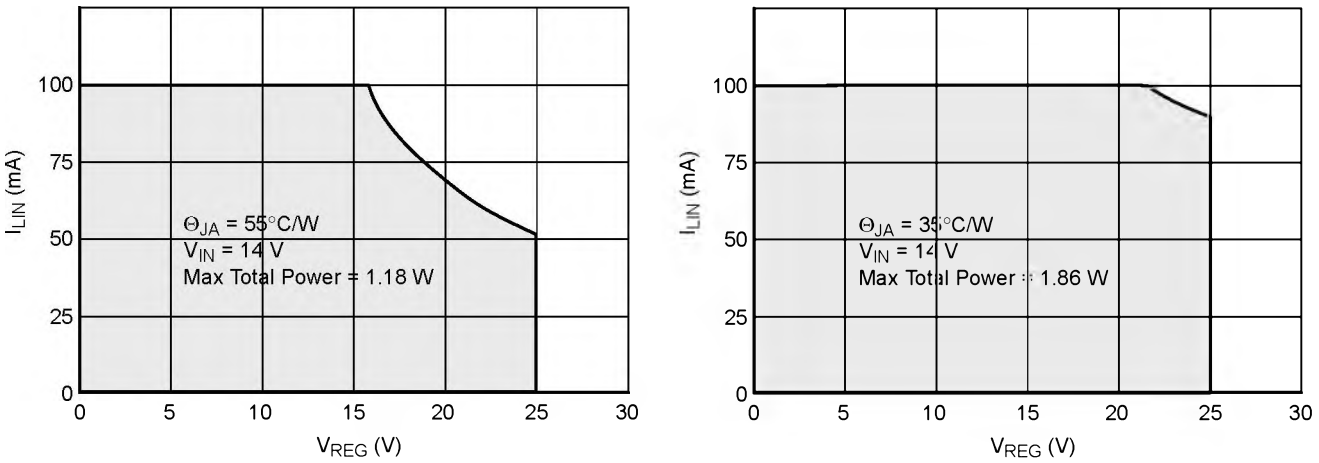


Figure 17. The Shaded Area Shows the Safe Operating Area of the CS5112 as a Function of I_{LIN}, V_{REG}, and Θ_{JA}. Refer to Table 5 for Typical Loads and Voltages.

Table 5.

V_{REG} (V)	V_{IN} (V)	I_{LIN} (mA)	Linear Power Dissipation (W)	Worst Case Switcher Power Available (Θ_{JA} = 55°C/W) (W)	Worst Case Switcher Power Available (Θ_{JA} = 35°C/W) (W)
20	14	25	0.44	0.74	1.42
20	14	50	0.83	0.35	1.03
20	14	75	1.22	*	0.64
20	14	100	1.60	*	0.26
25	14	25	0.60	0.58	1.26
25	14	50	1.11	0.07	0.75
25	14	75	1.62	*	0.24
25	14	100	2.14	*	*

*Subjecting the CS5112 to these conditions will exceed the maximum total power that the part can handle, thereby forcing it into thermal limit.

PACKAGE THERMAL DATA

Parameter		SO−24L	Unit
$R_{\Theta JC}$	Typical	9	°C/W
$R_{\Theta JA}$	Typical	55	°C/W