



CD4522BM/CD4522BC Programmable Divide-By-N 4-Bit BCD Counter

CD4526BM/CD4526BC Programmable Divide-By-N 4-Bit Binary Counter

General Description

The CD4522BM/CD4522BC, CD4526BM/CD4526BC are CMOS programmable cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications, the "0" output is applied to the Preset Enable input. For multi-stage applications, the "0" output is used in conjunction with the CF (Cascade Feedback) input to perform the divide-by-N function. The "0" output is normally at logical "0" level; it will go to a logical "1" state only when the counter is at its terminal count (0000) and if CF is at logical "1" level. Thus, CF acts as an active low inhibit for the "0" output. This feature allows cascade divide-by-N operations with no additional gate required (see Applications section). The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS} .

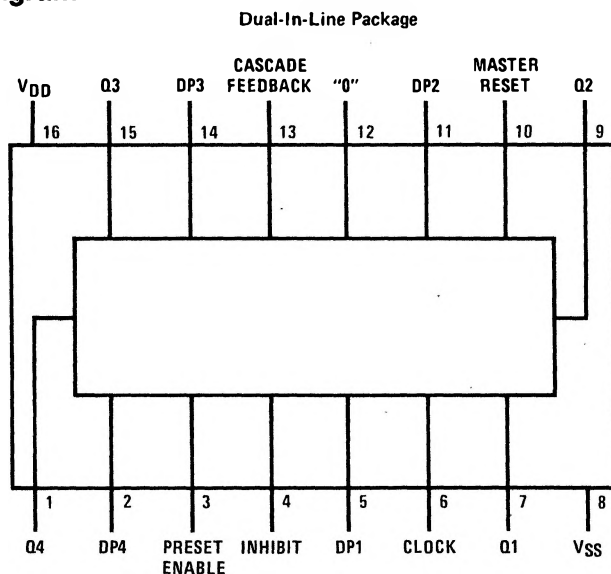
Features

- Wide supply voltage range 3.0V to 18V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Quiescent current = 5 nA/package (typ.) @ $V_{DD} = 5.0V$
- Internally synchronous for high internal and external speed
- Logic edge-clocked design—incremented on positive transition of Clock or negative transition of Clock Inhibit
- Medium speed 7.7 MHz (typ.) @ $V_{DD} = 10V$
- Asynchronous Preset Enable

Applications

- Programmable down counter
- Programmable frequency divider
- Frequency synthesizers
- Phase-locked loops

Connection Diagram



TOP VIEW

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	-0.5 to +18 V _{DC}
V_{IN} Input Voltage	-0.5 to V_{DD} +0.5 V _{DC}
T_S Storage Temperature Range	-65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V _{DC}
V_{IN} Input Voltage	0 to V_{DD} V _{DC}
T_A Operating Temperature Range	-55°C to +125°C
CD4522BM, CD4526BM	-40°C to +85°C
CD4522BC, CD4526BC	

DC Electrical Characteristics CD4522BM, CD4526BM (Note 2)

PARAMETER	CONDITIONS	-55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		5		0.005	5		150	μA
	$V_{DD} = 10V$		10		0.010	10		300	μA
	$V_{DD} = 15V$		20		0.015	20		600	μA
V_{OL} Low Level Output Voltage	$ I_{OL} < 1 \mu A$								
	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$		0.05		0	0.05		0.05	V
	$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$ I_{OH} < 1 \mu A$								
	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5			1.5		1.5	V
	$V_{DD} = 10V, V_O = 1.0V$ or 9.0V		3.0			3.0		3.0	V
	$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5			3.5		V
	$V_{DD} = 10V, V_O = 1.0V$ or 9.0V	7.0		7.0			7.0		V
	$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
	$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
	$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
	$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
	$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN} Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		-10^{-5}	-0.1		-1.0	μA
	$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4522BC, CD4526BC (Note 2)

PARAMETER	CONDITIONS	-40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		20		0.005	20		150	μA
	$V_{DD} = 10V$		40		0.010	40		300	μA
	$V_{DD} = 15V$		80		0.015	80		600	μA
V_{OL} Low Level Output Voltage	$ I_{OL} < 1 \mu A$								
	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$		0.05		0	0.05		0.05	V
	$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$ I_{OH} < 1 \mu A$								
	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5			1.5		1.5	V
	$V_{DD} = 10V, V_O = 1.0V$ or 9.0V		3.0			3.0		3.0	V
	$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Continued) CD4522BC, CD4526BC (Note 2)

PARAMETER	CONDITIONS	-40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V _{IH} High Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V	3.5		3.5			3.5		V
	V _{DD} = 10V, V _O = 1.0V or 9.0V	7.0		7.0			7.0		V
	V _{DD} = 15V, V _O = 1.5V or 13.5V	11.0		11.0			11.0		V
I _{OL} Low Level Output Current	V _{DD} = 5V, V _O = 0.4V	0.52		0.44	0.88		0.36		mA
	V _{DD} = 10V, V _O = 0.5V	1.3		1.1	2.25		0.9		mA
	V _{DD} = 15V, V _O = 1.5V	3.6		3.0	8.8		2.4		mA
I _{OH} High Level Output Current	V _{DD} = 5V, V _O = 4.6V	-0.52		-0.44	-0.88		-0.36		mA
	V _{DD} = 10V, V _O = 9.5V	-1.3		-1.1	-2.25		-0.9		mA
	V _{DD} = 15V, V _O = 13.5V	-3.6		-3.0	-8.8		-2.4		mA
I _{IN} Input Current	V _{DD} = 15V, V _{IN} = 0V		-0.3		-10 ⁻⁵	-0.3		-1.0	μA
	V _{DD} = 15V, V _{IN} = 15V		0.3		10 ⁻⁵	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t _{THL} or t _{TLH} Output Transition Time	V _{DD} = 5V		100	200	ns
	V _{DD} = 10V		50	100	ns
	V _{DD} = 15V		40	80	ns
t _{PHL} & t _{PLH} Propagation Delay Time From Clock to Q Outputs	V _{DD} = 5V		350	825	ns
	V _{DD} = 10V		130	345	ns
	V _{DD} = 15V		90	240	ns
t _{PHL} & t _{PLH} Propagation Delay Time From Clock to "0" Output	V _{DD} = 5V		200	500	ns
	V _{DD} = 10V		80	250	ns
	V _{DD} = 15V		60	190	ns
P _{WC} Minimum Clock Pulse Width	V _{DD} = 5V		120	280	ns
	V _{DD} = 10V		50	120	ns
	V _{DD} = 15V		35	85	ns
f _{CL} Maximum Clock Pulse Frequency	V _{DD} = 5V	1.5	2.9		MHz
	V _{DD} = 10V	3.0	7.7		MHz
	V _{DD} = 15V	4.0	11		MHz
t _{rCL} & t _{fCL} Maximum Clock or Inhibit Rise and Fall Time	V _{DD} = 5V	15			μs
	V _{DD} = 10V	15			μs
	V _{DD} = 15V	15			μs
t _{HOLD} Hold Time	V _{DD} = 5V		40	125	ns
	V _{DD} = 10V		25	50	ns
	V _{DD} = 15V		20	40	ns
P _{WPE} Minimum Preset Enable Pulse Width	V _{DD} = 5V		120	280	ns
	V _{DD} = 10V		50	120	ns
	V _{DD} = 15V		35	85	ns
P _{WMR} Minimum Master Reset Pulse Width	V _{DD} = 5V		160	350	ns
	V _{DD} = 10V		75	180	ns
	V _{DD} = 15V		50	120	ns
C _{IN} Input Capacitance	(Note 3)		5	7.5	pF
C _{PD} Power Dissipation Capacitance	Per Package (Note 4)		100		μF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

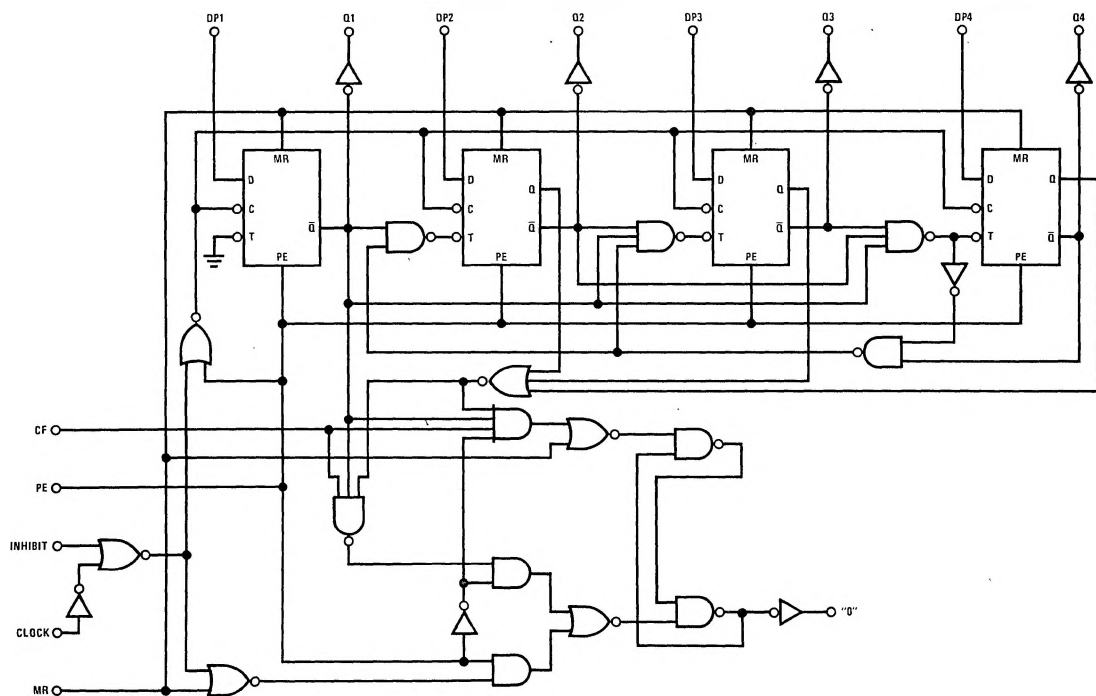
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

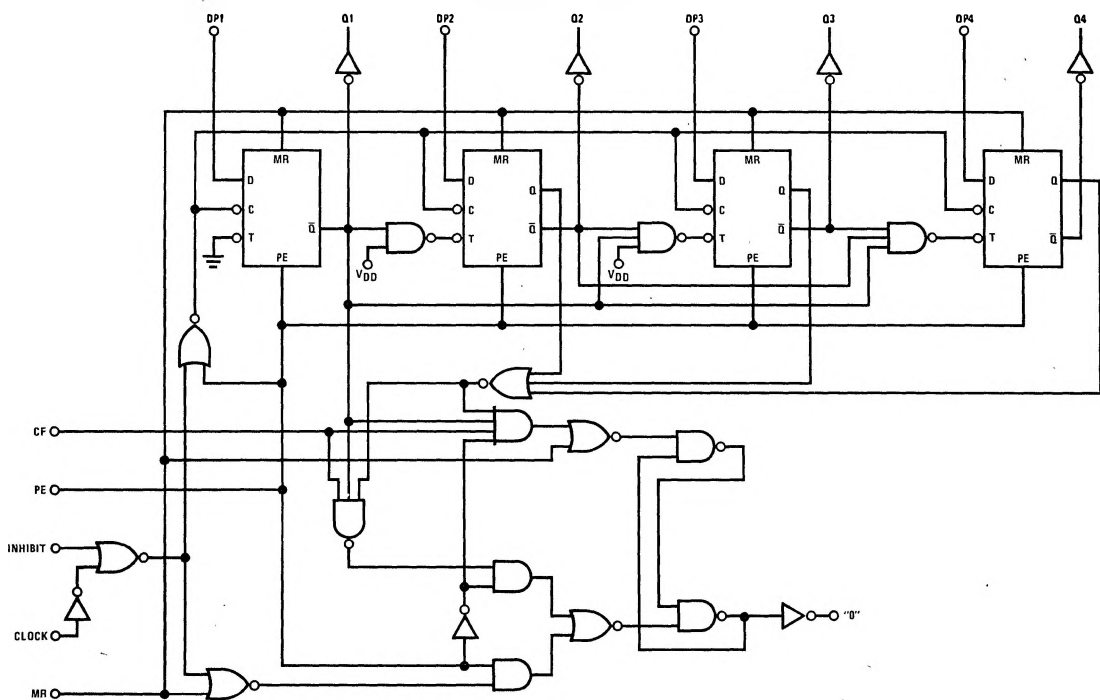
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Logic Diagrams

CD4522BM/CD4522BC



CD4526BM/CD4526BC



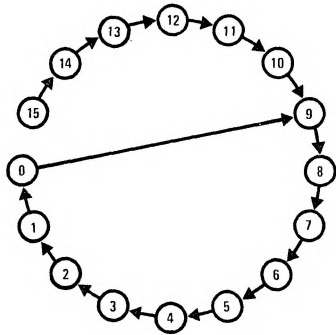
Truth Tables and Count Sequences

Both Types

CLOCK	INHIBIT	PRESET ENABLE	MASTER RESET	ACTION
0	0	0	0	No count
	0	0	0	Count 1
X	1	0	0	No count
1		0	0	Count 1
X	X	1	0	Preset
X	X	X	1	Reset

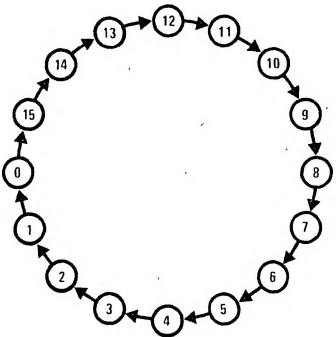
CD4522BM/CD4522BC

COUNT	OUTPUT			
	Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



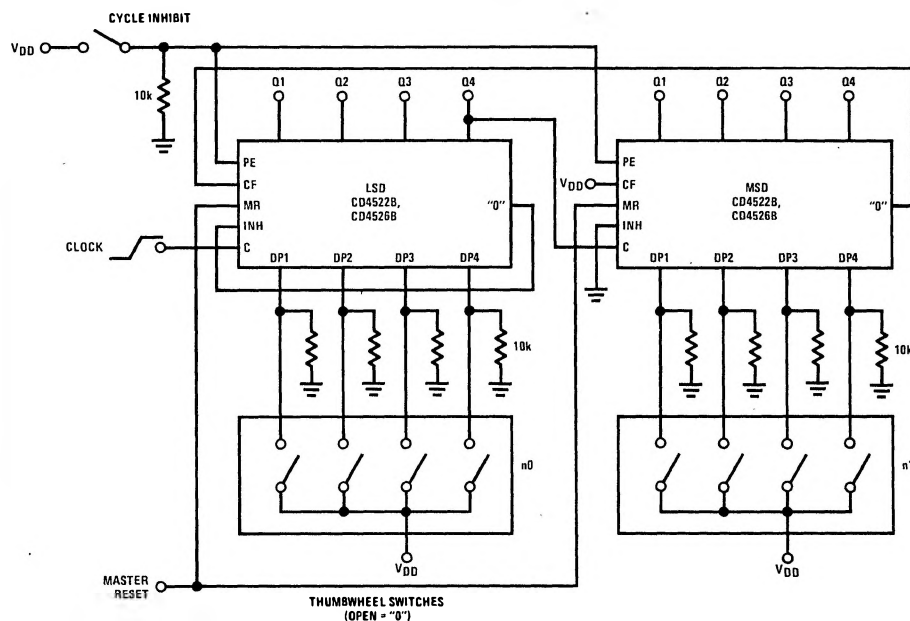
CD4526BM/CD4526BC

COUNT	OUTPUT			
	Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



Typical Applications

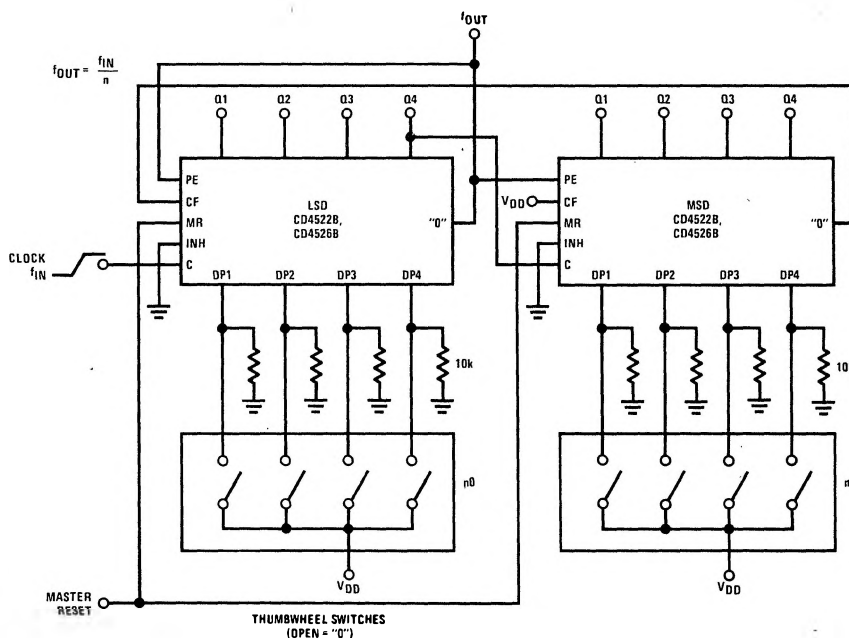
2-Stage Programmable Down Counter



COUNTING CYCLE

LSD	MSD
n0	n0-1
1	n1
0	1
9 (15)	0
8 (14)	
1	n1-1
0	1
9 (15)	0
8 (14)	
1	0
0	STOP

2-Stage Programmable Frequency Divider



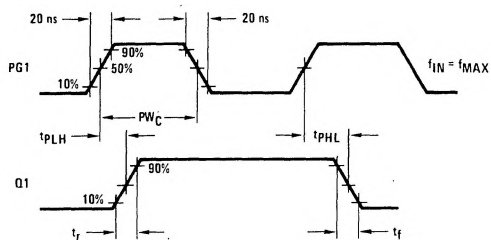
COUNTING CYCLE

LSD	MSD
n0	n0-1
1	n1
0	1
9 (15)	0
8 (14)	
1	n1-1
0	1
9 (15)	0
8 (14)	
1	0
0	REPEAT CYCLE

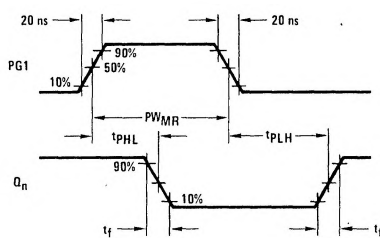
Note. When cascading more than 2 packages, tie "0" output of the nth package to CF input of the (n-1)th package for all n = 2, 3.

Switching Time Waveforms

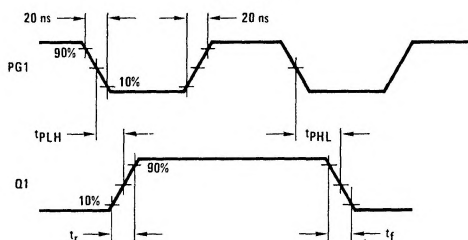
Test No. 1



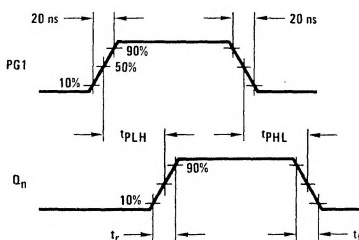
Test No. 4



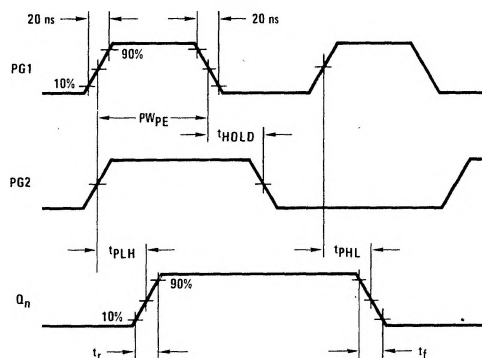
Test No. 2



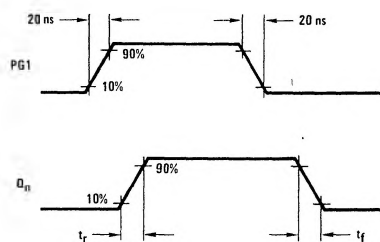
Tests No. 5 and 7



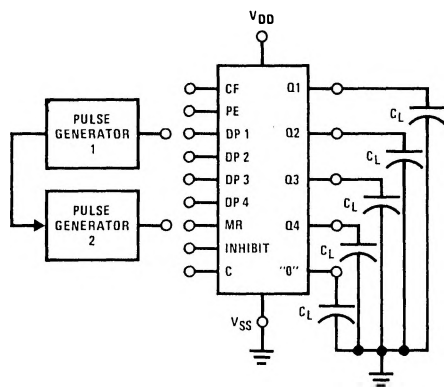
Test No. 3



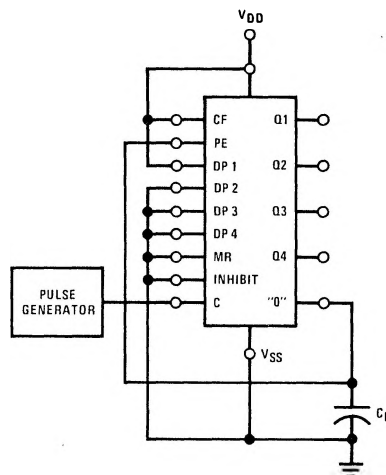
Test No. 6



AC Test Circuits



a) Tests No. 1-6



b) Test No. 7

FIGURE 1. Test Circuit

Test Conditions

TABLE I

CHARACTERISTIC	TEST NO.	CLOCK	INHIBIT	PE	MR	DP _n	CF	OUTPUT
t _r , t _f , t _{PLH} , t _{PHL}	1	PG1	VSS	VSS	VSS	VSS	VSS	Q1
	2	VDD	PG1	VSS	VSS	VSS	VSS	Q1
	3	VSS	VSS	PG1	VSS	PG2	VSS	Q _n
	4	VSS	VSS	VDD	PG1	VDD	VSS	Q _n
	5	VSS	VSS	VDD	VSS	PG1	VSS	Q _n
PW _{MR}	4	VSS	VSS	VDD	PG1	VDD	VSS	Q _n
PW _{PE}	3	VSS	VSS	PG1	VSS	PG2	VSS	Q _n
PW _C	1	PG1	VSS	VSS	VSS	VSS	VSS	Q1
f _{MAX}	1	PG1	VSS	VSS	VSS	VSS	VSS	Q1
t _{HOLD}	3	VSS	VSS	PG1	VSS	PG2	VSS	Q _n
t _r , t _f	6	VSS	VSS	VSS	VDD	VSS	PG1	"0"
t _{PLH} , t _{PHL}	7	PG	VSS	Fig. 1b	VSS	Fig. 1b	VDD	"0"