

MSP430 SoC With RF Core

FEATURES

- True System-on-Chip (SoC) for Low-Power Wireless Communication Applications
- Wide Supply Voltage Range: 1.8 V to 3.6 V
- Ultralow Power Consumption:
 - CPU Active Mode (AM): 160 μ A/MHz
 - Standby Mode (LPM3 RTC Mode): 2.0 μ A
 - Off Mode (LPM4 RAM Retention): 1.0 μ A
 - RTC Only Mode (LPM3.5): 1.0 μ A
 - Shutdown Mode (LPM4.5): 0.3 μ A
 - Radio in RX: 15 mA, 250 kbps, 915 MHz
- MSP430™ System and Peripherals
 - 16-Bit RISC Architecture, Extended Memory, up to 20-MHz System Clock
 - Wake-Up From Standby Mode in Less Than 6 μ s
 - Flexible Power Management System With SVS and Brownout
 - Unified Clock System With FLL
 - 16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers
 - 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
 - Hardware Real-Time Clock
 - Two Universal Serial Communication Interfaces
 - USCI_A0 Supports UART, IrDA, SPI
 - USCI_B0 Supports I²C™, SPI
 - 10-Bit A/D Converter With Internal Reference, Sample-and-Hold, and Autoscan Features (Only CC430F614x and CC430F514x)
 - Comparator
 - Integrated LCD Driver With Contrast Control for up to 96 Segments (Only CC430F614x)
 - 128-Bit AES Security Encryption and Decryption Coprocessor
 - 32-Bit Hardware Multiplier
 - Three-Channel Internal DMA
 - Serial Onboard Programming, No External Programming Voltage Needed
- Embedded Emulation Module (EEM)
- High-Performance Sub-1-GHz RF Transceiver Core
 - Same as in CC1101
 - Wide Supply Voltage Range: 2.0 V to 3.6 V
 - Frequency Bands: 300 MHz to 348 MHz, 389 MHz to 464 MHz, and 779 MHz to 928 MHz
 - Programmable Data Rate From 0.6 kBaud to 500 kBaud
 - High Sensitivity (-117 dBm at 0.6 kBaud, -111 dBm at 1.2 kBaud, 315 MHz, 1% Packet Error Rate)
 - Excellent Receiver Selectivity and Blocking Performance
 - Programmable Output Power Up to +12 dBm for All Supported Frequencies
 - 2-FSK, 2-GFSK, and MSK Supported as well as OOK and Flexible ASK Shaping
 - Flexible Support for Packet-Oriented Systems: On-Chip Support for Sync Word Detection, Address Check, Flexible Packet Length, and Automatic CRC Handling
 - Support for Automatic Clear Channel Assessment (CCA) Before Transmitting (for Listen-Before-Talk Systems)
 - Digital RSSI Output
 - Suited for Systems Targeting Compliance With EN 300 220 (Europe) and FCC CFR Part 15 (US)
 - Suited for Systems Targeting Compliance With Wireless M-Bus Standard EN 13757-4:2005
 - Support for Asynchronous and Synchronous Serial Receive/Transmit Mode for Backward Compatibility With Existing Radio Communication Protocols
- Family Members Summarized in [Table 1](#)
- For Complete Module Descriptions, See the [CC430 Family User's Guide \(SLAU259\)](#)



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DESCRIPTION

The Texas Instruments CC430 family of ultralow-power microcontroller system-on-chip with integrated RF transceiver cores consists of several devices featuring different sets of peripherals targeted for a wide range of applications. The architecture, combined with seven low-power modes (including LPM3.5 and LMP4.5), is optimized to achieve extended battery life in portable measurement applications. The device features the powerful MSP430™ 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The CC430 family provides a tight integration between the microcontroller core, its peripherals, software, and the RF transceiver, making these true system-on-chip solutions easy to use as well as improving performance.

The CC430F614x series are microcontroller system-on-chip configurations combining the excellent performance of the state-of-the-art CC1101 sub-1-GHz RF transceiver with the MSP430 CPUXV2, up to 32 kB of in-system programmable flash memory, up to 4 kB of RAM, two 16-bit timers, a high-performance 10-bit A/D converter with eight external inputs plus internal temperature and battery sensors, comparator, universal serial communication interfaces (USCIs), 128-bit AES security accelerator, hardware multiplier, DMA, real-time clock module with alarm capabilities, LCD driver, and up to 44 I/O pins.

The CC430F514x and CC430F512x series are microcontroller system-on-chip configurations combining the excellent performance of the state-of-the-art CC1101 sub-1-GHz RF transceiver with the MSP430 CPUXV2, up to 32 kB of in-system programmable flash memory, up to 4 kB of RAM, two 16-bit timers, a high performance 10-bit A/D converter with six external inputs plus internal temperature and battery sensors on CC430F514x devices, comparator, universal serial communication interfaces (USCI), 128-bit AES security accelerator, hardware multiplier, DMA, real-time clock module with alarm capabilities, and up to 30 I/O pins.

Typical applications for these devices include wireless analog and digital sensor systems, heat cost allocators, thermostats, metering (AMR, AMI), smart grid wireless networks etc.

Family members available are summarized in [Table 1](#).

For complete module descriptions, see the *CC430 Family User's Guide* ([SLAU259](#)).

Table 1. Family Members

| Device | Program (KB) | SRAM (KB) | Timer_A ⁽¹⁾ | LCD_B ⁽²⁾ | USCI | | ADC10_A ⁽²⁾ | Comp_B | I/O | Package |
|------------|--------------|-----------|------------------------|----------------------|---------------------------------|----------------------------------|------------------------|--------|-----|---------|
| | | | | | Channel A: UART, LIN, IrDA, SPI | Channel B: SPI, I ² C | | | | |
| CC430F6147 | 32 | 4 | 5, 3 | 96 seg | 1 | 1 | 8 ext, 4 int ch. | 8 ch. | 44 | 64 RGC |
| CC430F6145 | 16 | 2 | 5, 3 | 96 seg | 1 | 1 | 8 ext, 4 int ch. | 8 ch. | 44 | 64 RGC |
| CC430F6143 | 8 | 2 | 5, 3 | 96 seg | 1 | 1 | 8 ext, 4 int ch. | 8 ch. | 44 | 64 RGC |
| CC430F5147 | 32 | 4 | 5, 3 | n/a | 1 | 1 | 6 ext, 4 int ch. | 6 ch. | 30 | 48 RGZ |
| CC430F5145 | 16 | 2 | 5, 3 | n/a | 1 | 1 | 6 ext, 4 int ch. | 6 ch. | 30 | 48 RGZ |
| CC430F5143 | 8 | 2 | 5, 3 | n/a | 1 | 1 | 6 ext, 4 int ch. | 6 ch. | 30 | 48 RGZ |
| CC430F5125 | 16 | 2 | 5, 3 | n/a | 1 | 1 | n/a | 6 ch. | 30 | 48 RGZ |
| CC430F5123 | 8 | 2 | 5, 3 | n/a | 1 | 1 | n/a | 6 ch. | 30 | 48 RGZ |

(1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 5, 3 would represent two instantiations of Timer_A, the first instantiation having 5 and the second instantiation having 3 capture compare registers and PWM output generators, respectively.

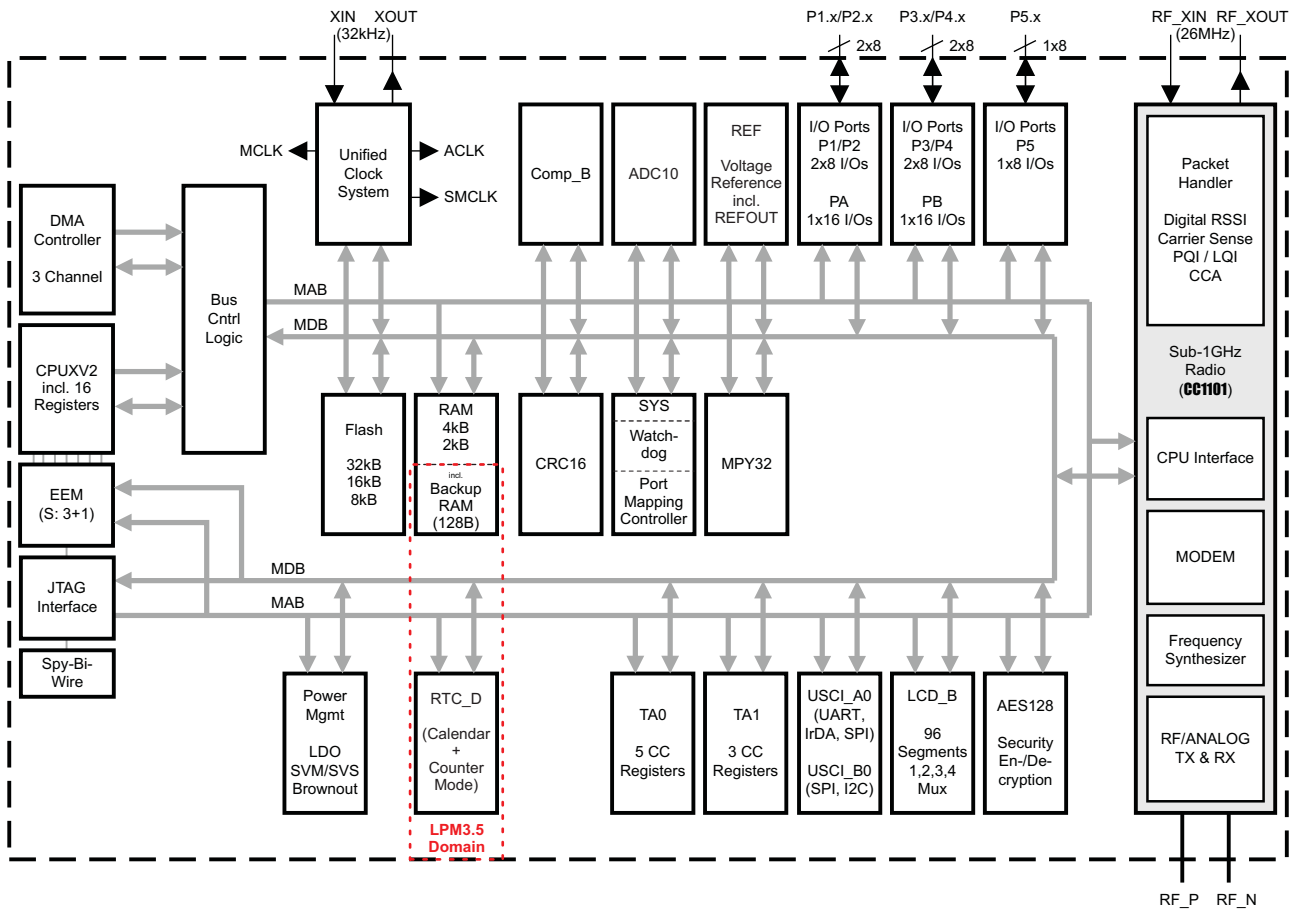
(2) n/a = not available

Table 2. Ordering Information⁽¹⁾

| T _A | PACKAGED DEVICES ⁽²⁾ | |
|----------------|---------------------------------|--------------------------|
| | PLASTIC 64-PIN QFN (RGC) | PLASTIC 48-PIN QFN (RGZ) |
| -40°C to 85°C | CC430F6147IRGC | CC430F5147IRGZ |
| | CC430F6145IRGC | CC430F5145IRGZ |
| | CC430F6143IRGC | CC430F5143IRGZ |
| | | CC430F5125IRGZ |
| | | CC430F5123IRGZ |

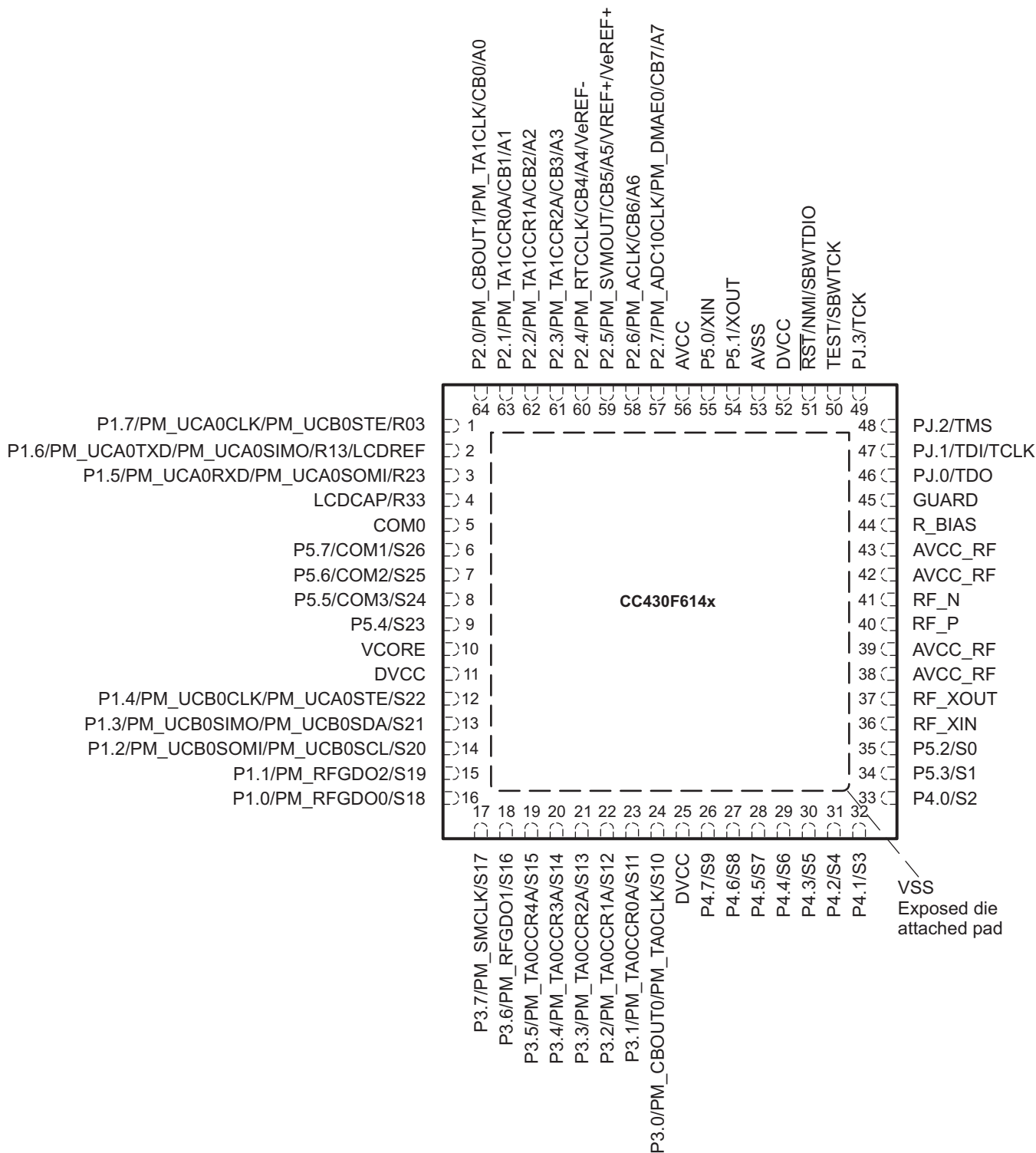
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

CC430F614x Functional Block Diagram



NOTE: Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for ports P1 and P2.

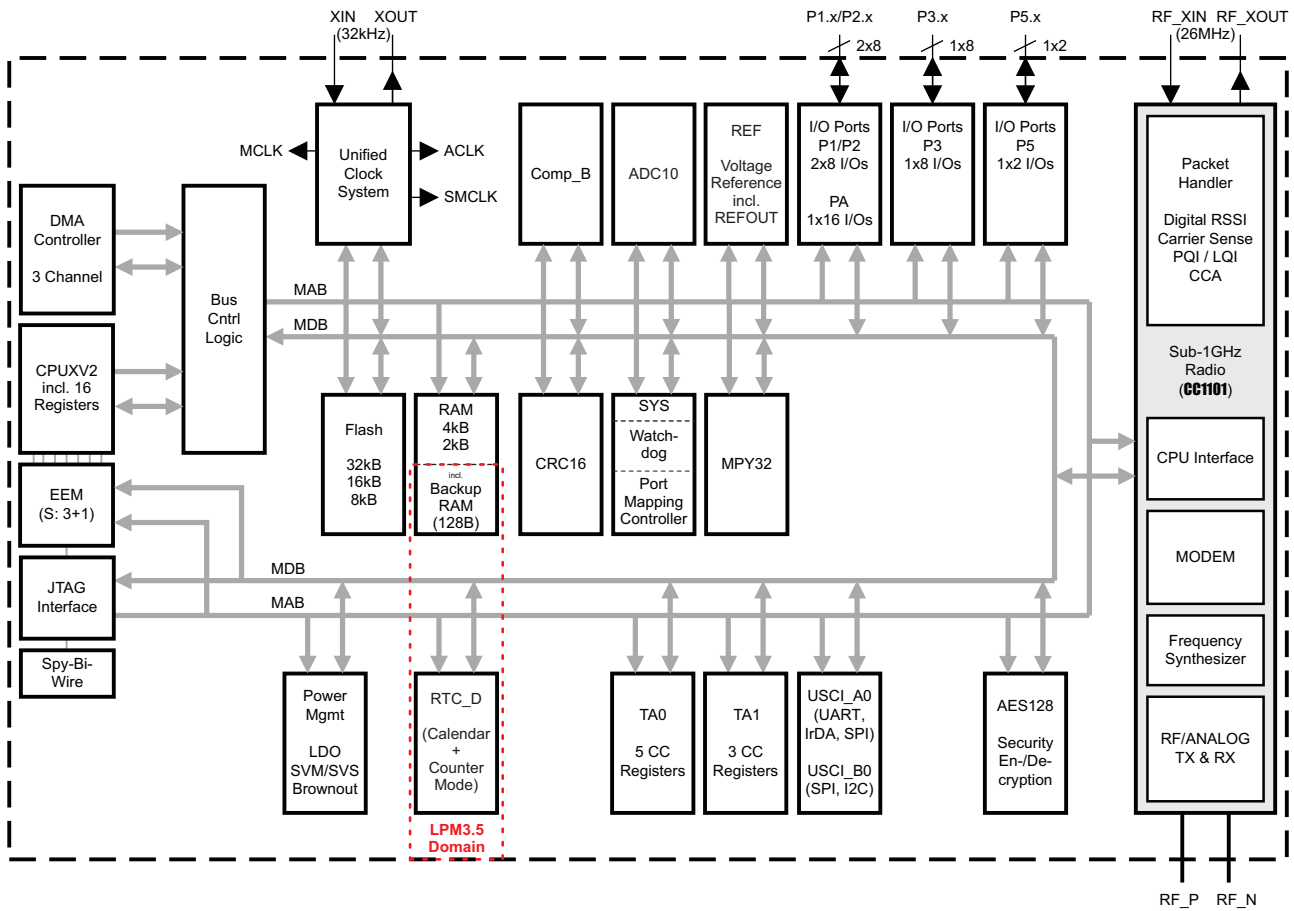
**RGC PACKAGE
(TOP VIEW)**



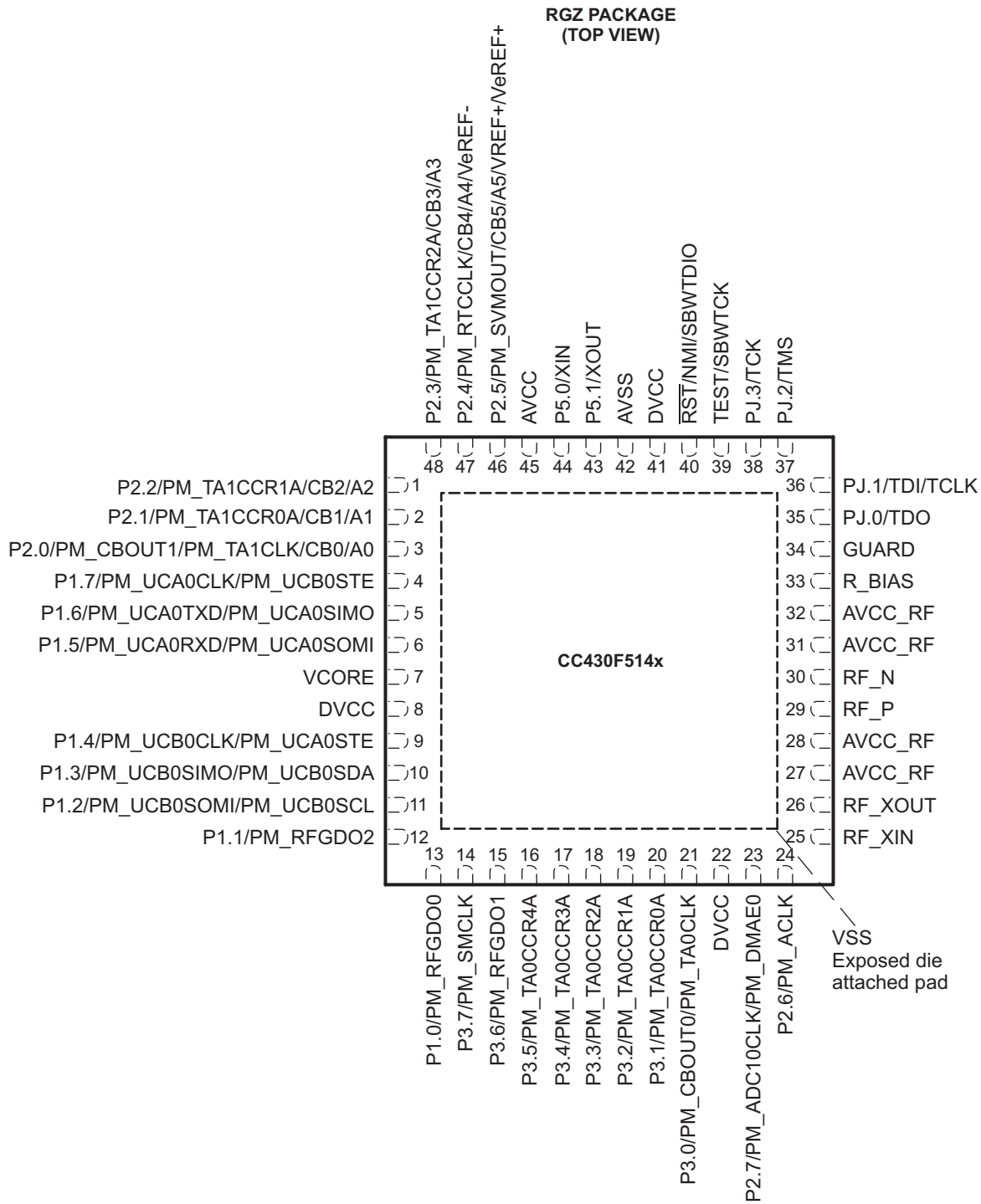
NOTE: The secondary digital functions on ports P1, P2, and P3 are fully mappable. Pinout shows only the default mapping. See [Table 10](#) for details.

CAUTION: LDCAP/R33 must be connected to VSS if not used.

CC430F514x Functional Block Diagram

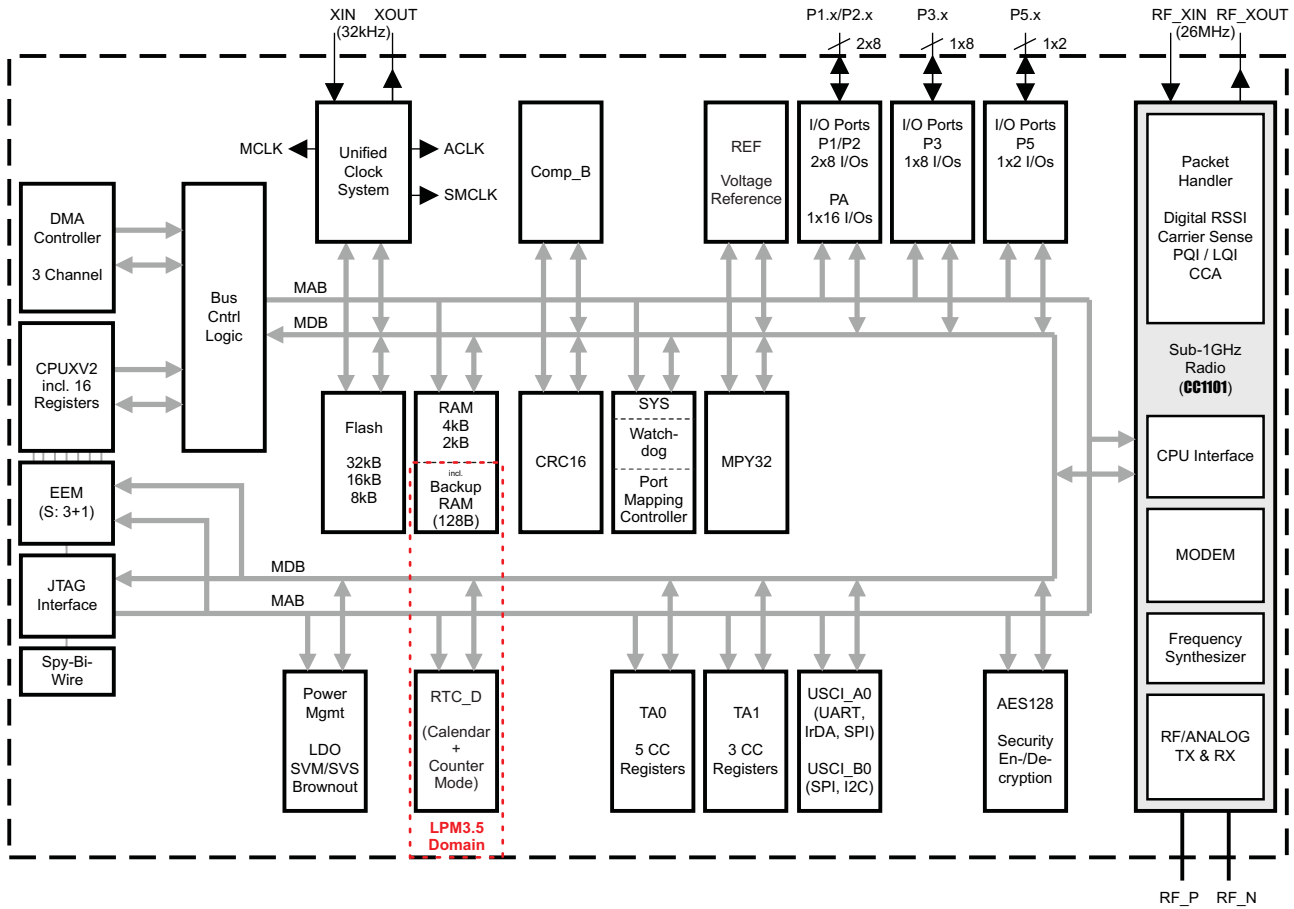


NOTE: Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for ports P1 and P2.



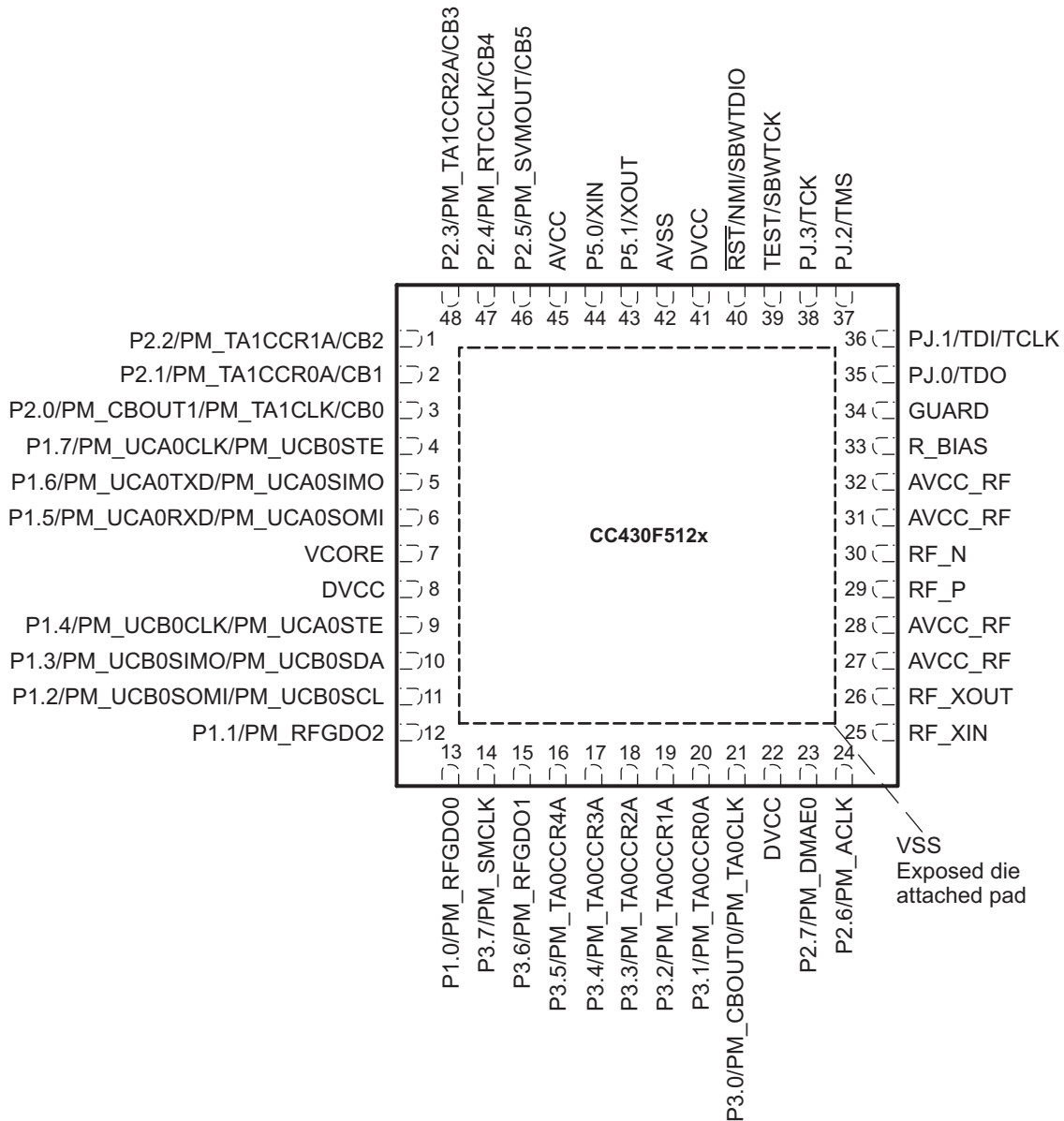
NOTE: The secondary digital functions on ports P1, P2, and P3 are fully mappable. Pinout shows only the default mapping. See [Table 10](#) for details.

CC430F512x Functional Block Diagram



NOTE: Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for ports P1 and P2.

RGZ PACKAGE
(TOP VIEW)



NOTE: The secondary digital functions on ports P1, P2, and P3 are fully mappable. Pinout shows only the default mapping. See [Table 10](#) for details.

Table 3. CC430F614x Terminal Functions

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|---|-----|--------------------|---|
| NAME | NO. | | |
| P1.7/ PM_UCA0CLK/ PM_UCB0STE/ R03 | 1 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 clock input/output; USCI_B0 SPI slave transmit enable Input/output port of lowest analog LCD voltage (V5) |
| P1.6/ PM_UCA0TXD/ PM_UCA0SIMO/ R13/ LCDREF | 2 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 UART transmit data; USCI_A0 SPI slave in master out Input/output port of third most positive analog LCD voltage (V3 or V4) External reference voltage input for regulated LCD voltage |
| P1.5/ PM_UCA0RXD/ PM_UCA0SOMI/ R23 | 3 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 UART receive data; USCI_A0 SPI slave out master in Input/output port of second most positive analog LCD voltage (V2) |
| LCDCAP/ R33 | 4 | I/O | LCD capacitor connection Input/output port of most positive analog LCD voltage (V1) CAUTION: Must be connected to VSS if not used. |
| COM0 | 5 | O | LCD common output COM0 for LCD backplane |
| P5.7/ COM1/ S26 | 6 | I/O | General-purpose digital I/O LCD common output COM1 for LCD backplane LCD segment output S26 |
| P5.6/ COM2/ S25 | 7 | I/O | General-purpose digital I/O LCD common output COM2 for LCD backplane LCD segment output S25 |
| P5.5/ COM3/ S24 | 8 | I/O | General-purpose digital I/O LCD common output COM3 for LCD backplane LCD segment output S24 |
| P5.4/ S23 | 9 | I/O | General-purpose digital I/O LCD segment output S23 |
| VCORE | 10 | | Regulated core power supply |
| DVCC | 11 | | Digital power supply |
| P1.4/ PM_UCB0CLK/ PM_UCA0STE/ S22 | 12 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 clock input/output; USCI_A0 SPI slave transmit enable LCD segment output S22 |
| P1.3/ PM_UCB0SIMO/ PM_UCB0SDA/ S21 | 13 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave in master out; USCI_B0 I2C data LCD segment output S21 |
| P1.2/ PM_UCB0SOMI/ PM_UCB0SCL/ S20 | 14 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave out master in; USCI_B0 I2C clock LCD segment output S20 |
| P1.1/ PM_RFGDO2/ S19 | 15 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Radio GDO2 output LCD segment output S19 |
| P1.0/ PM_RFGDO0/ S18 | 16 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Radio GDO0 output LCD segment output S18 |
| P3.7/ PM_SMCLK/ S17 | 17 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: SMCLK output LCD segment output S17 |
| P3.6/ PM_RFGDO1/ S16 | 18 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: Radio GDO1 output LCD segment output S16 |
| P3.5/ PM_TA0CCR4A/ S15 | 19 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR4 compare output, capture input LCD segment output S15 |
| P3.4/ PM_TA0CCR3A/ S14 | 20 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR3 compare output, capture input LCD segment output S14 |
| P3.3/ PM_TA0CCR2A/ S13 | 21 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR2 compare output, capture input LCD segment output S13 |

(1) I = input, O = output

Table 3. CC430F614x Terminal Functions (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------------------------------|-----|--------------------|---|
| NAME | NO. | | |
| P3.2/ PM_TA0CCR1A/ S12 | 22 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR1 compare output, capture input LCD segment output S12 |
| P3.1/ PM_TA0CCR0A/ S11 | 23 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR0 compare output, capture input LCD segment output S11 |
| P3.0/ PM_CBOU0/ PM_TA0CLK/ S10 | 24 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: Comparator_B output; TA0 clock input LCD segment output S10 |
| DVCC | 25 | | Digital power supply |
| P4.7/ S9 | 26 | I/O | General-purpose digital I/O LCD segment output S9 |
| P4.6/ S8 | 27 | I/O | General-purpose digital I/O LCD segment output S8 |
| P4.5/ S7 | 28 | I/O | General-purpose digital I/O LCD segment output S7 |
| P4.4/ S6 | 29 | I/O | General-purpose digital I/O LCD segment output S6 |
| P4.3/ S5 | 30 | I/O | General-purpose digital I/O LCD segment output S5 |
| P4.2/ S4 | 31 | I/O | General-purpose digital I/O LCD segment output S4 |
| P4.1/ S3 | 32 | I/O | General-purpose digital I/O LCD segment output S3 |
| P4.0/ S2 | 33 | I/O | General-purpose digital I/O LCD segment output S2 |
| P5.3/ S1 | 34 | I/O | General-purpose digital I/O LCD segment output S1 |
| P5.2/ S0 | 35 | I/O | General-purpose digital I/O LCD segment output S0 |
| RF_XIN | 36 | I | Input terminal for RF crystal oscillator or external clock input |
| RF_XOUT | 37 | O | Output terminal for RF crystal oscillator |
| AVCC_RF | 38 | | Radio analog power supply |
| AVCC_RF | 39 | | Radio analog power supply |
| RF_P | 40 | RF I/O | Positive RF input to LNA in receive mode Positive RF output from PA in transmit mode |
| RF_N | 41 | RF I/O | Negative RF input to LNA in receive mode Negative RF output from PA in transmit mode |
| AVCC_RF | 42 | | Radio analog power supply |
| AVCC_RF | 43 | | Radio analog power supply |
| RBIAS | 44 | | External bias resistor for radio reference current |
| GUARD | 45 | | Power supply connection for digital noise isolation |
| PJ.0/ TDO | 46 | I/O | General-purpose digital I/O Test data output port |
| PJ.1/ TDI/ TCLK | 47 | I/O | General-purpose digital I/O Test data input or test clock input |
| PJ.2/ TMS | 48 | I/O | General-purpose digital I/O Test mode select |
| PJ.3/ TCK | 49 | I/O | General-purpose digital I/O Test clock |
| TEST/ SBWTCK | 50 | I | Test mode pin - select digital I/O on JTAG pins Spy-bi-wire input clock |

Table 3. CC430F614x Terminal Functions (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|--|-----|--------------------|--|
| NAME | NO. | | |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | 51 | I/O | Reset input active low Non-maskable interrupt input Spy-bi-wire data input/output |
| DVCC | 52 | | Digital power supply |
| AVSS | 53 | | Analog ground supply for ADC10 |
| P5.1/ XOUT | 54 | I/O | General-purpose digital I/O Output terminal of crystal oscillator XT1 |
| P5.0/ XIN | 55 | I/O | General-purpose digital I/O Input terminal for crystal oscillator XT1 |
| AVCC | 56 | | Analog power supply |
| P2.7/ PM_ADC10CLK/ PM_DMAE0/ CB7 (/A7) | 57 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: ADC10CLK output; DMA external trigger input Comparator_B input CB7 Analog input A7 - 10-bit ADC |
| P2.6/ PM_ACLK/ CB6 (/A6) | 58 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: ACLK output Comparator_B input CB6 Analog input A6 - 10-bit ADC |
| P2.5/ PM_SVMOUT/ CB5 (/A5/ VREF+/ V _{REF+}) | 59 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: SVM output Comparator_B input CB5 Analog input A5 - 10-bit ADC Output of reference voltage to the ADC Positive terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage |
| P2.4/ PM_RTCCLK/ CB4 (/A4/ V _{REF-}) | 60 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: RTCCLK output Comparator_B input CB4 Analog input A4 - 10-bit ADC Negative terminal for the ADC reference voltage for an external applied reference voltage |
| P2.3/ PM_TA1CCR2A/ CB3 (/A3) | 61 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR2 compare output, capture input Comparator_B input CB3 Analog input A3 - 10-bit ADC |
| P2.2/ PM_TA1CCR1A/ CB2 (/A2) | 62 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR1 compare output, capture input Comparator_B input CB2 Analog input A2 - 10-bit ADC |
| P2.1/PM_TA1CCR0A/CB1(/A1) | 63 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR0 compare output, capture input Comparator_B input CB1 Analog input A1 - 10-bit ADC |
| P2.0/ PM_CBOU1/ PM_TA1CLK/ CB0 (/A0) | 64 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Comparator_B output; TA1 clock input Comparator_B input CB0 Analog input A0 - 10-bit ADC |
| VSS - Exposed die attach pad | | | Ground supply The exposed die attach pad must be connected to a solid ground plane as this is the ground connection for the chip. |

Table 4. CC430F514x and CC430F512x Terminal Functions

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|---|-----|--------------------|--|
| NAME | NO. | | |
| P2.2/ PM_TA1CCR1A/ CB2/ (A2) | 1 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR1 compare output, capture input Comparator_B input CB2 Analog input A2 - 10-bit ADC (only CC430F514x) |
| P2.1/ PM_TA1CCR0A/ CB1/ (A1) | 2 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR0 compare output, capture input Comparator_B input CB1 Analog input A1 - 10-bit ADC (only CC430F514x) |
| P2.0/ PM_CBOU1/ PM_TA1CLK/ CB0/ (A0) | 3 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Comparator_B output; TA1 clock input Comparator_B input CB0 Analog input A0 - 10-bit ADC (only CC430F514x) |
| P1.7/ PM_UCA0CLK/ PM_UCA0STE | 4 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 clock input/output; USCI_B0 SPI slave transmit enable |
| P1.6/ PM_UCA0TXD/ PM_UCA0SIMO | 5 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 UART transmit data; USCI_A0 SPI slave in master out |
| P1.5/ PM_UCA0RXD/ PM_UCA0SOMI | 6 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 UART receive data; USCI_A0 SPI slave out master in |
| VCORE | 7 | | Regulated core power supply |
| DVCC | 8 | | Digital power supply |
| P1.4/ PM_UCB0CLK/ PM_UCA0STE | 9 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 clock input/output; USCI_A0 SPI slave transmit enable |
| P1.3/ PM_UCB0SIMO/ PM_UCB0SDA | 10 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave in master out; USCI_B0 I2C data |
| P1.2/ PM_UCB0SOMI/ PM_UCB0SCL | 11 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave out master in; USCI_B0 I2C clock |
| P1.1/ PM_RFGDO2 | 12 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Radio GDO2 output |
| P1.0/ PM_RFGDO0 | 13 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Radio GDO0 output |
| P3.7/ PM_SMCLK | 14 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: SMCLK output |
| P3.6/ PM_RFGDO1 | 15 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: Radio GDO1 output |
| P3.5/ PM_TA0CCR4A | 16 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR4 compare output, capture input |
| P3.4/ PM_TA0CCR3A | 17 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR3 compare output, capture input |
| P3.3/ PM_TA0CCR2A | 18 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR2 compare output, capture input |
| P3.2/ PM_TA0CCR1A | 19 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR1 compare output, capture input |
| P3.1/ PM_TA0CCR0A | 20 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: TA0 CCR0 compare output, capture input |
| P3.0/ PM_CBOU0/ PM_TA0CLK | 21 | I/O | General-purpose digital I/O with mappable secondary function Default mapping: Comparator_B output; TA0 clock input |
| DVCC | 22 | | Digital power supply |
| P2.7/ PM_ADC10CLK/ PM_DMAE0 | 23 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: ADC10CLK output; DMA external trigger input |
| P2.6/ PM_ACLK | 24 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: ACLK output |
| RF_XIN | 25 | I | Input terminal for RF crystal oscillator, or external clock input |
| RF_XOUT | 26 | O | Output terminal for RF crystal oscillator |
| AVCC_RF | 27 | | Radio analog power supply |

(1) I = input, O = output

Table 4. CC430F514x and CC430F512x Terminal Functions (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|--|-----|--------------------|--|
| NAME | NO. | | |
| AVCC_RF | 28 | | Radio analog power supply |
| RF_P | 29 | RF I/O | Positive RF input to LNA in receive mode Positive RF output from PA in transmit mode |
| RF_N | 30 | RF I/O | Negative RF input to LNA in receive mode Negative RF output from PA in transmit mode |
| AVCC_RF | 31 | | Radio analog power supply |
| AVCC_RF | 32 | | Radio analog power supply |
| RBIAS | 33 | | External bias resistor for radio reference current |
| GUARD | 34 | | Power supply connection for digital noise isolation |
| PJ.0/ TDO | 35 | I/O | General-purpose digital I/O Test data output port |
| PJ.1/ TDI/ TCLK | 36 | I/O | General-purpose digital I/O Test data input or test clock input |
| PJ.2/ TMS | 37 | I/O | General-purpose digital I/O Test mode select |
| PJ.3/ TCK | 38 | I/O | General-purpose digital I/O Test clock |
| TEST/ SBWTCK | 39 | I | Test mode pin - select digital I/O on JTAG pins Spy-bi-wire input clock |
| $\overline{\text{RST}}/\text{NMI}/ \text{SBWTDIO}$ | 40 | I/O | Reset input active low Non-maskable interrupt input Spy-bi-wire data input/output |
| DVCC | 41 | | Digital power supply |
| AVSS | 42 | | Analog ground supply for ADC10 |
| P5.1/ XOUT | 43 | I/O | General-purpose digital I/O Output terminal of crystal oscillator XT1 |
| P5.0/ XIN | 44 | I/O | General-purpose digital I/O Input terminal for crystal oscillator XT1 |
| AVCC | 45 | | Analog power supply |
| P2.5/ PM_SVMOUT/ CB5/ (A5/ VREF+/VREF+) | 46 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: SVM output Comparator_B input CB5 Analog input A5 - 10-bit ADC (only CC430F514x) Positive terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage (only CC430F514x) |
| P2.4/ PM_RTCCLK/ CB4/ (A4/ VREF-) | 47 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: RTCCLK output Comparator_B input CB4 Analog input A4 - 10-bit ADC (only CC430F514x) Negative terminal for the ADC reference voltage for an external applied reference voltage (only CC430F514x) |
| P2.3/ PM_TA1CCR2A/ CB3/ (A3) | 48 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: TA1 CCR2 compare output, capture input Comparator_B input CB3 Analog input A3 - 10-bit ADC (only CC430F514x) |
| VSS - Exposed die attach pad | | | Ground supply The exposed die attach pad must be connected to a solid ground plane as this is the ground connection for the chip. |

SHORT-FORM DESCRIPTION

Sub-1-GHz Radio

The implemented sub-1-GHz radio module is based on the industry-leading CC1101, requiring very few external components. [Figure 1](#) shows a high-level block diagram of the implemented radio.

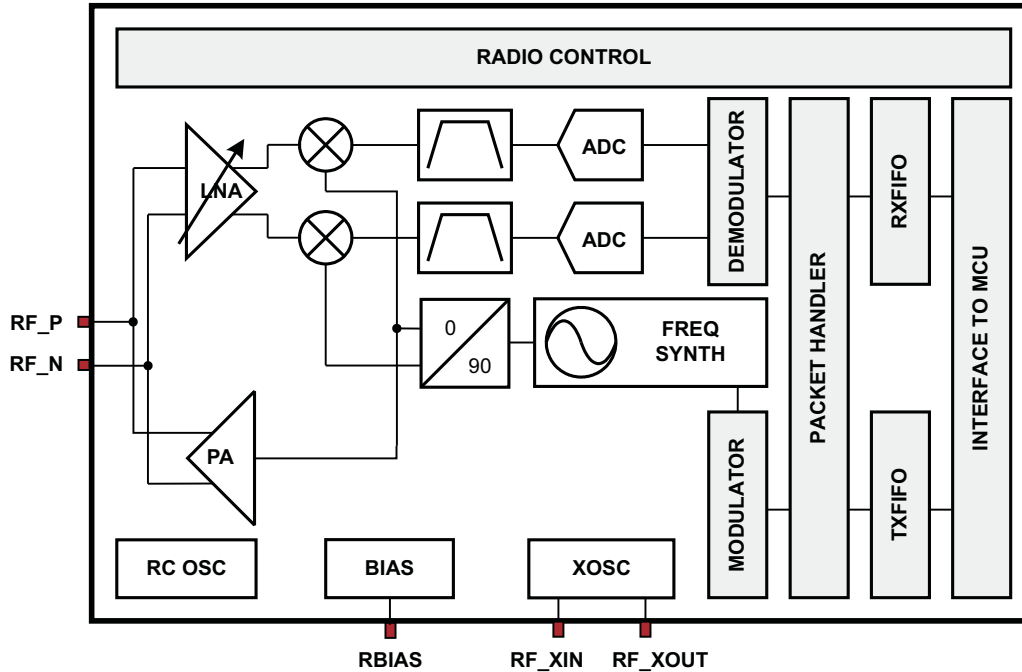


Figure 1. Sub-1 GHz Radio Block Diagram

The radio features a low-IF receiver. The received RF signal is amplified by a low-noise amplifier (LNA) and down-converted in quadrature to the intermediate frequency (IF). At IF, the I/Q signals are digitized. Automatic gain control (AGC), fine channel filtering, demodulation bit and packet synchronization are performed digitally.

The transmitter part is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO and a 90° phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

The 26-MHz crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A memory mapped register interface is used for data access, configuration and status request by the CPU.

The digital baseband includes support for channel configuration, packet handling, and data buffering.

For complete module descriptions, see the *CC430 Family User's Guide* ([SLAU259](#)).

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

Operating Modes

The CC430 has one active mode and seven software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following eight operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
 - FLL loop control remains active
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - FLL loop control is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and FLL loop control and DCOCLK are disabled
 - DCO's dc-generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's dc-generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO's dc-generator is disabled
 - Crystal oscillator is stopped
 - Complete data retention
- Low-power mode 3.5 (LPM3.5)
 - Internal regulator disabled
 - No data retention except Backup RAM and RTC
 - RTC enabled and clocked by low-frequency crystal oscillator XT1
 - Wake up from $\overline{\text{RST}}/\text{NMI}$, RTC, P1, P2
- Low-power mode 4.5 (LPM4.5)
 - Internal regulator disabled
 - No data retention except Backup RAM
 - Wake up from $\overline{\text{RST}}/\text{NMI}$, P1, P2

Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 5. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|--|------------------|--------------|-------------|
| System Reset Power-Up External Reset Watchdog Timeout, Password Violation Flash Memory Password Violation | WDTIFG, KEYV (SYSRSTIV) ⁽¹⁾⁽²⁾ | Reset | 0FFFEh | 63, highest |
| System NMI PMM Vacant Memory Access JTAG Mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) ⁽¹⁾⁽³⁾ | (Non)maskable | 0FFFCh | 62 |
| User NMI NMI Oscillator Fault Flash Memory Access Violation | NMIIFG, OFIFG, ACCVIFG (SYSUNIV) ⁽¹⁾⁽³⁾ | (Non)maskable | 0FFFAh | 61 |
| Comparator_B | Comparator_B Interrupt Flags (CBIV) ⁽¹⁾ | Maskable | 0FFF8h | 60 |
| Watchdog Interval Timer Mode | WDTIFG | Maskable | 0FFF6h | 59 |
| USCI_A0 Receive/Transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV) ⁽¹⁾ | Maskable | 0FFF4h | 58 |
| USCI_B0 Receive/Transmit | UCB0RXIFG, UCB0TXIFG, I2C Status Interrupt Flags (UCB0IV) ⁽¹⁾ | Maskable | 0FFF2h | 57 |
| ADC10_A (Reserved on CC430F512x) | ADC10IFG0, ADC10INIFG, ADC10LOIFG, ADC10HIIFG, ADC10TOVIFG, ADC10OVIFG (ADC10IV) ⁽¹⁾ | Maskable | 0FFF0h | 56 |
| TA0 | TA0CCR0 CCIFG0 | Maskable | 0FFEEh | 55 |
| TA0 | TA0CCR1 CCIFG1 ... TA0CCR4 CCIFG4, TA0IFG (TA0IV) ⁽¹⁾ | Maskable | 0FFEC | 54 |
| RF1A CC1101-based Radio | Radio Interface Interrupt Flags (RF1AIFIV) Radio Core Interrupt Flags (RF1AIV) | Maskable | 0FFEAh | 53 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ⁽¹⁾ | Maskable | 0FFE8h | 52 |
| TA1 | TA1CCR0 CCIFG0 | Maskable | 0FFE6h | 51 |
| TA1 | TA1CCR1 CCIFG1 ... TA1CCR2 CCIFG2, TA1IFG (TA1IV) ⁽¹⁾ | Maskable | 0FFE4h | 50 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) ⁽¹⁾ | Maskable | 0FFE2h | 49 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV) ⁽¹⁾ | Maskable | 0FFE0h | 48 |
| LCD_B (Reserved on CC430F514x and CC430F512x) | LCD_B Interrupt Flags (LCDBIV) ⁽¹⁾ | Maskable | 0FFDEh | 47 |
| RTC_D | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) ⁽¹⁾ | Maskable | 0FFDCh | 46 |
| AES | AESRDYIFG | Maskable | 0FFDAh | 45 |
| Reserved | Reserved ⁽⁴⁾ | | 0FFD8h | 44 |
| | | | : | : |
| | | | 0FF80h | 0, lowest |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space.

(3) (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot disable it.

(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

Memory Organization

Table 6. Memory Organization⁽¹⁾

| | | CC430F6147 CC430F5147 | CC430F6145 CC430F5145 CC430F5125 | CC430F6143 CC430F5143 CC430F5123 |
|---------------------------------------|------------|----------------------------------|---|---|
| Main Memory (flash) | Total Size | 32kB | 16kB | 8kB |
| Main: Interrupt vector | | 00FFFFh-00FF80h | 00FFFFh-00FF80h | 00FFFFh-00FF80h |
| Main: code memory | Bank 0 | 32kB 00FFFFh-008000h | 16kB 00FFFFh-00C000h | 8kB 00FFFFh-00E000h |
| RAM | Total Size | 4kB | 2kB | 2kB |
| | Sect 1 | 2kB 002BFFh-002400h | not available | not available |
| | Sect 0 | 1.875kB 0023FFh-001C80h | 1.875kB 0023FFh-001C80h | 1.875kB 0023FFh-001C80h |
| Backup RAM ⁽²⁾ | | 128B 001C7Fh-001C00h | 128B 001C7Fh-001C00h | 128B 001C7Fh-001C00h |
| Device Descriptor | | 128 B 001AFFh to 001A80h | 128 B 001AFFh to 001A80h | 128 B 001AFFh to 001A80h |
| | | 128 B 001A7Fh to 001A00h | 128 B 001A7Fh to 001A00h | 128 B 001A7Fh to 001A00h |
| Information memory (flash) | Info A | 128 B 0019FFh to 001980h | 128 B 0019FFh to 001980h | 128 B 0019FFh to 001980h |
| | Info B | 128 B 00197Fh to 001900h | 128 B 00197Fh to 001900h | 128 B 00197Fh to 001900h |
| | Info C | 128 B 0018FFh to 001880h | 128 B 0018FFh to 001880h | 128 B 0018FFh to 001880h |
| | Info D | 128 B 00187Fh to 001800h | 128 B 00187Fh to 001800h | 128 B 00187Fh to 001800h |
| Bootstrap loader (BSL) memory (flash) | BSL 3 | 512 B 0017FFh to 001600h | 512 B 0017FFh to 001600h | 512 B 0017FFh to 001600h |
| | BSL 2 | 512 B 0015FFh to 001400h | 512 B 0015FFh to 001400h | 512 B 0015FFh to 001400h |
| | BSL 1 | 512 B 0013FFh to 001200h | 512 B 0013FFh to 001200h | 512 B 0013FFh to 001200h |
| | BSL 0 | 512 B 0011FFh to 001000h | 512 B 0011FFh to 001000h | 512 B 0011FFh to 001000h |
| Peripherals | | 4 KB 000FFFh to 0h | 4 KB 000FFFh to 0h | 4 KB 000FFFh to 0h |

(1) All memory regions not specified here are vacant memory and any access to them causes a Vacant Memory Interrupt.

(2) Content retained in LPM3.5 and LPM4.5.

Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory via the BSL is protected by a user-defined password. BSL entry requires a specific entry sequence on the RST/NMI/SBWDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 7. UART BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|------------------------------------|-----------------------|
| $\overline{\text{RST/NMI/SBWDIO}}$ | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P1.6 | Data transmit |
| P1.5 | Data receive |
| VCC | Power supply |
| VSS | Ground supply |

JTAG Operation

JTAG Standard Interface

The CC430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the RST/NMI/SBWDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 8. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 8. JTAG Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|------------------------------------|-----------|-----------------------------|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{\text{RST/NMI/SBWDIO}}$ | IN | External reset |
| VCC | | Power supply |
| VSS | | Ground supply |

Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the CC430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 9. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 9. Spy-Bi-Wire Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|------------------------------------|-----------|-------------------------------|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST/NMI/SBWDIO}}$ | IN, OUT | Spy-Bi-Wire data input/output |
| VCC | | Power supply |
| VSS | | Ground supply |

Flash Memory

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (Info A to Info D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments Info A to Info D can be erased individually, or as a group with the main memory segments. Segments Info A to Info D are also called *information memory*.
- Segment A can be locked separately.

RAM Memory

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage, however all data is lost. Features of the RAM memory include:

- RAM memory has n sectors of 2k bytes each.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.

Backup RAM

The backup RAM provides 128 bytes of memory that are retained even in LPM3.5 and LPM4.5 when the core is powered down.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *CC430 Family User's Guide* (SLAU259).

Oscillator and System Clock

The Unified Clock System (UCS) module includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The UCS module is designed to meet the requirements of both low system cost and low-power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 5 μ s. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, the internal low-frequency oscillator (VLO), or the trimmed low-frequency oscillator (REFO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/ n , the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

Digital I/O

There are up to five 8-bit I/O ports implemented: ports P1 through P5.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for all the eight bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P5) or word-wise in pairs (PA and PB).

Port Mapping Controller

The port mapping controller allows the flexible and re-configurable mapping of digital functions to port pins of ports P1 through P3.

Table 10. Port Mapping Mnemonics and Functions

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION (PxDIR.y = 0) | OUTPUT PIN FUNCTION (PxDIR.y = 1) |
|-------------------|-----------------|--|--|
| 0 | PM_NONE | None | DVSS |
| 1 ⁽¹⁾ | PM_CBOUT0 | | Comparator_B output (on TA0 clock input) |
| | PM_TA0CLK | TA0 clock input | - |
| 2 ⁽¹⁾ | PM_CBOUT1 | - | Comparator_B output (on TA1 clock input) |
| | PM_TA1CLK | TA1 clock input | - |
| 3 | PM_ACLK | None | ACLK output |
| 4 | PM_MCLK | None | MCLK output |
| 5 | PM_SMCLK | None | SMCLK output |
| 6 | PM_RTCCLK | None | RTCCLK output |
| 7 ⁽¹⁾ | PM_ADC10CLK | - | ADC10CLK output |
| | PM_DMAE0 | DMA external trigger input | - |
| 8 | PM_SVMOUT | None | SVM output |
| 9 | PM_TA0CCR0A | TA0 CCR0 capture input CCI0A | TA0 CCR0 compare output Out0 |
| 10 | PM_TA0CCR1A | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| 11 | PM_TA0CCR2A | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| 12 | PM_TA0CCR3A | TA0 CCR3 capture input CCI3A | TA0 CCR3 compare output Out3 |
| 13 | PM_TA0CCR4A | TA0 CCR4 capture input CCI4A | TA0 CCR4 compare output Out4 |
| 14 | PM_TA1CCR0A | TA1 CCR0 capture input CCI0A | TA1 CCR0 compare output Out0 |
| 15 | PM_TA1CCR1A | TA1 CCR1 capture input CCI1A | TA1 CCR1 compare output Out1 |
| 16 | PM_TA1CCR2A | TA1 CCR2 capture input CCI2A | TA1 CCR2 compare output Out2 |
| 17 ⁽²⁾ | PM_UCA0RXD | USCI_A0 UART RXD (Direction controlled by USCI - input) | |
| | PM_UCA0SOMI | USCI_A0 SPI slave out master in (direction controlled by USCI) | |
| 18 ⁽²⁾ | PM_UCA0TXD | USCI_A0 UART TXD (Direction controlled by USCI - output) | |
| | PM_UCA0SIMO | USCI_A0 SPI slave in master out (direction controlled by USCI) | |
| 19 ⁽³⁾ | PM_UCA0CLK | USCI_A0 clock input/output (direction controlled by USCI) | |
| | PM_UCB0STE | USCI_B0 SPI slave transmit enable (direction controlled by USCI - input) | |
| 20 ⁽⁴⁾ | PM_UCB0SOMI | USCI_B0 SPI slave out master in (direction controlled by USCI) | |
| | PM_UCB0SCL | USCI_B0 I2C clock (open drain and direction controlled by USCI) | |

(1) Input or output function is selected by the corresponding setting in the port direction register PxDIR.

(2) UART or SPI functionality is determined by the selected USCI mode.

(3) UCA0CLK function takes precedence over UCB0STE function. If the mapped pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode even if 4-wire mode is selected.

(4) SPI or I2C functionality is determined by the selected USCI mode. If I2C functionality is selected, the output of the mapped pin drives only the logical 0 to V_{SS} level.

Table 10. Port Mapping Mnemonics and Functions (continued)

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION (PxDIR.y = 0) | OUTPUT PIN FUNCTION (PxDIR.y = 1) |
|--------------------------|-----------------|--|--------------------------------------|
| 21 ⁽⁴⁾ | PM_UCB0SIMO | USCI_B0 SPI slave in master out (direction controlled by USCI) | |
| | PM_UCB0SDA | USCI_B0 I2C data (open drain and direction controlled by USCI) | |
| 22 ⁽⁵⁾ | PM_UCB0CLK | USCI_B0 clock input/output (direction controlled by USCI) | |
| | PM_UCA0STE | USCI_A0 SPI slave transmit enable (direction controlled by USCI - input) | |
| 23 | PM_RFGDO0 | Radio GDO0 (direction controlled by Radio) | |
| 24 | PM_RFGDO1 | Radio GDO1 (direction controlled by Radio) | |
| 25 | PM_RFGDO2 | Radio GDO2 (direction controlled by Radio) | |
| 26 | Reserved | None | DVSS |
| 27 | Reserved | None | DVSS |
| 28 | Reserved | None | DVSS |
| 29 | Reserved | None | DVSS |
| 30 | Reserved | None | DVSS |
| 31 (0FFh) ⁽⁶⁾ | PM_ANALOG | Disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. | |

- (5) UCB0CLK function takes precedence over UCA0STE function. If the mapped pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode even if 4-wire mode is selected.
- (6) The value of the PMPAP_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored resulting in a read out value of 31.

Table 11. Default Mapping

| PIN | PxMAPy MNEMONIC | INPUT PIN FUNCTION (PxDIR.y = 0) | OUTPUT PIN FUNCTION (PxDIR.y = 1) |
|-------------|------------------------|---|--------------------------------------|
| P1.0/P1MAP0 | PM_RFGDO0 | None | Radio GDO0 |
| P1.1/P1MAP1 | PM_RFGDO2 | None | Radio GDO2 |
| P1.2/P1MAP2 | PM_UCB0SOMI/PM_UCB0SCL | USCI_B0 SPI slave out master in (direction controlled by USCI) USCI_B0 I2C clock (open drain and direction controlled by USCI) | |
| P1.3/P1MAP3 | PM_UCB0SIMO/PM_UCB0SDA | USCI_B0 SPI slave in master out (direction controlled by USCI) USCI_B0 I2C data (open drain and direction controlled by USCI) | |
| P1.4/P1MAP4 | PM_UCB0CLK/PM_UCA0STE | USCI_B0 clock input/output (direction controlled by USCI) USCI_A0 SPI slave transmit enable (direction controlled by USCI - input) | |
| P1.5/P1MAP5 | PM_UCA0RXD/PM_UCA0SOMI | USCI_A0 UART RXD (Direction controlled by USCI - input) USCI_A0 SPI slave out master in (direction controlled by USCI) | |
| P1.6/P1MAP6 | PM_UCA0TXD/PM_UCA0SIMO | USCI_A0 UART TXD (Direction controlled by USCI - output) USCI_A0 SPI slave in master out (direction controlled by USCI) | |
| P1.7/P1MAP7 | PM_UCA0CLK/PM_UCB0STE | USCI_A0 clock input/output (direction controlled by USCI) USCI_B0 SPI slave transmit enable (direction controlled by USCI - input) | |
| P2.0/P2MAP0 | PM_CBOU1/PM_TA1CLK | TA1 clock input | Comparator_B output |
| P2.1/P2MAP1 | PM_TA1CCR0A | TA1 CCR0 capture input CCI0A | TA1 CCR0 compare output Out0 |
| P2.2/P2MAP2 | PM_TA1CCR1A | TA1 CCR1 capture input CCI1A | TA1 CCR1 compare output Out1 |
| P2.3/P2MAP3 | PM_TA1CCR2A | TA1 CCR2 capture input CCI2A | TA1 CCR2 compare output Out2 |
| P2.4/P2MAP4 | PM_RTCCCLK | None | RTCCCLK output |
| P2.5/P2MAP5 | PM_SVMOUT | None | SVM output |
| P2.6/P2MAP6 | PM_ACLK | None | ACLK output |
| P2.7/P2MAP7 | PM_ADC10CLK/PM_DMAE0 | DMA external trigger input | ADC10CLK output |
| P3.0/P3MAP0 | PM_CBOU0/PM_TA0CLK | TA0 clock input | Comparator_B output |
| P3.1/P3MAP1 | PM_TA0CCR0A | TA0 CCR0 capture input CCI0A | TA0 CCR0 compare output Out0 |
| P3.2/P3MAP2 | PM_TA0CCR1A | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| P3.3/P3MAP3 | PM_TA0CCR2A | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| P3.4/P3MAP4 | PM_TA0CCR3A | TA0 CCR3 capture input CCI3A | TA0 CCR3 compare output Out3 |
| P3.5/P3MAP5 | PM_TA0CCR4A | TA0 CCR4 capture input CCI4A | TA0 CCR4 compare output Out4 |

Table 11. Default Mapping (continued)

| PIN | PxMAPy MNEMONIC | INPUT PIN FUNCTION (PxDIR.y = 0) | OUTPUT PIN FUNCTION (PxDIR.y = 1) |
|-------------|-----------------|-------------------------------------|--------------------------------------|
| P3.6/P3MAP6 | PM_RFGDO1 | None | Radio GDO1 |
| P3.7/P3MAP7 | PM_SMCLK | None | SMCLK output |

System Module (SYS)

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, boot strap loader entry mechanisms, as well as, configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

Table 12. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY | |
|-------------------------------|------------|-------------------------------------|------------|----------------------|--------|
| SYSRSTIV, System Reset | 019Eh | No interrupt pending | 00h | | |
| | | Brownout (BOR) | 02h | Highest | |
| | | RST/NMI (POR) | 04h | | |
| | | DoBOR (BOR) | 06h | | |
| | | Reserved | 08h | | |
| | | Security violation (BOR) | 0Ah | | |
| | | SVSL (POR) | 0Ch | | |
| | | SVSH (POR) | 0Eh | | |
| | | SVML_OVP (POR) | 10h | | |
| | | SVMH_OVP (POR) | 12h | | |
| | | DoPOR (POR) | 14h | | |
| | | WDT timeout (PUC) | 16h | | |
| | | WDT password violation (PUC) | 18h | | |
| | | KEYV flash password violation (PUC) | 1Ah | | |
| | | Reserved | 1Ch | | |
| | | Peripheral area fetch (PUC) | 1Eh | | |
| | | PMM password violation (PUC) | 20h | | |
| Reserved | 22h to 3Eh | | Lowest | | |
| SYSSNIV, System NMI | 019Ch | No interrupt pending | 00h | | |
| | | SVMLIFG | 02h | Highest | |
| | | SVMHIFG | 04h | | |
| | | DLYLIFG | 06h | | |
| | | DLYHIFG | 08h | | |
| | | VMAIFG | 0Ah | | |
| | | JMBINIFG | 0Ch | | |
| | | JMBOUTIFG | 0Eh | | |
| | | VLRIFG | 10h | | |
| | | VLRHIFG | 12h | | |
| | | Reserved | 14h to 1Eh | | Lowest |
| | | SYSUNIV, User NMI | 019Ah | No interrupt pending | 00h |
| NMIFG | 02h | | | Highest | |
| OFIFG | 04h | | | | |
| ACCVIFG | 06h | | | | |
| Reserved | 08h to 1Eh | | | | Lowest |

DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

Table 13. DMA Trigger Assignments⁽¹⁾

| TRIGGER | CHANNEL | | |
|---------|--------------------------|--------------------------|--------------------------|
| | 0 | 1 | 2 |
| 0 | DMAREQ | DMAREQ | DMAREQ |
| 1 | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2 | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3 | TA1CCR0 CCIFG | TA1CCR0 CCIFG | TA1CCR0 CCIFG |
| 4 | TA1CCR2 CCIFG | TA1CCR2 CCIFG | TA1CCR2 CCIFG |
| 5 | Reserved | Reserved | Reserved |
| 6 | Reserved | Reserved | Reserved |
| 7 | Reserved | Reserved | Reserved |
| 8 | Reserved | Reserved | Reserved |
| 9 | Reserved | Reserved | Reserved |
| 10 | Reserved | Reserved | Reserved |
| 11 | Reserved | Reserved | Reserved |
| 12 | Reserved | Reserved | Reserved |
| 13 | Reserved | Reserved | Reserved |
| 14 | RFRXIFG | RFRXIFG | RFRXIFG |
| 15 | RFTXIFG | RFTXIFG | RFTXIFG |
| 16 | UCA0RXIFG | UCA0RXIFG | UCA0RXIFG |
| 17 | UCA0TXIFG | UCA0TXIFG | UCA0TXIFG |
| 18 | UCB0RXIFG | UCB0RXIFG | UCB0RXIFG |
| 19 | UCB0TXIFG | UCB0TXIFG | UCB0TXIFG |
| 20 | Reserved | Reserved | Reserved |
| 21 | Reserved | Reserved | Reserved |
| 22 | Reserved | Reserved | Reserved |
| 23 | Reserved | Reserved | Reserved |
| 24 | ADC10IFG0 ⁽²⁾ | ADC10IFG0 ⁽²⁾ | ADC10IFG0 ⁽²⁾ |
| 25 | Reserved | Reserved | Reserved |
| 26 | Reserved | Reserved | Reserved |
| 27 | Reserved | Reserved | Reserved |
| 28 | Reserved | Reserved | Reserved |
| 29 | MPY ready | MPY ready | MPY ready |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | DMAE0 | DMAE0 | DMAE0 |

- (1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers will not cause any DMA trigger event when selected.
 (2) Only on CC430F614x and CC430F514x. Reserved on CC430F512x.

Watchdog Timer (WDT_A)

The primary function of the watchdog timer is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the timer can be configured as an interval timer and can generate interrupts at selected time intervals.

CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

AES128 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

Universal Serial Communication Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA.

The USCI_An module provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

The USCI_Bn module provides support for SPI (3 or 4 pin) and I2C.

A USCI_A0 and USCI_B0 module are implemented.

TA0

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing. TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 14. TA0 Signal Connections

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|----------------------------|-------------------|--------------|----------------------|--|
| PM_TA0CLK | TACLK | Timer | NA | |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| RFCLK/192 ⁽¹⁾ | INCLK | | | |
| PM_TA0CCR0A | CCI0A | CCR0 | TA0 | PM_TA0CCR0A |
| DVSS | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | V _{CC} | | | |
| PM_TA0CCR1A | CCI1A | CCR1 | TA1 | PM_TA0CCR1A |
| CBOUT (internal) | CCI1B | | | ADC10 (internal) ⁽²⁾ ADC10SHSx = {1} |
| DVSS | GND | | | |
| DVCC | V _{CC} | | | |
| PM_TA0CCR2A | CCI2A | CCR2 | TA2 | PM_TA0CCR2A |
| ACLK (internal) | CCI2B | | | |
| DVSS | GND | | | |
| DVCC | V _{CC} | | | |
| PM_TA0CCR3A | CCI3A | CCR3 | TA3 | PM_TA0CCR3A |
| GDO1 from radio (internal) | CCI3B | | | |
| DVSS | GND | | | |
| DVCC | V _{CC} | | | |
| PM_TA0CCR4A | CCI4A | CCR4 | TA4 | PM_TA0CCR4A |
| GDO2 from radio (internal) | CCI4B | | | |
| DVSS | GND | | | |
| DVCC | V _{CC} | | | |

(1) If a different RFCLK divider setting is selected for a radio GDO output, this divider setting is also used for the Timer_A INCLK.

(2) Only on CC430F614x and CC430F514x.

TA1

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing. TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 15. TA1 Signal Connections

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|-----------------------------|-------------------|--------------|----------------------|----------------------------|
| | | | | PZ |
| PM_TA1CLK | TACLK | Timer | NA | |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| RFCLK/192 ⁽¹⁾ | INCLK | | | |
| PM_TA1CCR0A | CCI0A | CCR0 | TA0 | PM_TA1CCR0A |
| RF Async. Output (internal) | CCI0B | | | RF Async. Input (internal) |
| DVSS | GND | | | |
| DVCC | V _{CC} | | | |
| PM_TA1CCR1A | CCI1A | CCR1 | TA1 | PM_TA1CCR1A |
| CBOUT (internal) | CCI1B | | | |
| DVSS | GND | | | |
| DVCC | V _{CC} | | | |
| PM_TA1CCR2A | CCI2A | CCR2 | TA2 | PM_TA1CCR2A |
| ACLK (internal) | CCI2B | | | |
| DVSS | GND | | | |
| DVCC | V _{CC} | | | |

(1) If a different RFCLK divider setting is selected for a radio GDO output, this divider setting is also used for the Timer_A INCLK.

Real-Time Clock (RTC_D)

The RTC_D module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_D also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_D also supports flexible alarm functions and offset-calibration hardware.

REF Voltage Reference (Including Output)

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device. These include the ADC10_A, LCD_B, and COMP_B modules.

It can also provide the ADC reference voltages to the VREF+ pin (see the pin schematics).

LCD_B (Only CC430F614x)

The LCD_B driver generates the segment and common signals required to drive a Liquid Crystal Display (LCD). The LCD_B controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, and 4-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage and thus contrast by software. The module also provides an automatic blinking capability for individual segments.

Comparator_B

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

ADC10_A (Only CC430F614x and CC430F514x)

The ADC10_A module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limit allows CPU independent result monitoring with three window comparator interrupt flags.

Embedded Emulation Module (EEM) (S Version)

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The S version of the EEM implemented on all devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

Peripheral File Map
Table 16. Peripherals

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|--|--------------|----------------------|
| Special Functions (see Table 17) | 0100h | 000h-01Fh |
| PMM (see Table 18) | 0120h | 000h-00Fh |
| Flash Control (see Table 19) | 0140h | 000h-00Fh |
| CRC16 (see Table 20) | 0150h | 000h-007h |
| RAM Control (see Table 21) | 0158h | 000h-001h |
| Watchdog (see Table 22) | 015Ch | 000h-001h |
| UCS (see Table 23) | 0160h | 000h-01Fh |
| SYS (see Table 24) | 0180h | 000h-01Fh |
| Shared Reference (see Table 25) | 01B0h | 000h-001h |
| Port Mapping Control (see Table 26) | 01C0h | 000h-007h |
| Port Mapping Port P1 (see Table 27) | 01C8h | 000h-007h |
| Port Mapping Port P2 (see Table 28) | 01D0h | 000h-007h |
| Port Mapping Port P3 (see Table 29) | 01D8h | 000h-007h |
| Port P1, P2 (see Table 30) | 0200h | 000h-01Fh |
| Port P3, P4 (see Table 31) (P4 not available on CC430F514x and CC430F512x) | 0220h | 000h-01Fh |
| Port P5 (see Table 32) | 0240h | 000h-01Fh |
| Port PJ (see Table 33) | 0320h | 000h-01Fh |
| TA0 (see Table 34) | 0340h | 000h-03Fh |
| TA1 (see Table 35) | 0380h | 000h-03Fh |
| RTC_D (see Table 36) | 04A0h | 000h-01Fh |
| 32-Bit Hardware Multiplier (see Table 37) | 04C0h | 000h-02Fh |
| DMA Module Control (see Table 38) | 0500h | 000h-00Fh |
| DMA Channel 0 (see Table 39) | 0510h | 000h-00Fh |
| DMA Channel 1 (see Table 40) | 0520h | 000h-00Fh |
| DMA Channel 2 (see Table 41) | 0530h | 000h-00Fh |
| USCI_A0 (see Table 42) | 05C0h | 000h-01Fh |
| USCI_B0 (see Table 43) | 05E0h | 000h-01Fh |
| ADC10 (see Table 44) (only CC430F614x and CC430F514x) | 0740h | 000h-01Fh |
| Comparator_B (see Table 45) | 08C0h | 000h-00Fh |
| AES Accelerator (see Table 46) | 09C0h | 000h-00Fh |
| LCD_B (see Table 47 , only CC430F614x) | 0A00h | 000h-05Fh |
| Radio Interface (see Table 48) | 0F00h | 000h-03Fh |

Table 17. Special Function Registers (Base Address: 0100h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

Table 18. PMM Registers (Base Address: 0120h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| PMM Control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high side control | SVSMHCTL | 04h |
| SVS low side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM power mode 5 control | PM5CTL0 | 10h |

Table 19. Flash Control Registers (Base Address: 0140h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

Table 20. CRC16 Registers (Base Address: 0150h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

Table 21. RAM Control Registers (Base Address: 0158h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RAM control 0 | RCCTL0 | 00h |

Table 22. Watchdog Registers (Base Address: 015Ch)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL | 00h |

Table 23. UCS Registers (Base Address: 0160h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |
| UCS control 8 | UCSCTL8 | 10h |

Table 24. SYS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------------|-----------|--------|
| System control | SYSCTL | 00h |
| Bootstrap loader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBIO | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus Error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

Table 25. Shared Reference Registers (Base Address: 01B0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL | 00h |

Table 26. Port Mapping Control Registers (Base Address: 01C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|-----------|--------|
| Port mapping key register | PMAPKEYID | 00h |
| Port mapping control register | PMAPCTL | 02h |

Table 27. Port Mapping Port P1 Registers (Base Address: 01C8h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Port P1.0 mapping register | P1MAP0 | 00h |
| Port P1.1 mapping register | P1MAP1 | 01h |
| Port P1.2 mapping register | P1MAP2 | 02h |
| Port P1.3 mapping register | P1MAP3 | 03h |
| Port P1.4 mapping register | P1MAP4 | 04h |
| Port P1.5 mapping register | P1MAP5 | 05h |
| Port P1.6 mapping register | P1MAP6 | 06h |
| Port P1.7 mapping register | P1MAP7 | 07h |

Table 28. Port Mapping Port P2 Registers (Base Address: 01D0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Port P2.0 mapping register | P2MAP0 | 00h |
| Port P2.1 mapping register | P2MAP1 | 01h |
| Port P2.2 mapping register | P2MAP2 | 02h |
| Port P2.3 mapping register | P2MAP3 | 03h |
| Port P2.4 mapping register | P2MAP4 | 04h |
| Port P2.5 mapping register | P2MAP5 | 05h |
| Port P2.6 mapping register | P2MAP6 | 06h |
| Port P2.7 mapping register | P2MAP7 | 07h |

Table 29. Port Mapping Port P3 Registers (Base Address: 01D8h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Port P3.0 mapping register | P3MAP0 | 00h |
| Port P3.1 mapping register | P3MAP1 | 01h |
| Port P3.2 mapping register | P3MAP2 | 02h |
| Port P3.3 mapping register | P3MAP3 | 03h |
| Port P3.4 mapping register | P3MAP4 | 04h |
| Port P3.5 mapping register | P3MAP5 | 05h |
| Port P3.6 mapping register | P3MAP6 | 06h |
| Port P3.7 mapping register | P3MAP7 | 07h |

Table 30. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pullup/pulldown enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |
| Port P1 selection | P1SEL | 0Ah |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pullup/pulldown enable | P2REN | 07h |
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection | P2SEL | 0Bh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

Table 31. Port P3, P4 Registers (Base Address: 0220h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pullup/pulldown enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection | P3SEL | 0Ah |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 pullup/pulldown enable | P4REN | 07h |
| Port P4 drive strength | P4DS | 09h |
| Port P4 selection | P4SEL | 0Bh |

Table 32. Port P5 Registers (Base Address: 0240h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 pullup/pulldown enable | P5REN | 06h |
| Port P5 drive strength | P5DS | 08h |
| Port P5 selection | P5SEL | 0Ah |

Table 33. Port J Registers (Base Address: 0320h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ pullup/pulldown enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |

Table 34. TA0 Registers (Base Address: 0340h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA0 control | TAOCTL | 00h |
| Capture/compare control 0 | TAOCCTL0 | 02h |
| Capture/compare control 1 | TAOCCTL1 | 04h |
| Capture/compare control 2 | TAOCCTL2 | 06h |
| Capture/compare control 3 | TAOCCTL3 | 08h |
| Capture/compare control 4 | TAOCCTL4 | 0Ah |
| TA0 counter register | TAOR | 10h |
| Capture/compare register 0 | TAOCCR0 | 12h |
| Capture/compare register 1 | TAOCCR1 | 14h |
| Capture/compare register 2 | TAOCCR2 | 16h |
| Capture/compare register 3 | TAOCCR3 | 18h |
| Capture/compare register 4 | TAOCCR4 | 1Ah |
| TA0 expansion register 0 | TAOEX0 | 20h |
| TA0 interrupt vector | TAOIV | 2Eh |

Table 35. TA1 Registers (Base Address: 0380h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter register | TA1R | 10h |
| Capture/compare register 0 | TA1CCR0 | 12h |
| Capture/compare register 1 | TA1CCR1 | 14h |
| Capture/compare register 2 | TA1CCR2 | 16h |
| TA1 expansion register 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

Table 36. Real Time Clock Registers (Base Address: 04A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|----------------|--------|
| RTC control 0 | RTCCTL0 | 00h |
| RTC control 1 | RTCCTL1 | 01h |
| RTC control 2 | RTCCTL2 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds/counter register 1 | RTCSEC/RTCNT1 | 10h |
| RTC minutes/counter register 2 | RTCMIN/RTCNT2 | 11h |
| RTC hours/counter register 3 | RTCHOUR/RTCNT3 | 12h |
| RTC day of week/counter register 4 | RTCDOW/RTCNT4 | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year low | RTCYEARL | 16h |
| RTC year high | RTCYEARH | 17h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |

Table 37. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-----------|--------|
| 16-bit operand 1 - multiply | MPY | 00h |
| 16-bit operand 1 - signed multiply | MPYS | 02h |
| 16-bit operand 1 - multiply accumulate | MAC | 04h |
| 16-bit operand 1 - signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension register | SUMEXT | 0Eh |
| 32-bit operand 1 - multiply low word | MPY32L | 10h |
| 32-bit operand 1 - multiply high word | MPY32H | 12h |
| 32-bit operand 1 - signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 - signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 - multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 - multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 - signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 - signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 - low word | OP2L | 20h |
| 32-bit operand 2 - high word | OP2H | 22h |
| 32 × 32 result 0 - least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 - most significant word | RES3 | 2Ah |
| MPY32 control register 0 | MPY32CTL0 | 2Ch |

Table 38. DMA Module Control Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Ah |

Table 39. DMA Channel 0 Registers (Base Address: 0510h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 0 control | DMA0CTL | 00h |
| DMA channel 0 source address low | DMA0SAL | 02h |
| DMA channel 0 source address high | DMA0SAH | 04h |
| DMA channel 0 destination address low | DMA0DAL | 06h |
| DMA channel 0 destination address high | DMA0DAH | 08h |
| DMA channel 0 transfer size | DMA0SZ | 0Ah |

Table 40. DMA Channel 1 Registers (Base Address: 0520h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 1 control | DMA1CTL | 00h |
| DMA channel 1 source address low | DMA1SAL | 02h |
| DMA channel 1 source address high | DMA1SAH | 04h |
| DMA channel 1 destination address low | DMA1DAL | 06h |
| DMA channel 1 destination address high | DMA1DAH | 08h |
| DMA channel 1 transfer size | DMA1SZ | 0Ah |

Table 41. DMA Channel 2 Registers (Base Address: 0530h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 2 control | DMA2CTL | 00h |
| DMA channel 2 source address low | DMA2SAL | 02h |
| DMA channel 2 source address high | DMA2SAH | 04h |
| DMA channel 2 destination address low | DMA2DAL | 06h |
| DMA channel 2 destination address high | DMA2DAH | 08h |
| DMA channel 2 transfer size | DMA2SZ | 0Ah |

Table 42. USCI_A0 Registers (Base Address: 05C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|------------|--------|
| USCI control 1 | UCA0CTL1 | 00h |
| USCI control 0 | UCA0CTL0 | 01h |
| USCI baud rate 0 | UCA0BR0 | 06h |
| USCI baud rate 1 | UCA0BR1 | 07h |
| USCI modulation control | UCA0MCTL | 08h |
| USCI status | UCA0STAT | 0Ah |
| USCI receive buffer | UCA0RXBUF | 0Ch |
| USCI transmit buffer | UCA0TXBUF | 0Eh |
| USCI LIN control | UCA0ABCTL | 10h |
| USCI IrDA transmit control | UCA0IRTCTL | 12h |
| USCI IrDA receive control | UCA0IRRCTL | 13h |
| USCI interrupt enable | UCA0IE | 1Ch |
| USCI interrupt flags | UCA0IFG | 1Dh |
| USCI interrupt vector word | UCA0IV | 1Eh |

Table 43. USCI_B0 Registers (Base Address: 05E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1 | UCB0CTL1 | 00h |
| USCI synchronous control 0 | UCB0CTL0 | 01h |
| USCI synchronous bit rate 0 | UCB0BR0 | 06h |
| USCI synchronous bit rate 1 | UCB0BR1 | 07h |
| USCI synchronous status | UCB0STAT | 0Ah |
| USCI synchronous receive buffer | UCB0RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB0TXBUF | 0Eh |
| USCI I2C own address | UCB0I2COA | 10h |
| USCI I2C slave address | UCB0I2CSA | 12h |
| USCI interrupt enable | UCB0IE | 1Ch |
| USCI interrupt flags | UCB0IFG | 1Dh |
| USCI interrupt vector word | UCB0IV | 1Eh |

Table 44. ADC10_A Registers (Base Address: 0740h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|------------|--------|
| ADC10_A Control register 0 | ADC10CTL0 | 00h |
| ADC10_A Control register 1 | ADC10CTL1 | 02h |
| ADC10_A Control register 2 | ADC10CTL2 | 04h |
| ADC10_A Window Comparator Low Threshold | ADC10LO | 06h |
| ADC10_A Window Comparator High Threshold | ADC10HI | 08h |
| ADC10_A Memory Control Register 0 | ADC10MCTL0 | 0Ah |
| ADC10_A Conversion Memory Register | ADC10MEM0 | 12h |
| ADC10_A Interrupt Enable | ADC10IE | 1Ah |
| ADC10_A Interrupt Flags | ADC10IGH | 1Ch |
| ADC10_A Interrupt Vector Word | ADC10IV | 1Eh |

Table 45. Comparator_B Registers (Base Address: 08C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Comp_B control register 0 | CBCTL0 | 00h |
| Comp_B control register 1 | CBCTL1 | 02h |
| Comp_B control register 2 | CBCTL2 | 04h |
| Comp_B control register 3 | CBCTL3 | 06h |
| Comp_B interrupt register | CBINT | 0Ch |
| Comp_B interrupt vector word | CBIV | 0Eh |

Table 46. AES Accelerator Registers (Base Address: 09C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| AES accelerator control register 0 | AESACTL0 | 00h |
| Reserved | | 02h |
| AES accelerator status register | AESASTAT | 04h |
| AES accelerator key register | AESAKEY | 06h |
| AES accelerator data in register | AESADIN | 008h |
| AES accelerator data out register | AESADOUT | 00Ah |

Table 47. LCD_B Registers (Base Address: 0A00h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|------------|--------|
| LCD_B control register 0 | LCDBCTL0 | 000h |
| LCD_B control register 1 | LCDBCTL1 | 002h |
| LCD_B blinking control register | LCDBBLKCTL | 004h |
| LCD_B memory control register | LCDBMEMCTL | 006h |
| LCD_B voltage control register | LCDBVCTL | 008h |
| LCD_B port control register 0 | LCDBPCTL0 | 00Ah |
| LCD_B port control register 1 | LCDBPCTL1 | 00Ch |
| LCD_B charge pump control register | LCDBCTL0 | 012h |
| LCD_B interrupt vector word | LCDBIV | 01Eh |
| LCD_B memory 1 | LCDM1 | 020h |
| LCD_B memory 2 | LCDM2 | 021h |
| ... | | |
| LCD_B memory 14 | LCDM14 | 02Dh |
| LCD_B blinking memory 1 | LCDBM1 | 040h |
| LCD_B blinking memory 2 | LCDBM2 | 041h |
| ... | | |
| LCD_B blinking memory 14 | LCDBM14 | 04Dh |

Table 48. Radio Interface Registers (Base Address: 0F00h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-------------|--------|
| Radio interface control register 0 | RF1AIFCTL0 | 00h |
| Radio interface control register 1 | RF1AIFCTL1 | 02h |
| Radio interface error flag register | RF1AIFERR | 06h |
| Radio interface error vector word | RF1AIFERRV | 0Ch |
| Radio interface interrupt vector word | RF1AIFIV | 0Eh |
| Radio instruction word register | RF1AINSTRW | 10h |
| Radio instruction word register, 1-byte auto-read | RF1AINSTR1W | 12h |
| Radio instruction word register, 2-byte auto-read | RF1AINSTR2W | 14h |
| Radio data in register | RF1ADINW | 16h |
| Radio status word register | RF1ASTATW | 20h |
| Radio status word register, 1-byte auto-read | RF1ASTAT1W | 22h |
| Radio status word register, 2-byte auto-read | RF1AISTAT2W | 24h |
| Radio data out register | RF1ADOUTW | 28h |
| Radio data out register, 1-byte auto-read | RF1ADOUT1W | 2Ah |
| Radio data out register, 2-byte auto-read | RF1ADOUT2W | 2Ch |
| Radio core signal input register | RF1AIN | 30h |
| Radio core interrupt flag register | RF1AIFG | 32h |
| Radio core interrupt edge select register | RF1AIES | 34h |
| Radio core interrupt enable register | RF1AIE | 36h |
| Radio core interrupt vector word | RF1AIV | 38h |

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | |
|--|---|
| Voltage applied at DVCC and AVCC pins to V _{SS} | -0.3 V to 4.1 V |
| Voltage applied to any pin (excluding V _{CORE} , RF_P, RF_N, and R_BIAS) ⁽²⁾ | -0.3 V to (V _{CC} + 0.3 V), 4.1 V Maximum |
| Voltage applied to V _{CORE} , RF_P, RF_N, and R_BIAS ⁽²⁾ | -0.3 V to 2.0 V |
| Input RF level at pins RF_P and RF_N | 10 dBm |
| Diode current at any device terminal | ±2 mA |
| Storage temperature range ⁽³⁾ , T _{stg} | -55°C to 150°C |
| Maximum junction temperature, T _J | 95°C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS}.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Thermal Packaging Characteristics CC430F51xx

| | | | |
|---|--------------|--------------|--------|
| θ _{JA} Junction-to-ambient thermal resistance, still air | Low-K board | 48 QFN (RGZ) | 98°C/W |
| | High-K board | 48 QFN (RGZ) | 28°C/W |

Thermal Packaging Characteristics CC430F61xx

| | | | |
|---|--------------|--------------|--------|
| θ _{JA} Junction-to-ambient thermal resistance, still air | Low-K board | 64 QFN (RGC) | 83°C/W |
| | High-K board | 64 QFN (RGC) | 26°C/W |

Recommended Operating Conditions

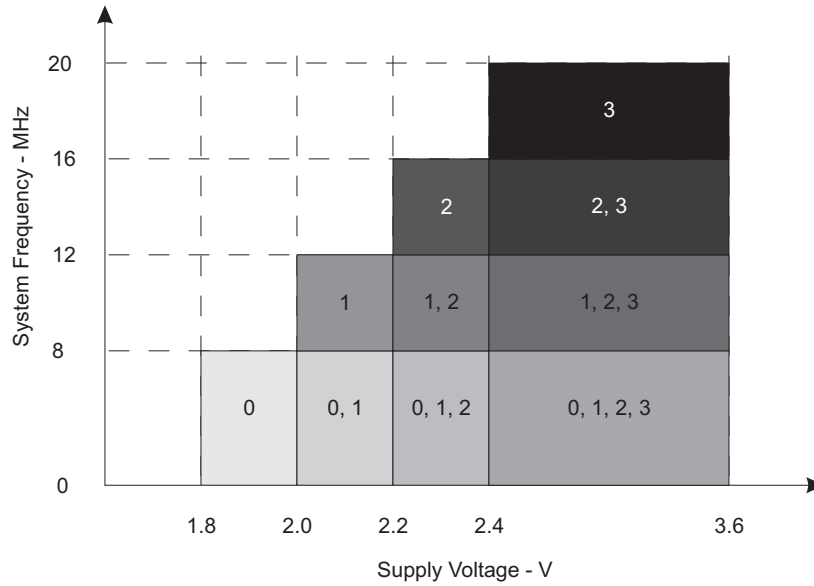
| | | MIN | NOM | MAX | UNIT |
|-------------------------------|--|-----------------------------------|-----|-----|------|
| V _{CC} | Supply voltage range applied at all DVCC and AVCC pins ⁽¹⁾⁽²⁾ during program execution and flash programming with PMM default settings. Radio is not operational with PMMCOREVx = 0, 1. ⁽³⁾ | PMMCOREVx = 0 (default after POR) | 1.8 | 3.6 | V |
| | | PMMCOREVx = 1 | 2.0 | 3.6 | V |
| V _{CC} | Supply voltage range applied at all DVCC and AVCC pins ⁽¹⁾⁽²⁾ during program execution, flash programming and radio operation with PMM default settings. ⁽³⁾ | PMMCOREVx = 2 | 2.2 | 3.6 | V |
| | | PMMCOREVx = 3 | 2.4 | 3.6 | V |
| V _{CC} | Supply voltage range applied at all DVCC and AVCC pins ⁽¹⁾⁽²⁾ during program execution, flash programming and radio operation with PMMCOREVx = 2, high-side SVS level lowered (SVSHRVLx = SVSHRRRLx = 1) or high-side SVS disabled (SVSHE = 0). ⁽⁴⁾⁽³⁾ | 2.0 | 3.6 | V | |
| V _{SS} | Supply voltage applied at the exposed die attach VSS and AVSS pin | | 0 | | V |
| T _A | Operating free-air temperature | -40 | | 85 | °C |
| T _J | Operating junction temperature | -40 | | 85 | °C |
| C _{V_{CORE}} | Recommended capacitor at V _{CORE} | | 470 | | nF |
| C _{V_{CORE}} | Reduced capacitor at V _{CORE} | | 100 | | nF |
| C _{DVCC} | Recommended capacitor at DVCC | | 4.7 | | μF |

- (1) It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
- (2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the [PMM, SVS High Side](#) threshold parameters for the exact values and further details.
- (3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
- (4) Lowering the high-side SVS level or disabling the high-side SVS might cause the LDO to operate out of regulation but the core voltage still stays within its limits and is still supervised by the low-side SVS to ensure reliable operation.

Recommended Operating Conditions (continued)

| | | MIN | NOM | MAX | UNIT | |
|---------------------|--|--|-----|-----|------|-----|
| f _{SYSTEM} | Processor (MCLK) frequency ⁽⁵⁾ (see Figure 2) | PMMCOREVx = 0 (default condition) | | 0 | 8 | MHz |
| | | PMMCOREVx = 1 | | 0 | 12 | MHz |
| | | PMMCOREVx = 2 | | 0 | 16 | MHz |
| | | PMMCOREVx = 3 | | 0 | 20 | MHz |
| P _{INT} | Internal power dissipation | V _{CC} × I _{DVCC} | | | W | |
| P _{IO} | I/O power dissipation of I/O pins powered by DVCC | (V _{CC} - V _{IOH}) × I _{IOH} + V _{IO L} × I _{IO L} | | | W | |
| P _{MAX} | Maximum allowed power dissipation, P _{MAX} > P _{IO} + P _{INT} | (T _J - T _A) / θ _{JA} | | | W | |

(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 2. Maximum System Frequency

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

| PARAMETER | EXECUTION MEMORY | V_{CC} | PMMVCOREVx | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | | | UNIT |
|-----------------------|------------------|----------|------------|--|------|-------|------|--------|------|--------|------|--------|------|------|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 16 MHz | | 20 MHz | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM, Flash}^{(4)}$ | Flash | 3.0 V | 0 | 0.23 | 0.26 | 1.35 | 1.60 | | | | | | | mA |
| | | | 1 | 0.25 | 0.28 | 1.55 | | 2.30 | 2.65 | | | | | |
| | | | 2 | 0.27 | 0.30 | 1.75 | | 2.60 | | 3.45 | 3.90 | | | |
| | | | 3 | 0.28 | 0.32 | 1.85 | | 2.75 | | 3.65 | | 4.55 | 5.10 | |
| $I_{AM, RAM}^{(5)}$ | RAM | 3.0 V | 0 | 0.18 | 0.20 | 0.95 | 1.10 | | | | | | mA | |
| | | | 1 | 0.20 | 0.22 | 1.10 | | 1.60 | 1.85 | | | | | |
| | | | 2 | 0.21 | 0.24 | 1.20 | | 1.80 | | 2.40 | 2.70 | | | |
| | | | 3 | 0.22 | 0.25 | 1.30 | | 1.90 | | 2.50 | | 3.10 | | 3.60 |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Characterized with program executing typical data processing.
 $f_{ACLK} = 32786$ Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
 $XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0$.
- (4) Active mode supply current when program executes in flash at a nominal supply voltage of 3.0 V.
- (5) Active mode supply current when program executes in RAM at a nominal supply voltage of 3.0 V.

Typical Characteristics - Active Mode Supply Currents

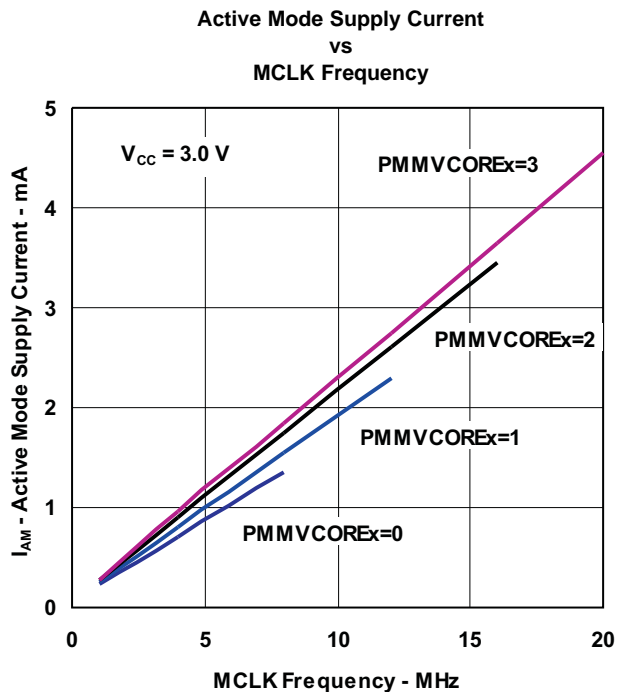


Figure 3.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | V_{CC} | PMMCOREVx | Temperature (T_A) | | | | | | | | UNIT |
|---|----------|-----------|-----------------------|-----|------|-----|------|-----|------|-----|---------|
| | | | -40°C | | 25°C | | 60°C | | 85°C | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ Low-power mode 0 ⁽³⁾⁽⁴⁾ | 2.2 V | 0 | 80 | 100 | 80 | 100 | 80 | 100 | 80 | 100 | μA |
| | 3.0 V | 3 | 90 | 110 | 90 | 110 | 90 | 110 | 90 | 110 | |
| I_{LPM2} Low-power mode 2 ⁽⁵⁾⁽⁴⁾ | 2.2 V | 0 | 6.5 | 11 | 6.5 | 11 | 6.5 | 11 | 6.5 | 11 | μA |
| | 3.0 V | 3 | 7.5 | 12 | 7.5 | 12 | 7.5 | 12 | 7.5 | 12 | |
| $I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode ⁽⁶⁾⁽⁴⁾ | 3.0 V | 0 | 1.8 | | 2.0 | 2.6 | 3.0 | 4.0 | 4.4 | 5.9 | μA |
| | | 1 | 1.9 | | 2.1 | | 3.2 | | 4.8 | | |
| | | 2 | 2.0 | | 2.2 | | 3.4 | | 5.1 | | |
| | | 3 | 2.0 | | 2.2 | 2.9 | 3.5 | 4.8 | 5.3 | 7.4 | |
| $I_{LPM3,VLO,WDT}$ Low-power mode 3, VLO mode, only WDT enabled ⁽⁷⁾⁽⁴⁾ | 3.0 V | 0 | 0.9 | | 1.1 | 2.3 | 2.1 | 3.7 | 3.5 | 5.6 | μA |
| | | 1 | 1.0 | | 1.2 | | 2.3 | | 3.9 | | |
| | | 2 | 1.1 | | 1.3 | | 2.5 | | 4.2 | | |
| | | 3 | 1.1 | | 1.3 | 2.6 | 2.6 | 4.5 | 4.4 | 7.1 | |
| I_{LPM4} Low-power mode 4 ⁽⁸⁾⁽⁴⁾ | 3.0 V | 0 | 0.8 | | 1.0 | 2.2 | 2.0 | 3.6 | 3.4 | 5.5 | μA |
| | | 1 | 0.9 | | 1.1 | | 2.2 | | 3.8 | | |
| | | 2 | 1.0 | | 1.2 | | 2.4 | | 4.1 | | |
| | | 3 | 1.0 | | 1.2 | 2.5 | 2.5 | 4.4 | 4.3 | 7.0 | |
| $I_{LPM3.5}$ Low-power mode 3.5 ⁽⁹⁾ | 2.2 V | n/a | 0.7 | | 0.9 | 1.4 | 1.0 | 1.5 | 1.2 | 1.7 | μA |
| | 3.0 V | n/a | 1.0 | | 1.0 | 1.5 | 1.2 | 1.7 | 1.4 | 1.8 | |
| $I_{LPM4.5}$ Low-power mode 4.5 ⁽¹⁰⁾ | 2.2 V | n/a | 0.2 | | 0.25 | 0.7 | 0.4 | 0.9 | 0.6 | 1.1 | μA |
| | 3.0 V | n/a | 0.3 | | 0.3 | 0.8 | 0.4 | 0.9 | 0.7 | 1.2 | |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
- (4) Current for brownout and high-side supervisor (SVSH) normal mode included. Low-side supervisor (SVSL) and low-side monitor (SVM_L) disabled. High-side monitor disabled (SVM_H). RAM retention enabled.
- (5) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.
- (6) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
- (7) Current for watchdog timer clocked by VLO included. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{VLO} , f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
- (8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
- (9) Internal regulator disabled. No data retention except Backup RAM. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPMx.5), RTC active (Calendar mode) with RTCHOLD = 0 (LPM3.5) and f_{XT1} = 32768 Hz, f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz.
- (10) Internal regulator disabled. No data retention except bBackup RAM. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPMx.5), RTC disabled with RTCHOLD = 1 (LPM4.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz.

Typical Characteristics - Low-Power Mode Supply Currents

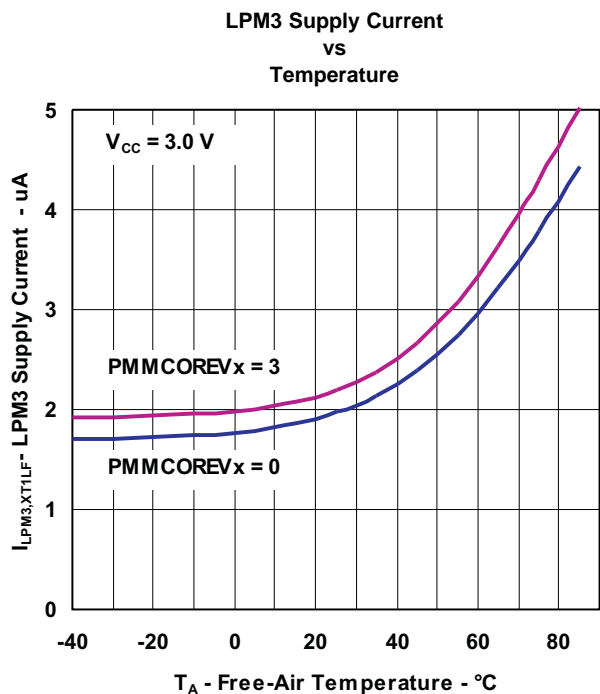


Figure 4.

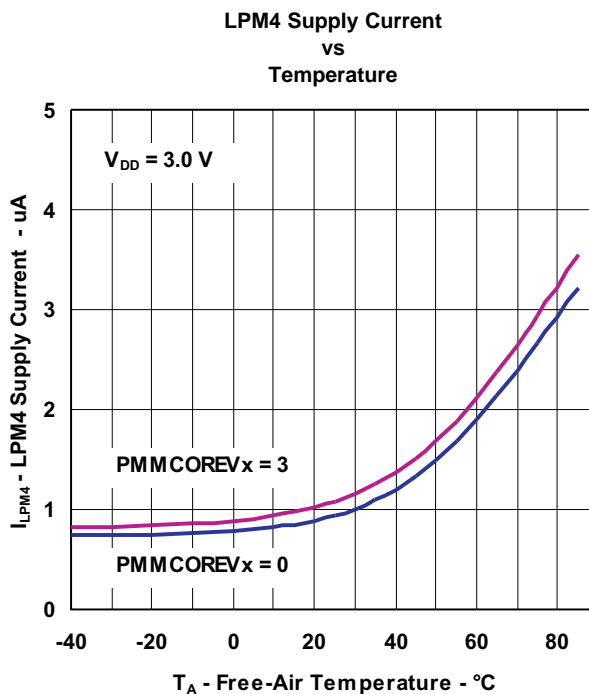


Figure 5.

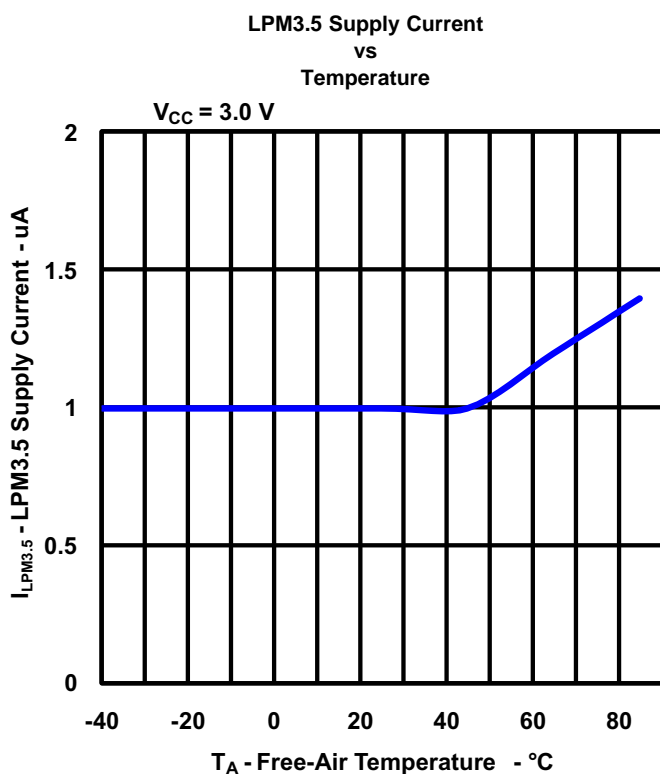


Figure 6.

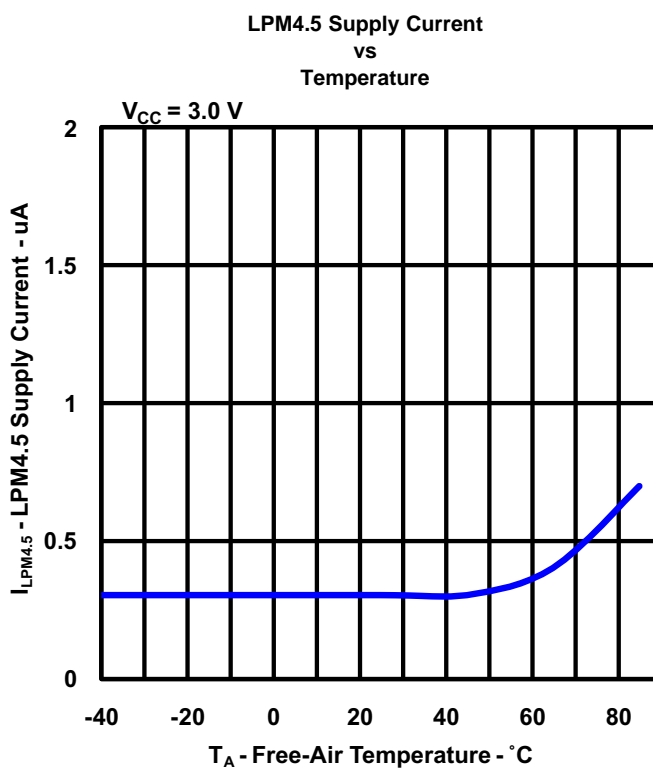


Figure 7.

Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | V_{CC} | PMMCOREVx | Temperature (T_A) | | | | | | | | UNIT |
|---------------------------------|----------|-----------|-----------------------|-----|------|-----|------|---------|---------|-----|------|
| | | | -40°C | | 25°C | | 60°C | | 85°C | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| I_{LPM3} LCD, int. bias | 3.0 V | 0 | 3.1 | 3.3 | 4.0 | 4.3 | 5.8 | 7.4 | μA | | |
| | | 1 | 3.2 | 3.4 | | 4.5 | 6.2 | | | | |
| | | 2 | 3.3 | 3.5 | | 4.7 | 6.5 | | | | |
| | | 3 | 3.3 | 3.5 | 4.3 | 4.8 | 6.7 | 8.9 | | | |
| I_{LPM3} LCD,CP | 2.2 V | 0 | | 4.0 | | | | μA | | | |
| | | 1 | | 4.1 | | | | | | | |
| | | 2 | | 4.2 | | | | | | | |
| | 3.0 V | 0 | | 4.2 | | | | | | | |
| | | 1 | | 4.3 | | | | | | | |
| | | 2 | | 4.5 | | | | | | | |
| | | 3 | | 4.5 | | | | | | | |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
Current for brownout, high-side supervisor (SVSH) normal mode included. Low-side supervisor and monitors disabled (SVSL, SVM_L). High side monitor disabled (SVM_H). RAM retention enabled.
- (4) LCDMx = 11 (4-mux mode), LCDREXT=0, LCDEXTBIAS=0 (internal biasing), LCD2B=0 (1/3 bias), LCDCPEN=0 (charge pump disabled), LCDSSEL=0, LCDPREx=101, LCDDIVx=00011 (f_{LCD} = 32768 Hz/32/4 = 256 Hz)
Even segments S0, S2,...=0, odd segments S1, S3,...=1. No LCD panel load.
- (5) LCDMx = 11 (4-mux mode), LCDREXT=0, LCDEXTBIAS=0 (internal biasing), LCD2B=0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 (V_{LCD} = 3 V typ.), LCDSSEL=0, LCDPREx=101, LCDDIVx=00011 (f_{LCD} = 32768 Hz/32/4 = 256 Hz)
Even segments S0, S2,...=0, odd segments S1, S3,...=1. No LCD panel load.

Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|--|--|-----------------|------|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| V _{IT-} | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} - V _{IT-}) | | 1.8 V | 0.3 | | 0.8 | V |
| | | | 3 V | 0.4 | | 1.0 | |
| R _{Pull} | Pullup/pulldown resistor | For pullup: V _{IN} = V _{SS} . For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _I | Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |
| I _{Ikg(Px.x)} | High-impedance leakage current | ⁽¹⁾⁽²⁾ | | | | ±50 | nA |
| t _(int) | External interrupt timing (external trigger pulse duration to set interrupt flag) ⁽³⁾ | Ports with interrupt capability (see block diagram and terminal function descriptions) | 1.8 V, 3 V | 20 | | | ns |

- (1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
- (2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
- (3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|--|--|--|------------------------|------------------------|------|
| V _{OH} | High-level output voltage, Reduced Drive Strength ⁽¹⁾ | I _(OHmax) = -1 mA, PxDS.y = 0 ⁽²⁾ | 1.8 V | V _{CC} - 0.25 | V _{CC} | V |
| V _{OH} | High-level output voltage, Reduced Drive Strength ⁽¹⁾ | I _(OHmax) = -3 mA, PxDS.y = 0 ⁽³⁾ | 1.8 V | V _{CC} - 0.60 | V _{CC} | V |
| V _{OH} | High-level output voltage, Reduced Drive Strength ⁽¹⁾ | I _(OHmax) = -2 mA, PxDS.y = 0 ⁽²⁾ | 3.0 V | V _{CC} - 0.25 | V _{CC} | V |
| V _{OH} | High-level output voltage, Reduced Drive Strength ⁽¹⁾ | I _(OHmax) = -6 mA, PxDS.y = 0 ⁽³⁾ | 3.0 V | V _{CC} - 0.60 | V _{CC} | V |
| V _{OL} | Low-level output voltage, Reduced Drive Strength ⁽¹⁾ | I _(OLmax) = 1 mA, PxDS.y = 0 ⁽²⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| V _{OL} | Low-level output voltage, Reduced Drive Strength ⁽¹⁾ | I _(OLmax) = 3 mA, PxDS.y = 0 ⁽³⁾ | 1.8 V | V _{SS} | V _{SS} + 0.60 | V |
| V _{OL} | Low-level output voltage, Reduced Drive Strength ⁽¹⁾ | I _(OLmax) = 2 mA, PxDS.y = 0 ⁽²⁾ | 3.0 V | V _{SS} | V _{SS} + 0.25 | V |
| V _{OL} | Low-level output voltage, Reduced Drive Strength ⁽¹⁾ | I _(OLmax) = 6 mA, PxDS.y = 0 ⁽³⁾ | 3.0 V | V _{SS} | V _{SS} + 0.60 | V |
| V _{OH} | High-level output voltage, Full Drive Strength | I _(OHmax) = -3 mA, PxDS.y = 1 ⁽²⁾ | 1.8 V | V _{CC} - 0.25 | V _{CC} | V |
| V _{OH} | High-level output voltage, Full Drive Strength | I _(OHmax) = -10 mA, PxDS.y = 1 ⁽³⁾ | 1.8 V | V _{CC} - 0.60 | V _{CC} | V |
| V _{OH} | High-level output voltage, Full Drive Strength | I _(OHmax) = -5 mA, PxDS.y = 1 ⁽²⁾ | 3 V | V _{CC} - 0.25 | V _{CC} | V |
| V _{OH} | High-level output voltage, Full Drive Strength | I _(OHmax) = -15 mA, PxDS.y = 1 ⁽³⁾ | 3 V | V _{CC} - 0.60 | V _{CC} | V |
| V _{OL} | Low-level output voltage, Full Drive Strength | I _(OLmax) = 3 mA, PxDS.y = 1 ⁽²⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| V _{OL} | Low-level output voltage, Full Drive Strength | I _(OLmax) = 10 mA, PxDS.y = 1 ⁽³⁾ | 1.8 V | V _{SS} | V _{SS} + 0.60 | V |
| V _{OL} | Low-level output voltage, Full Drive Strength | I _(OLmax) = 5 mA, PxDS.y = 1 ⁽²⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | V |
| V _{OL} | Low-level output voltage, Full Drive Strength | I _(OLmax) = 15 mA, PxDS.y = 1 ⁽³⁾ | 3 V | V _{SS} | V _{SS} + 0.60 | V |
| f _{Px,y} | Port output frequency (with load) | C _L = 20 pF, R _L ⁽⁴⁾⁽⁵⁾ | V _{CC} = 1.8 V, PMMCOREVx = 0 | | 16 | MHz |
| | | | V _{CC} = 3 V, PMMCOREVx = 2 | | 25 | |
| f _{Port_CLK} | Clock output frequency | C _L = 20 pF ⁽⁵⁾ | V _{CC} = 1.8 V, PMMCOREVx = 0 | | 16 | MHz |
| | | | V _{CC} = 3 V, PMMCOREVx = 2 | | 25 | |

- (1) Selecting reduced drive strength may reduce EMI.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (3) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
- (4) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
- (5) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics - Outputs, Reduced Drive Strength (PxDS.y = 0)

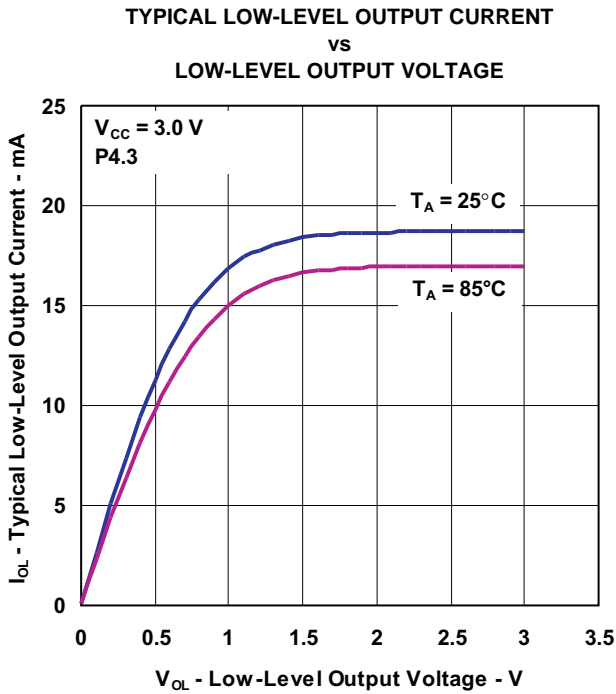


Figure 8.

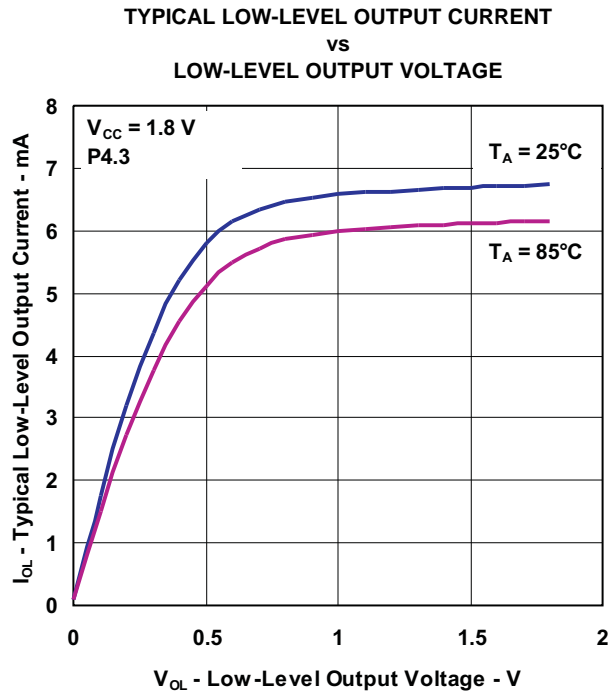


Figure 9.

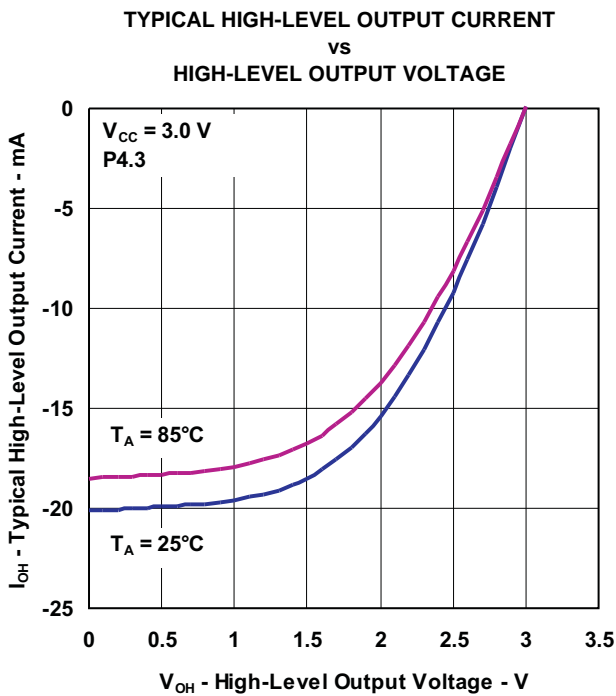


Figure 10.

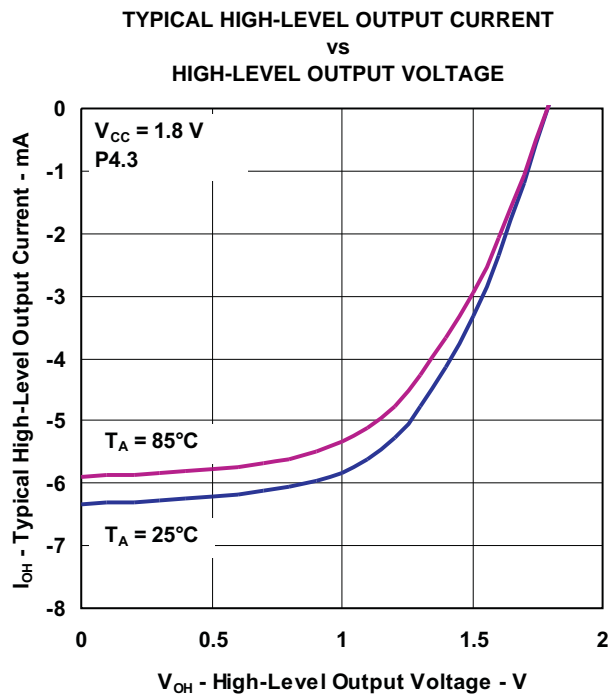


Figure 11.

Typical Characteristics - Outputs, Full Drive Strength (PxDS.y = 1)

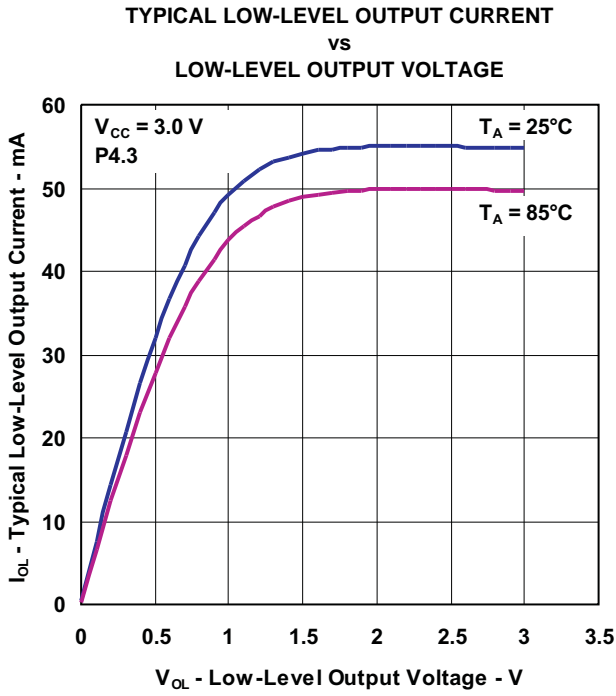


Figure 12.

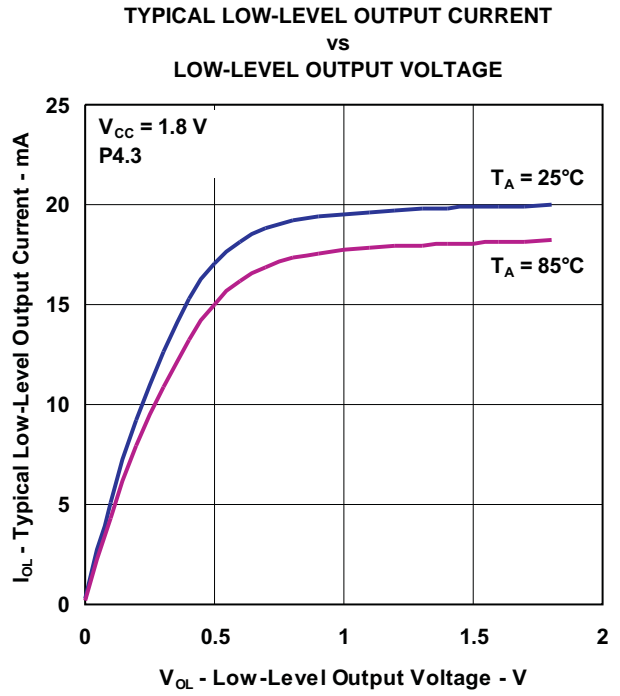


Figure 13.

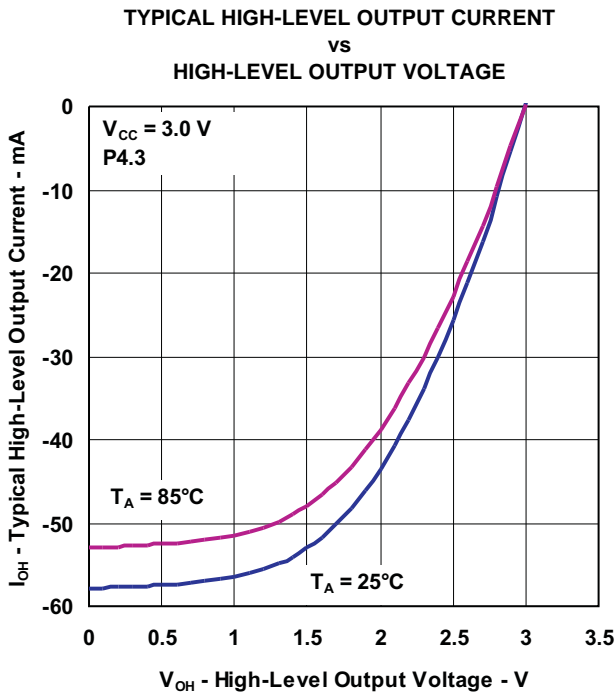


Figure 14.

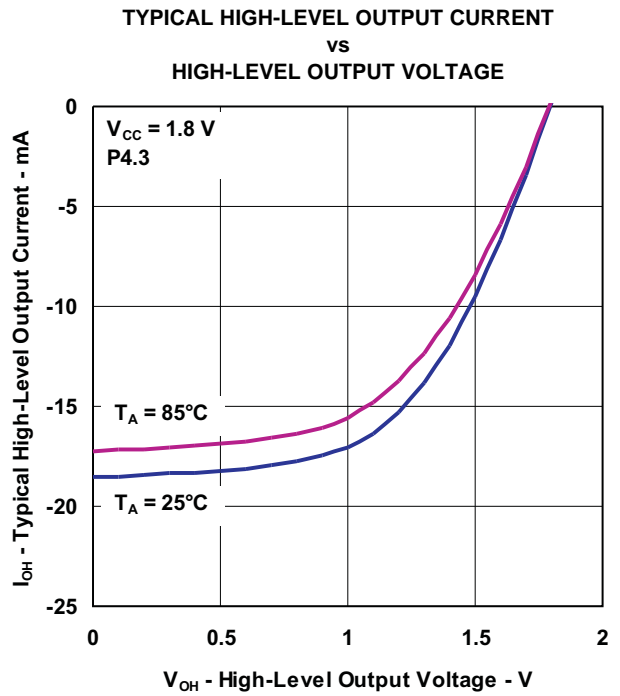


Figure 15.

Crystal Oscillator, XT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------------|-----|--------|-------|------|
| $\Delta I_{DVCC,LF}$ Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C | 3 V | | 0.075 | | μA |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C | | | 0.170 | | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C | | | 0.290 | | |
| $f_{XT1,LF0}$ XT1 oscillator crystal frequency, LF mode | XTS = 0, XT1BYPASS = 0 | | | 32768 | | Hz |
| $f_{XT1,LF,SW}$ XT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, XT1BYPASS = 1 ⁽²⁾⁽³⁾ | | 10 | 32.768 | 50 | kHz |
| O _{ALF} Oscillation allowance for LF crystals ⁽⁴⁾ | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 6 pF | | | 210 | | kΩ |
| | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 12 pF | | | 300 | | |
| C _{L,eff} Integrated effective load capacitance, LF mode ⁽⁵⁾ | XTS = 0, XCAP _x = 0 ⁽⁶⁾ | | | 2 | | pF |
| | XTS = 0, XCAP _x = 1 | | | 5.5 | | |
| | XTS = 0, XCAP _x = 2 | | | 8.5 | | |
| | XTS = 0, XCAP _x = 3 | | | 12.0 | | |
| Duty cycle, LF mode | XTS = 0, Measured at ACLK, $f_{XT1,LF} = 32768$ Hz | | 30 | | 70 | % |
| $f_{Fault,LF}$ Oscillator fault frequency, LF mode ⁽⁷⁾ | XTS = 0 ⁽⁸⁾ | | 10 | | 10000 | Hz |
| $t_{START,LF}$ Startup time, LF mode | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 6 pF | 3 V | | 1000 | | ms |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C, C _{L,eff} = 12 pF | | | 500 | | |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - (a) Keep the trace between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE_x settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - (a) For XT1DRIVE_x = 0, C_{L,eff} ≤ 6 pF
 - (b) For XT1DRIVE_x = 1, 6 pF ≤ C_{L,eff} ≤ 9 pF
 - (c) For XT1DRIVE_x = 2, 6 pF ≤ C_{L,eff} ≤ 10 pF
 - (d) For XT1DRIVE_x = 3, C_{L,eff} ≥ 6 pF
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.4 | 14 | kHz |
| df _{VLO} /dT | VLO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 4 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40 | 50 | 60 | % |

(1) Calculated using the box method: (MAX(-40 to 85°C) - MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C - (-40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) - MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V - 1.8 V)

Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------------------|-------------------------------------|---------------------------------|-----------------|-----|-------|------|------|
| I _{REFO} | REFO oscillator current consumption | T _A = 25°C | 1.8 V to 3.6 V | | 3 | | μA |
| f _{REFO} | REFO frequency calibrated | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance calibrated | Full temperature range | 1.8 V to 3.6 V | | | ±3.5 | % |
| | REFO absolute tolerance calibrated | T _A = 25°C | 3 V | | | ±1.5 | % |
| df _{REFO} /dT | REFO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| df _{REFO} /dV _{CC} | REFO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 1.0 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40 | 50 | 60 | % |
| t _{START} | REFO startup time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | μs |

(1) Calculated using the box method: (MAX(-40 to 85°C) - MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C - (-40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) - MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V - 1.8 V)

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--------------------|--|--|------|------|-------|------|
| $f_{DCO(0,0)}$ | DCO frequency (0, 0) | DCORSELx = 0, DCOx = 0, MODx = 0 | 0.07 | 0.20 | MHz | |
| $f_{DCO(0,31)}$ | DCO frequency (0, 31) | DCORSELx = 0, DCOx = 31, MODx = 0 | 0.70 | 1.70 | MHz | |
| $f_{DCO(1,0)}$ | DCO frequency (1, 0) | DCORSELx = 1, DCOx = 0, MODx = 0 | 0.15 | 0.36 | MHz | |
| $f_{DCO(1,31)}$ | DCO frequency (1, 31) | DCORSELx = 1, DCOx = 31, MODx = 0 | 1.47 | 3.45 | MHz | |
| $f_{DCO(2,0)}$ | DCO frequency (2, 0) | DCORSELx = 2, DCOx = 0, MODx = 0 | 0.32 | 0.75 | MHz | |
| $f_{DCO(2,31)}$ | DCO frequency (2, 31) | DCORSELx = 2, DCOx = 31, MODx = 0 | 3.17 | 7.38 | MHz | |
| $f_{DCO(3,0)}$ | DCO frequency (3, 0) | DCORSELx = 3, DCOx = 0, MODx = 0 | 0.64 | 1.51 | MHz | |
| $f_{DCO(3,31)}$ | DCO frequency (3, 31) | DCORSELx = 3, DCOx = 31, MODx = 0 | 6.07 | 14.0 | MHz | |
| $f_{DCO(4,0)}$ | DCO frequency (4, 0) | DCORSELx = 4, DCOx = 0, MODx = 0 | 1.3 | 3.2 | MHz | |
| $f_{DCO(4,31)}$ | DCO frequency (4, 31) | DCORSELx = 4, DCOx = 31, MODx = 0 | 12.3 | 28.2 | MHz | |
| $f_{DCO(5,0)}$ | DCO frequency (5, 0) | DCORSELx = 5, DCOx = 0, MODx = 0 | 2.5 | 6.0 | MHz | |
| $f_{DCO(5,31)}$ | DCO frequency (5, 31) | DCORSELx = 5, DCOx = 31, MODx = 0 | 23.7 | 54.1 | MHz | |
| $f_{DCO(6,0)}$ | DCO frequency (6, 0) | DCORSELx = 6, DCOx = 0, MODx = 0 | 4.6 | 10.7 | MHz | |
| $f_{DCO(6,31)}$ | DCO frequency (6, 31) | DCORSELx = 6, DCOx = 31, MODx = 0 | 39.0 | 88.0 | MHz | |
| $f_{DCO(7,0)}$ | DCO frequency (7, 0) | DCORSELx = 7, DCOx = 0, MODx = 0 | 8.5 | 19.6 | MHz | |
| $f_{DCO(7,31)}$ | DCO frequency (7, 31) | DCORSELx = 7, DCOx = 31, MODx = 0 | 60 | 135 | MHz | |
| $S_{DCORSEL}$ | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{RSEL} = f_{DCO(DCORSEL+1,DCO)} / f_{DCO(DCORSEL,DCO)}$ | 1.2 | 2.3 | ratio | |
| S_{DCO} | Frequency step between tap DCO and DCO + 1 | $S_{DCO} = f_{DCO(DCORSEL,DCO+1)} / f_{DCO(DCORSEL,DCO)}$ | 1.02 | 1.12 | ratio | |
| | Duty cycle | Measured at SMCLK | 40 | 50 | 60 | % |
| df_{DCO}/dT | DCO frequency temperature drift | $f_{DCO} = 1$ MHz | | 0.1 | | %/°C |
| df_{DCO}/dV_{CC} | DCO frequency voltage drift | $f_{DCO} = 1$ MHz | | 1.9 | | %/V |

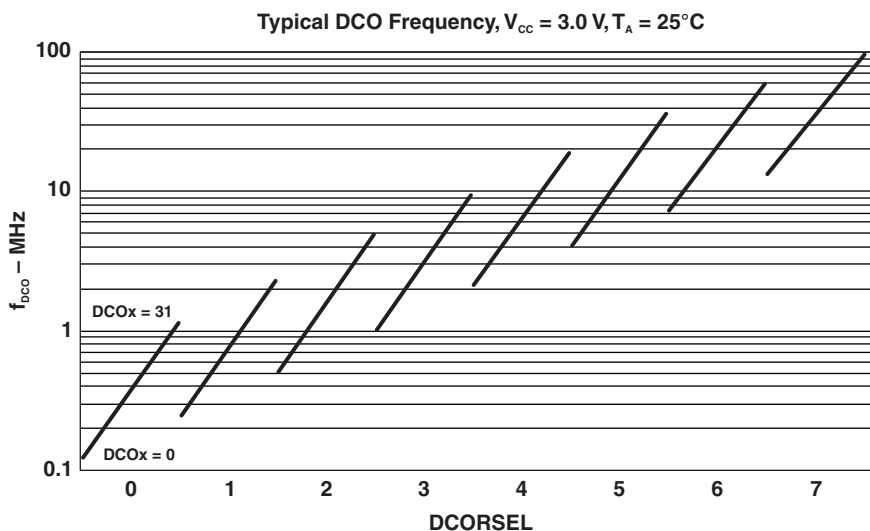


Figure 16. Typical DCO frequency

PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---|---------------------------------|------|------|------|------|
| V(DV _{CC} _BOR_IT-) | BOR _H on voltage, DV _{CC} falling level | dDV _{CC} /dt < 3 V/s | | | 1.45 | V |
| V(DV _{CC} _BOR_IT+) | BOR _H off voltage, DV _{CC} rising level | dDV _{CC} /dt < 3 V/s | 0.80 | 1.30 | 1.50 | V |
| V(DV _{CC} _BOR_hys) | BOR _H hysteresis | | 60 | | 250 | mV |
| t _{RESET} | Pulse duration required at $\overline{\text{RST}}$ /NMI pin to accept a reset | | 2 | | | μs |

PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--|----------------------------------|-----|------|-----|------|
| V _{CORE3} (AM) | Core voltage, active mode, PMMCOREV = 3 | 2.4 V ≤ DV _{CC} ≤ 3.6 V | | 1.90 | | V |
| V _{CORE2} (AM) | Core voltage, active mode, PMMCOREV = 2 | 2.2 V ≤ DV _{CC} ≤ 3.6 V | | 1.80 | | V |
| V _{CORE1} (AM) | Core voltage, active mode, PMMCOREV = 1 | 2.0 V ≤ DV _{CC} ≤ 3.6 V | | 1.60 | | V |
| V _{CORE0} (AM) | Core voltage, active mode, PMMCOREV = 0 | 1.8 V ≤ DV _{CC} ≤ 3.6 V | | 1.40 | | V |
| V _{CORE3} (LPM) | Core voltage, low-current mode, PMMCOREV = 3 | 2.4 V ≤ DV _{CC} ≤ 3.6 V | | 1.93 | | V |
| V _{CORE2} (LPM) | Core voltage, low-current mode, PMMCOREV = 2 | 2.2 V ≤ DV _{CC} ≤ 3.6 V | | 1.90 | | V |
| V _{CORE1} (LPM) | Core voltage, low-current mode, PMMCOREV = 1 | 2.0 V ≤ DV _{CC} ≤ 3.6 V | | 1.70 | | V |
| V _{CORE0} (LPM) | Core voltage, low-current mode, PMMCOREV = 0 | 1.8 V ≤ DV _{CC} ≤ 3.6 V | | 1.50 | | V |

PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|--|------|------|------|------|
| $I_{(SVSH)}$ | SVS current consumption | SVSHE = 0, DV _{CC} = 3.6 V | | 0 | | nA |
| | | SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 0 | | 200 | | nA |
| | | SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 1 | | 1.5 | | μA |
| $V_{(SVSH_IT-)}$ | SVS _H on voltage level ⁽¹⁾ | SVSHE = 1, SVSHRVL = 0 | 1.55 | 1.62 | 1.69 | V |
| | | SVSHE = 1, SVSHRVL = 1 | 1.75 | 1.82 | 1.89 | |
| | | SVSHE = 1, SVSHRVL = 2 | 1.95 | 2.02 | 2.09 | |
| | | SVSHE = 1, SVSHRVL = 3 | 2.05 | 2.12 | 2.19 | |
| $V_{(SVSH_IT+)}$ | SVS _H off voltage level ⁽¹⁾ | SVSHE = 1, SVSMHRRRL = 0 | 1.60 | 1.70 | 1.80 | V |
| | | SVSHE = 1, SVSMHRRRL = 1 | 1.80 | 1.90 | 2.00 | |
| | | SVSHE = 1, SVSMHRRRL = 2 | 2.00 | 2.10 | 2.20 | |
| | | SVSHE = 1, SVSMHRRRL = 3 | 2.10 | 2.20 | 2.30 | |
| | | SVSHE = 1, SVSMHRRRL = 4 | 2.25 | 2.35 | 2.50 | |
| | | SVSHE = 1, SVSMHRRRL = 5 | 2.52 | 2.65 | 2.78 | |
| | | SVSHE = 1, SVSMHRRRL = 6 | 2.85 | 3.00 | 3.15 | |
| | | SVSHE = 1, SVSMHRRRL = 7 | 2.85 | 3.00 | 3.15 | |
| $t_{pd(SVSH)}$ | SVS _H propagation delay | SVSHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVSHFP = 1 | | 2.5 | | μs |
| | | SVSHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVSHFP = 0 | | 20 | | |
| $t_{(SVSH)}$ | SVS _H on or off delay time | SVSHE = 0 → 1, dV _{DVCC} /dt = 10 mV/μs, SVSHFP = 1 | | 12.5 | | μs |
| | | SVSHE = 0 → 1, dV _{DVCC} /dt = 1 mV/μs, SVSHFP = 0 | | 100 | | |
| dV _{DVCC} /dt | DV _{CC} rise time | | 0 | | 1000 | V/s |

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *CC430 Family User's Guide (SLAU259)* on recommended settings and use.

PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---|--|------|------|------|------|
| $I_{(SVMH)}$ | SVM _H current consumption | SVMHE = 0, DV _{CC} = 3.6 V | | 0 | | nA |
| | | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 0 | | 200 | | nA |
| | | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 1 | | 1.5 | | μA |
| $V_{(SVMH)}$ | SVM _H on or off voltage level ⁽¹⁾ | SVMHE = 1, SVSMHRRRL = 0 | 1.60 | 1.70 | 1.80 | V |
| | | SVMHE = 1, SVSMHRRRL = 1 | 1.80 | 1.90 | 2.00 | |
| | | SVMHE = 1, SVSMHRRRL = 2 | 2.00 | 2.10 | 2.20 | |
| | | SVMHE = 1, SVSMHRRRL = 3 | 2.10 | 2.20 | 2.30 | |
| | | SVMHE = 1, SVSMHRRRL = 4 | 2.25 | 2.35 | 2.50 | |
| | | SVMHE = 1, SVSMHRRRL = 5 | 2.52 | 2.65 | 2.78 | |
| | | SVMHE = 1, SVSMHRRRL = 6 | 2.85 | 3.00 | 3.15 | |
| | | SVMHE = 1, SVSMHRRRL = 7 | 2.85 | 3.00 | 3.15 | |
| | | SVMHE = 1, SVMHOVPE = 1 | | 3.75 | | |
| $t_{pd(SVMH)}$ | SVM _H propagation delay | SVMHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1 | | 2.5 | | μs |
| | | SVMHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0 | | 20 | | |
| $t_{(SVMH)}$ | SVM _H on or off delay time | SVMHE = 0 → 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1 | | 12.5 | | μs |
| | | SVMHE = 0 → 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0 | | 100 | | |

(1) The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *CC430 Family User's Guide (SLAU259)* on recommended settings and use.

PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------------|--|-----|------|-----|------|
| $I_{(SVSL)}$ | SVS _L current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0 | | 200 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1 | | 1.5 | | μA |
| $t_{pd(SVSL)}$ | SVS _L propagation delay | SVSLE = 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1 | | 2.5 | | μs |
| | | SVSLE = 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0 | | 20 | | |
| $t_{(SVSL)}$ | SVS _L on or off delay time | SVSLE = 0 → 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1 | | 12.5 | | μs |
| | | SVSLE = 0 → 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0 | | 100 | | |

PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------------------|--|-----|------|-----|------|
| $I_{(SVM_L)}$ | SVM _L current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 0 | | 200 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 1 | | 1.5 | | μA |
| $t_{pd(SVM_L)}$ | SVM _L propagation delay | SVMLE = 1, dV _{CORE} /dt = 10 mV/μs, SVMLFP = 1 | | 2.5 | | μs |
| | | SVMLE = 1, dV _{CORE} /dt = 1 mV/μs, SVMLFP = 0 | | 20 | | |
| $t_{(SVM_L)}$ | SVM _L on or off delay time | SVMLE = 0 → 1, dV _{CORE} /dt = 10 mV/μs, SVMLFP = 1 | | 12.5 | | μs |
| | | SVMLE = 0 → 1, dV _{CORE} /dt = 1 mV/μs, SVMLFP = 0 | | 100 | | |

Wake-up From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|--|-----|-----|-----|------|
| $t_{WAKE-UP-FAST}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽¹⁾ | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1 | | | 5 | μs |
| | | $f_{MCLK} \geq 4.0$ MHz | | | 6 | |
| $t_{WAKE-UP-SLOW}$ | Wake-up time from LPM2, LPM3 or LPM4 to active mode ⁽²⁾ | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | 150 | 165 | μs |
| $t_{WAKE-UP-LPM5}$ | Wake-up time from LPMx.5 to active mode ⁽³⁾ | | | 2 | 3 | ms |
| $t_{WAKE-UP-RESET}$ | Wake-up time from \overline{RST} or BOR event to active mode ⁽³⁾ | | | 2 | 3 | ms |

(1) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low-side supervisor (SVS_L) and low side monitor (SVM_L). Fastest wakeup times are possible with SVS_L and SVM_L in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *CC430 Family User's Guide (SLAU259)*.

(2) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low-side supervisor (SVS_L) and low side monitor (SVM_L). In this case, the SVS_L and SVM_L are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *CC430 Family User's Guide (SLAU259)*.

(3) This value represents the time from the wakeup event to the reset vector execution.

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------|-------------------------------|--|-----------------|-----|-----|-----|------|
| f_{TA} | Timer_A input clock frequency | Internal: SMCLK, ACLK, External: TACLK, Duty cycle = 50% ± 10% | 1.8 V, 3.0 V | | | 25 | MHz |
| $t_{TA,cap}$ | Timer_A capture timing | All capture inputs, minimum pulse duration required for capture | 1.8 V, 3.0 V | 20 | | | ns |

USCI (UART Mode) Recommended Operating Conditions

| PARAMETER | | CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---|---|-----------------|-----|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10% | | | | f _{SYSTEM} | MHz |
| f _{BITCLK} | BITCLK clock frequency (equals baud rate in MBaud) | | | | | 1 | MHz |

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|---|-----------------|-----------------|-----|-----|-----|------|
| t _r | UART receive deglitch time ⁽¹⁾ | | 2.2 V | 50 | | 600 | ns |
| | | | 3 V | 50 | | 600 | |

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode) Recommended Operating Conditions

| PARAMETER | | CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|----------------------------|---|-----------------|-----|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK, ACLK Duty cycle = 50% ± 10% | | | | f _{SYSTEM} | MHz |

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ [Figure 17](#) [Figure 18](#)

| PARAMETER | | TEST CONDITIONS | PMM COREV _x | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|--|------------------------|-----------------|-----|-----|-----|------|
| t _{SU,MI} | SOMI input data setup time | | 0 | 1.8 V | 55 | | | ns |
| | | | | 3.0 V | 38 | | | |
| | | | 3 | 2.4 V | 30 | | | ns |
| | | | | 3.0 V | 25 | | | |
| t _{HD,MI} | SOMI input data hold time | | 0 | 1.8 V | 0 | | | ns |
| | | | | 3.0 V | 0 | | | |
| | | | 3 | 2.4 V | 0 | | | ns |
| | | | | 3.0 V | 0 | | | |
| t _{VALID,MO} | SIMO output data valid time ⁽²⁾ | UCLK edge to SIMO valid, C _L = 20 pF | 0 | 1.8 V | | | 20 | ns |
| | | | | 3.0 V | | | 18 | |
| | | | 3 | 2.4 V | | | 16 | ns |
| | | | | 3.0 V | | | 15 | |
| t _{HD,MO} | SIMO output data hold time ⁽³⁾ | C _L = 20 pF | 0 | 1.8 V | -10 | | | ns |
| | | | | 3.0 V | -8 | | | |
| | | | 3 | 2.4 V | -10 | | | ns |
| | | | | 3.0 V | -8 | | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave))$.
For the slave's parameters $t_{SU,SI}(Slave)$ and $t_{VALID,SO}(Slave)$ see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 17](#) and [Figure 18](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 17](#) and [Figure 18](#).

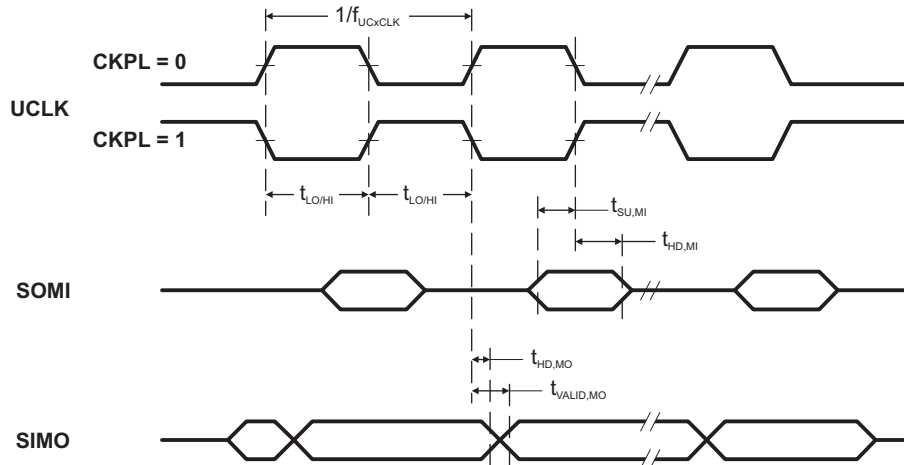


Figure 17. SPI Master Mode, CKPH = 0

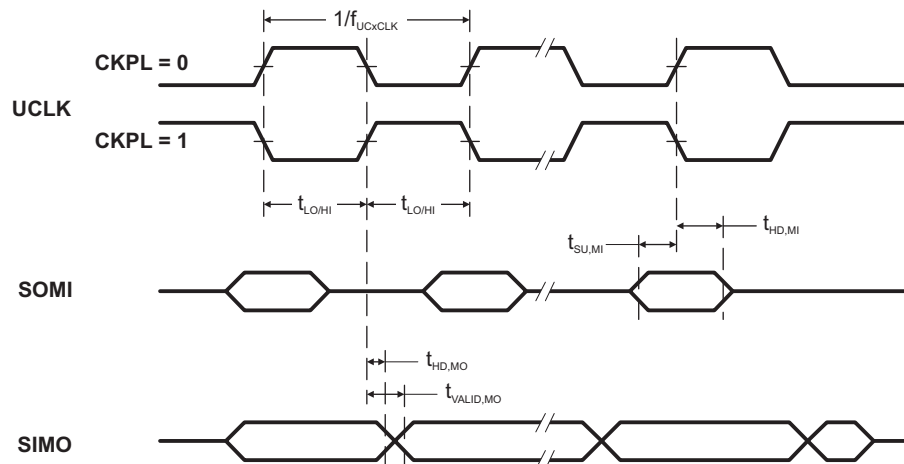


Figure 18. SPI Master Mode, CKPH = 1

USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ [Figure 19](#) [Figure 20](#)

| PARAMETER | | TEST CONDITIONS | PMM COREV _x | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|---------------------------|-----------------|-----|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE low to clock | | 0 | 1.8 V | 11 | | | ns |
| | | | | 3.0 V | 8 | | | |
| | | | 3 | 2.4 V | 7 | | | |
| | | | | 3.0 V | 6 | | | |
| t _{STE,LAG} | STE lag time, Last clock to STE high | | 0 | 1.8 V | 3 | | | ns |
| | | | | 3.0 V | 3 | | | |
| | | | 3 | 2.4 V | 3 | | | |
| | | | | 3.0 V | 3 | | | |
| t _{STE,ACC} | STE access time, STE low to SOMI data out | | 0 | 1.8 V | | | 66 | ns |
| | | | | 3.0 V | | | 50 | |
| | | | 3 | 2.4 V | | | 36 | |
| | | | | 3.0 V | | | 30 | |
| t _{STE,DIS} | STE disable time, STE high to SOMI high impedance | | 0 | 1.8 V | | | 30 | ns |
| | | | | 3.0 V | | | 23 | |
| | | | 3 | 2.4 V | | | 16 | |
| | | | | 3.0 V | | | 13 | |
| t _{SU,SI} | SIMO input data setup time | | 0 | 1.8 V | 5 | | | ns |
| | | | | 3.0 V | 5 | | | |
| | | | 3 | 2.4 V | 2 | | | |
| | | | | 3.0 V | 2 | | | |
| t _{HD,SI} | SIMO input data hold time | | 0 | 1.8 V | 5 | | | ns |
| | | | | 3.0 V | 5 | | | |
| | | | 3 | 2.4 V | 5 | | | |
| | | | | 3.0 V | 5 | | | |
| t _{VALID,SO} | SOMI output data valid time ⁽²⁾ | UCLK edge to SOMI valid, C _L = 20 pF | 0 | 1.8 V | | | 76 | ns |
| | | | | 3.0 V | | | 60 | |
| | | | 3 | 2.4 V | | | 44 | |
| | | | | 3.0 V | | | 40 | |
| t _{HD,SO} | SOMI output data hold time ⁽³⁾ | C _L = 20 pF | 0 | 1.8 V | 18 | | | ns |
| | | | | 3.0 V | 12 | | | |
| | | | 3 | 2.4 V | 10 | | | |
| | | | | 3.0 V | 8 | | | |

(1) $f_{UCXCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.

For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached master.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 17](#) and [Figure 18](#).

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 17](#) and [Figure 18](#).

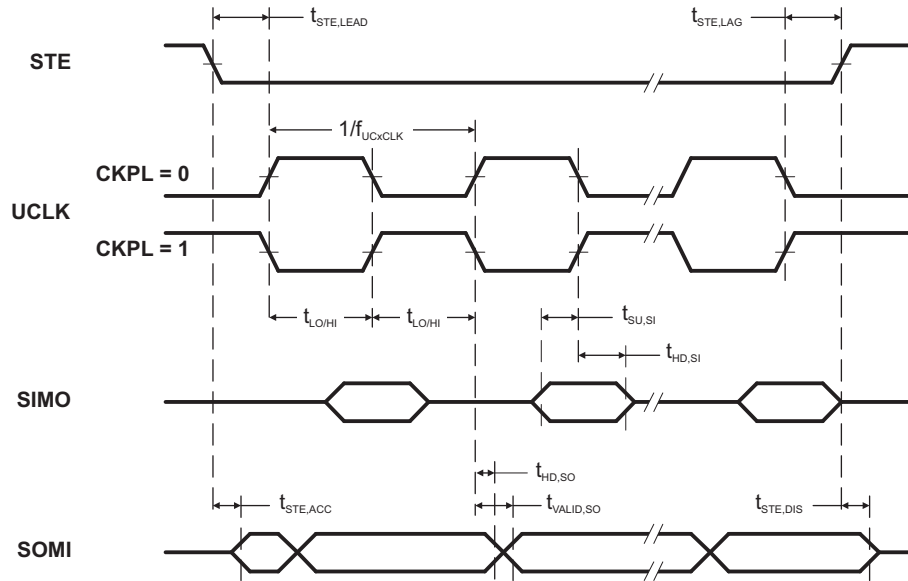


Figure 19. SPI Slave Mode, CKPH = 0

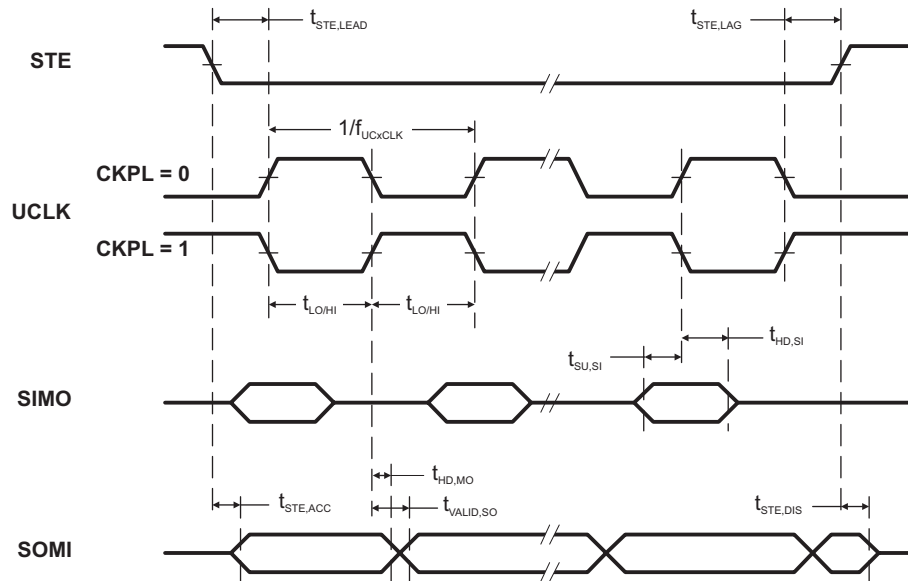


Figure 20. SPI Slave Mode, CKPH = 1

USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 21](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---|-----------------|----------------------------|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | | | | f _{SYSTEM} | MHz |
| f _{SCL} | SCL clock frequency | 2.2 V, 3 V | 0 | | 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START | 2.2 V, 3 V | f _{SCL} ≤ 100 kHz | 4.0 | | μs |
| | | | f _{SCL} > 100 kHz | 0.6 | | |
| t _{SU,STA} | Setup time for a repeated START | 2.2 V, 3 V | f _{SCL} ≤ 100 kHz | 4.7 | | μs |
| | | | f _{SCL} > 100 kHz | 0.6 | | |
| t _{HD,DAT} | Data hold time | 2.2 V, 3 V | 0 | | | ns |
| t _{SU,DAT} | Data setup time | 2.2 V, 3 V | 250 | | | ns |
| t _{SU,STO} | Setup time for STOP | 2.2 V, 3 V | f _{SCL} ≤ 100 kHz | 4.0 | | μs |
| | | | f _{SCL} > 100 kHz | 0.6 | | |
| t _{SP} | Pulse duration of spikes suppressed by input filter | 2.2 V | 50 | | 600 | ns |
| | | 3 V | 50 | | 600 | |

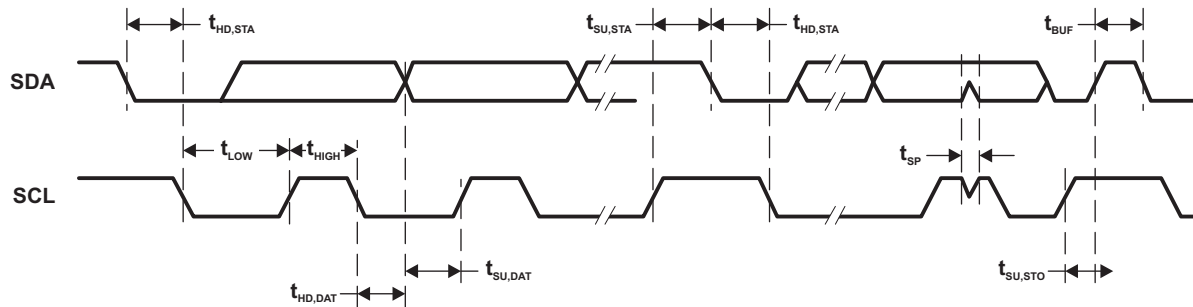


Figure 21. I2C Mode Timing

LCD_B Recommended Operating Conditions

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT | | |
|---------------------------|--|---|-----|-----------|---|-----------|---|
| $V_{CC,LCD_B,CPen,3.6}$ | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.6$ V | LCDPEN = 1, $0000 < VLCDx \leq 1111$ (charge pump enabled, $V_{LCD} \leq 3.6$ V) | | 2.2 | 3.6 | V | |
| $V_{CC,LCD_B,CPen,3.3}$ | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.3$ V | LCDPEN = 1, $0000 < VLCDx \leq 1100$ (charge pump enabled, $V_{LCD} \leq 3.3$ V) | | 2.0 | 3.6 | V | |
| $V_{CC,LCD_B,int. bias}$ | Supply voltage range, internal biasing, charge pump disabled | LCDPEN = 0, VLCDEXT = 0 | | 2.4 | 3.6 | V | |
| $V_{CC,LCD_B,ext. bias}$ | Supply voltage range, external biasing, charge pump disabled | LCDPEN = 0, VLCDEXT = 0 | | 2.4 | 3.6 | V | |
| $V_{CC,LCD_B,VLCDEXT}$ | Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled | LCDPEN = 0, VLCDEXT = 1 | | 2.0 | 3.6 | V | |
| $V_{LDCAP/R33}$ | External LCD voltage at LDCAP/R33, internal or external biasing, charge pump disabled | LCDPEN = 0, VLCDEXT = 1 | | 2.4 | 3.6 | V | |
| C_{LDCAP} | Capacitor on LDCAP when charge pump enabled | LCDPEN = 1, $VLCDx > 0000$ (charge pump enabled) | | 4.7 | 10 | μ F | |
| f_{Frame} | LCD frame frequency range | $f_{LCD} = 2 \times mux \times f_{FRAME}$ with mux = 1 (static), 2, 3, 4 | | 0 | 100 | Hz | |
| $f_{ACLK,in}$ | ACLK input frequency range | 30 | 32 | 40 | | kHz | |
| C_{Panel} | Panel capacitance | 100-Hz frame frequency | | | 10000 | pF | |
| V_{R33} | Analog input voltage at R33 | LCDPEN = 0, VLCDEXT = 1 | | 2.4 | $V_{CC} + 0.2$ | V | |
| $V_{R23,1/3bias}$ | Analog input voltage at R23 | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | | V_{R13} | $V_{R33} \cdot \frac{V_{R03} + 2/3}{V_{R03}}$ | V_{R33} | V |
| $V_{R13,1/3bias}$ | Analog input voltage at R13 with 1/3 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | | V_{R03} | $V_{R03} \cdot \frac{V_{R03} + 1/3}{V_{R03}}$ | V_{R23} | V |
| $V_{R13,1/2bias}$ | Analog input voltage at R13 with 1/2 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1 | | V_{R03} | $V_{R03} \cdot \frac{V_{R03} + 1/2}{V_{R03}}$ | V_{R33} | V |
| V_{R03} | Analog input voltage at R03 | R0EXT = 1 | | V_{SS} | | | V |
| $V_{LCD} - V_{R03}$ | Voltage difference between V_{LCD} and R03 | LCDPEN = 0, R0EXT = 1 | | 2.4 | $V_{CC} + 0.2$ | | V |
| $V_{LCDREF/R13}$ | External LCD reference voltage applied at LCDREF/R13 | VLCDFREFx = 01 | | 0.8 | 1.2 | 1.5 | V |

LCD_B Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------|--|--|-----------------|-----------------|------|-----|------|
| V _{LCD} | LCD voltage, with internal reference | VLCDx = 0000, VLCDEXT = 0 | 2.4 V to 3.6 V | V _{CC} | | | V |
| | | LCDCPEN = 1, VLCDx = 0001 | 2.0 V to 3.6 V | 2.59 | | | |
| | | LCDCPEN = 1, VLCDx = 0010 | | 2.65 | | | |
| | | LCDCPEN = 1, VLCDx = 0011 | | 2.71 | | | |
| | | LCDCPEN = 1, VLCDx = 0100 | | 2.78 | | | |
| | | LCDCPEN = 1, VLCDx = 0101 | | 2.84 | | | |
| | | LCDCPEN = 1, VLCDx = 0110 | | 2.91 | | | |
| | | LCDCPEN = 1, VLCDx = 0111 | | 2.97 | | | |
| | | LCDCPEN = 1, VLCDx = 1000 | | 3.03 | | | |
| | | LCDCPEN = 1, VLCDx = 1001 | | 3.09 | | | |
| | | LCDCPEN = 1, VLCDx = 1010 | | 3.15 | | | |
| | | LCDCPEN = 1, VLCDx = 1011 | | 3.22 | | | |
| | | LCDCPEN = 1, VLCDx = 1100 | | 3.28 | | | |
| | | LCDCPEN = 1, VLCDx = 1101 | | 2.2 V to 3.6 V | 3.34 | | |
| LCDCPEN = 1, VLCDx = 1110 | 3.40 | | | | | | |
| LCDCPEN = 1, VLCDx = 1111 | 3.46 | | 3.53 | | | | |
| I _{CC,Peak,CP} | Peak supply currents due to charge pump activities | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | 200 | | | μA |
| t _{LCD,CP,on} | Time to charge C _{LCD} when discharge | C _{LCDCAP} = 4.7 μF, LCDCPEN = 0→1, VLCDx = 1111 | 2.2 V | | 100 | 500 | ms |
| I _{CP,Load} | Maximum charge pump load current | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | 50 | | | μA |
| R _{LCD,Seg} | LCD driver output impedance, segment lines | LCDCPEN = 1, VLCDx = 1000, I _{LOAD} = ±10 μA | 2.2 V | | | 10 | kΩ |
| R _{LCD,COM} | LCD driver output impedance, common lines | LCDCPEN = 1, VLCDx = 1000, I _{LOAD} = ±10 μA | 2.2 V | | | 10 | kΩ |

10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|---|-----------------|-----|-----|------------------|------|
| AV _{CC} | Analog supply voltage | AV _{CC} and DV _{CC} are connected together, AV _{SS} and DV _{SS} are connected together, V _(AVSS) = V _(DVSS) = 0 V | | 1.8 | | 3.6 | V |
| V _(Ax) | Analog input voltage range ⁽²⁾ | All ADC10_A pins: P1.0 to P1.5, P3.6, P3.7 | | | | AV _{CC} | V |
| I _{ADC10_A} | Operating supply current into AVCC terminal. REF module and reference buffer off. | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00 | 2.2 V | | 70 | 105 | μA |
| | | | 3 V | | 80 | 115 | |
| | Operating supply current into AVCC terminal. REF module on, reference buffer on. | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01 | 3 V | | 130 | 185 | μA |
| | | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VREF = 2.5 V | 3 V | | 120 | 170 | μA |
| Operating supply current into AVCC terminal. REF module off, reference buffer off. | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VREF = 2.5 V | 3 V | | 85 | 120 | μA | |
| C _I | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad. | 2.2 V | | 3.5 | | pF |
| R _I | Input MUX ON resistance | AV _{CC} > 2.0 V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 36 | kΩ |
| | | 1.8 V < AV _{CC} < 2.0 V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 96 | |

(1) The leakage current is defined in the leakage current table with P2.x/Ax parameter.

(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors. See ⁰.

10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|---|-----------------|------|-----|-----|------|
| f _{ADC10CLK} | | For specified performance of ADC10_A linearity parameters | 2.2 V, 3 V | 0.45 | 5 | 5.5 | MHz |
| f _{ADC10OSC} | Internal ADC10_A oscillator ⁽¹⁾ | ADC10DIV = 0, f _{ADC10CLK} = f _{ADC10OSC} | 2.2 V, 3 V | 4.2 | 4.8 | 5.4 | MHz |
| t _{CONVERT} | Conversion time | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, f _{ADC10OSC} = 4 MHz to 5 MHz | 2.2 V, 3 V | 2.4 | | 3.0 | μs |
| | | External f _{ADC10CLK} from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0 | | | | | |
| ⁽²⁾ t _{ADC10ON} | Turn on settling time of the ADC | See ⁽³⁾ | | | | 100 | ns |
| t _{Sample} | Sampling time | R _S = 1000 Ω, R _I = 96 kΩ, C _I = 3.5 pF ⁽⁴⁾ | 1.8 V | 3 | | | μs |
| | | R _S = 1000 Ω, R _I = 36 kΩ, C _I = 3.5 pF ⁽⁴⁾ | 3 V | 1 | | | μs |

(1) The ADC10OSC is sourced directly from MODOSC inside the UCS.

(2) 12 × ADC10DIV × 1/f_{ADC10CLK}

(3) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.

(4) Approximately eight Tau (τ) are needed to get an error of less than ±0.5 LSB

10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|--|--|-----------------|------|------|------|-------------------|
| E _I | Integral linearity error | 1.4 V ≤ (VEREF+ - VEREF-)min ≤ 1.6 V | | -1.0 | | +1.0 | LSB |
| | | 1.6 V < (VEREF+ - VEREF-)min ≤ V _{AVCC} | | -1.0 | | +1.0 | |
| E _D | Differential linearity error | (VEREF+ - VEREF-)min ≤ (VEREF+ - VEREF-), C _{VEREF+} = 20 pF | | -1.0 | | +1.0 | LSB |
| E _O | Offset error | (VEREF+ - VEREF-)min ≤ (VEREF+ - VEREF-), Internal impedance of source R _S < 100 Ω, C _{VEREF+} = 20 pF | | -1.0 | | +1.0 | LSB |
| E _G | Gain error, external reference | (VEREF+ - VEREF-)min ≤ (VEREF+ - VEREF-), C _{VEREF+} = 20 pF | | -1.0 | | +1.0 | LSB |
| | Gain error, external reference, buffered | | | -5 | | +5 | |
| | Gain error, internal reference | See ⁽¹⁾ | | -1.5 | | +1.5 | %V _{REF} |
| E _T | Total unadjusted error, external reference | (VEREF+ - VEREF-)min ≤ (VEREF+ - VEREF-), C _{VEREF+} = 20 pF | | -2.0 | ±1.0 | +2.0 | LSB |
| | Total unadjusted error, external reference, buffered | | | -5 | ±1.0 | +5 | |
| | Total unadjusted error, internal reference | See ⁽¹⁾ | | -1.5 | ±1.0 | +1.5 | %V _{REF} |

(1) Dominated by the absolute voltage of the integrated reference voltage.

REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|--|-----------------|-----|------|------------------|------|
| VEREF+ | Positive external reference voltage input | VEREF+ > VEREF- ⁽²⁾ | | 1.4 | | AV _{CC} | V |
| VEREF- | Negative external reference voltage input | VEREF+ > VEREF- ⁽³⁾ | | 0 | | 1.2 | V |
| VEREF+ - VEREF- | Differential external reference voltage input | VEREF+ > VEREF- ⁽⁴⁾ | | 1.4 | | AV _{CC} | V |
| I _(VEREF+) I _(VEREF-) | Static input current | 1.4 V ≤ VEREF+ ≤ V(AVCC), VEREF- = 0 V f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x0001, Conversion rate 200 ksps | 2.2 V, 3 V | | ±8.5 | ±26 | μA |
| I _(VEREF+) I _(VEREF-) | Static input current | 1.4 V ≤ VEREF+ ≤ V(AVCC), VEREF- = 0 V f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x1000, Conversion rate 20 ksps | 2.2 V, 3 V | | | ±1 | μA |
| C _(VEREF+/-) | Capacitance at VEREF+ or VEREF- terminal | See ⁽⁵⁾ | | 10 | | | μF |

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- (5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VEREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. See also the *CC430 Family User's Guide* (SLAU259).

REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|--|---|-----------------|------|-------|-------|------------|
| VEREF+ | Positive built-in reference voltage | REFVSEL = {2} for 2.5 V, REFON = REFOUT = 1 | 3 V | | 2.5 | ±1.5% | V |
| VEREF+ | Positive built-in reference voltage | REFVSEL = {1} for 2.0 V, REFON = REFOUT = 1 | 3 V | | 2.01 | ±1.5% | V |
| VEREF+ | Positive built-in reference voltage | REFVSEL = {0} for 1.5 V, REFON = REFOUT = 1 | 2.2 V, 3 V | | 1.505 | ±1.5% | V |
| AV _{CC(min)} | AV _{CC} minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | | | 1.8 | | V |
| AV _{CC(min)} | AV _{CC} minimum voltage, Positive built-in reference active | REFVSEL = {1} for 2.0 V | | | 2.3 | | V |
| AV _{CC(min)} | AV _{CC} minimum voltage, Positive built-in reference active | REFVSEL = {2} for 2.5 V | | | 2.8 | | V |
| I _{REF+} | Operating supply current into AV _{CC} terminal ⁽²⁾ | f _{ADC10CLK} = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V | 3 V | | 15.5 | 19 | μA |
| | | f _{ADC10CLK} = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V | 3 V | | 18 | 24 | μA |
| | | f _{ADC10CLK} = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V | 3 V | | 21 | 30 | μA |
| I _{REF+,REFOUT} | Operating supply current into AV _{CC} terminal with REF output buffer enabled | REFON = 1, REFOUT = 1, REFBURST = 0 | 3 V | | 0.9 | 1.7 | mA |
| I _{L(VREF+)} | Load-current regulation, VREF+ terminal ⁽³⁾ | REFVSEL = {0, 1, 2}, I _{Load,VREF+} = +10 μA or -1000 μA, AV _{CC} = AV _{CC(min)} for each reference level, REFON = REFOUT = 1 | | | | 2500 | μV/ mA |
| C _{VREF+} | Capacitance at VREF+ terminals | REFON = REFOUT = 1 | | | 20 | 100 | pF |
| TC _{REF+} | Temperature coefficient of built-in reference ⁽⁴⁾ | REFVSEL = {0, 1, 2}, REFON = 1 | | | 30 | 50 | ppm/ °C |
| I _{SENSOR} | Operating supply current into AV _{CC} terminal ⁽⁵⁾ | REFON = 0, INCH = 0Ah, ADC10ON = NA, T _A = 30°C | 2.2 V | | 150 | 180 | μA |
| | | | 3 V | | 150 | 190 | |
| V _{SENSOR} | See ⁽⁶⁾ | ADC10ON = 1, INCH = 0Ah, T _A = 30°C | 2.2 V | | 765 | | mV |
| | | | 3 V | | 765 | | |
| V _{MID} | AV _{CC} divider at channel 11 | ADC10ON = 1, INCH = 0Bh, V _{MID} is approximately 0.5 × V _{AVCC} | 2.2 V | 1.06 | 1.1 | 1.14 | V |
| | | | 3 V | 1.46 | 1.5 | 1.54 | |
| t _{SENSOR(sample)} | Sample time required if channel 10 is selected ⁽⁷⁾ | ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | | | 30 | | μs |
| t _{MID(sample)} | Sample time required if channel 11 is selected ⁽⁸⁾ | ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | | | 1 | | μs |
| PSRR _{DC} | Power supply rejection ratio (dc) | AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , T _A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1 | | | 120 | 300 | μV/V |

- (1) The leakage current is defined in the leakage current table with P2.x/Ax parameter.
- (2) The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
- (3) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB trace and other factors. Positive load currents are flowing into the device.
- (4) Calculated using the box method: (MAX(-40 to 85°C) - MIN(-40 to 85°C)) / MIN(-40 to 85°C)/(85°C - (-40°C)).
- (5) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
- (6) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
- (7) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.
- (8) The on-time t_{MID(on)} is included in the sampling time t_{MID(sample)}; no additional on time is needed.

REF, Built-In Reference (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|---|---|-----------------|-----|--------------------------------|-----|------|----|
| PSRR_AC Power supply rejection ratio (ac) | AV _{CC} = AV _{CC (min)} - AV _{CC(max)} , T _A = 25°C, f = 1 kHz, ΔV _{pp} = 100 mV, REFVSEL = {0, 1, 2}, REFON = 1 | | | 6.4 | | mV/V | |
| t _{SETTLE} Settling time of reference voltage ⁽⁹⁾ | AV _{CC} = AV _{CC (min)} - AV _{CC(max)} , REFVSEL = {0, 1, 2}, REFON = 0 → 1 | | | T _A = -40°C to 85°C | 23 | 125 | μs |
| | | | | T _A = 25°C | 23 | 50 | |
| | | | | T _A = 85°C | 16 | 25 | |

(9) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

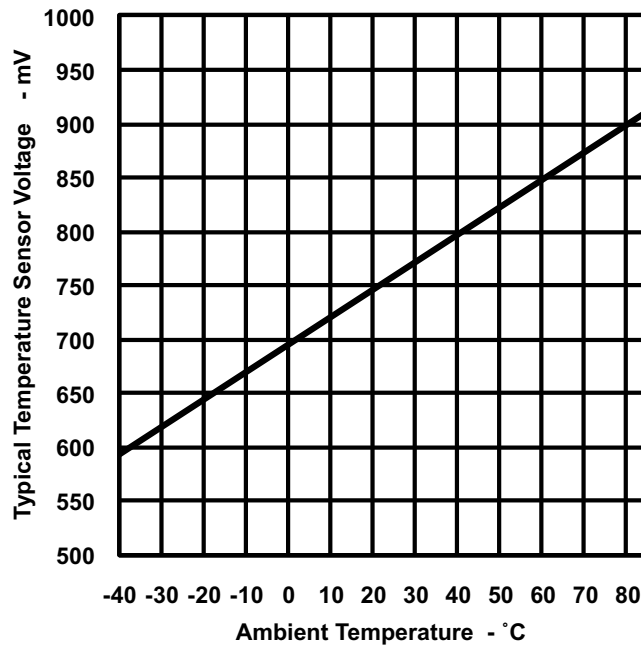


Figure 22. Typical Temperature Sensor Voltage

Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|------------------------|---|---|------------|--------------------|--------------------|--------------------|----|
| V _{CC} | Supply voltage | | 1.8 | | 3.6 | V | |
| I _{AVCC_COMP} | Comparator operating supply current into AV _{CC} . Excludes reference resistor ladder. | CBPWRMD = 00, CBON = 1, CBRSx = 00 | 1.8 V | | 40 | μA | |
| | | | 2.2 V | | 31 | | |
| | | | 3 V | | 32 | | |
| | | 2.2 V, 3 V | | 10 | 17 | | |
| | | CBPWRMD = 10, CBON = 1, CBRSx = 00 | 2.2 V, 3 V | | 0.2 | 0.85 | |
| I _{AVCC_REF} | Quiescent current of resistor ladder into AV _{CC} . Includes REF module current. | CBREFACC = 0, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0 | 2.2 V, 3 V | | 10 | 17 | μA |
| | | | 2.2 V, 3 V | | 33 | 40 | μA |
| V _{REF} | Reference voltage level | CBREFLx = 01, CBREFACC = 0 | ≥1.8 V | 1.49 | ±1.5% | V | |
| V _{REF} | Reference voltage level | CBREFLx = 10, CBREFACC = 0 | ≥2.2 V | 1.988 | ±1.5% | V | |
| V _{REF} | Reference voltage level | CBREFLx = 11, CBREFACC = 0 | ≥3.0 V | 2.5 | ±1.5% | V | |
| V _{IC} | Common mode input range | | 0 | | V _{CC} -1 | V | |
| V _{OFFSET} | Input offset voltage | CBPWRMD = 00 | | | ±20 | mV | |
| V _{OFFSET} | Input offset voltage | CBPWRMD = 01, 10 | | | ±10 | mV | |
| C _{IN} | Input capacitance | | | 5 | | pF | |
| R _{SIN} | Series input resistance | ON - switch closed | | 3 | 4 | kΩ | |
| | | OFF - switch opened | | 50 | | MΩ | |
| t _{PD} | Propagation delay, response time | CBPWRMD = 00, CBF = 0 | | | 450 | ns | |
| | | CBPWRMD = 01, CBF = 0 | | | 600 | ns | |
| | | CBPWRMD = 10, CBF = 0 | | | 50 | μs | |
| t _{PD,filter} | Propagation delay with filter active | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 00 | | 0.35 | 0.6 | 1.5 | μs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 01 | | 0.6 | 1.0 | 1.8 | μs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 10 | | 1.0 | 1.8 | 3.4 | μs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 11 | | 1.8 | 3.4 | 6.5 | μs |
| t _{EN_CMP} | Comparator enable time | CBON = 0 to CBON = 1, CBPWRMD = 00, 01 | | 1 | 2 | μs | |
| | | CBON = 0 to CBON = 1, CBPWRMD = 10 | | | 1.5 | μs | |
| t _{EN_REF} | Resistor reference enable time | CBON = 0 to CBON = 1 | | 1.0 | 1.5 | μs | |
| TC _{REF} | Temperature coefficient reference | | | | 50 | ppm/°C | |
| V _{CB_REF} | Reference voltage for a given tap | VIN = reference into resistor ladder, n = 0 to 31 | | VIN × (n+0.5) / 32 | VIN × (n+1) / 32 | VIN × (n+1.5) / 32 | V |

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----------------------|-----------------|-----------------|-----|--------|
| DV _{CC(PGM/ERASE)} | Program and erase supply voltage | | 1.8 | | 3.6 | V |
| I _{PGM} | Average supply current from DVCC during program | | | 3 | 5 | mA |
| I _{ERASE} | Average supply current from DVCC during erase | | | 2 | 6.5 | mA |
| I _{MERASE} , I _{BANK} | Average supply current from DVCC during mass erase or bank erase | | | | 2.5 | mA |
| t _{CPT} | Cumulative program time ⁽¹⁾ | | | | 16 | ms |
| | Program AND erase endurance | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | 100 | | | years |
| t _{Word} | Word or byte program time ⁽²⁾ | | 64 | | 85 | μs |
| t _{Block, 0} | Block program time for first byte or word ⁽²⁾ | | 49 | | 65 | μs |
| t _{Block, 1-(N-1)} | Block program time for each additional byte or word, except for last byte or word ⁽²⁾ | | 37 | | 49 | μs |
| t _{Block, N} | Block program time for last byte or word ⁽²⁾ | | 55 | | 73 | μs |
| t _{Erase} | Erase time for segment erase, mass erase, and bank erase when available ⁽²⁾ | | 23 | | 32 | ms |
| f _{MCLK,MGR} | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1) | | 0 | | 1 | MHz |

- (1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
 (2) These values are hardwired into the flash controller's state machine.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse length | 2.2 V, 3 V | 0.025 | | 15 | μs |
| t _{SBW,En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾ | 2.2 V, 3 V | | | 1 | μs |
| t _{SBW,Rst} | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | μs |
| f _{TCK} | TCK input frequency - 4-wire JTAG ⁽²⁾ | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | MHz |
| R _{Internal} | Internal pull-down resistance on TEST | 2.2 V, 3 V | 45 | 60 | 80 | kΩ |

- (1) Tools accessing the Spy-Bi-Wire interface need to wait for the minimum t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
 (2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

RF1A CC1101-Based Radio Parameters

RF1A Recommended Operating Conditions

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--------------------|-----|-----|-------|
| V _{CC} | Supply voltage range during radio operation | 2.0 | | 3.6 | V |
| PMMCOREVx | Core voltage range, PMMCOREVx setting during radio operation | 2 | | 3 | |
| RF frequency range | 300 MHz range | 300 | | 348 | MHz |
| | 400 MHz range | 389 ⁽¹⁾ | | 464 | |
| | 800/900 MHz range | 779 | | 928 | |
| Data rate | 2-FSK | 0.6 | | 500 | kBaud |
| | 2-GFSK, OOK, and ASK | 0.6 | | 250 | |
| | (Shaped) MSK (also known as differential offset QPSK) ⁽²⁾ | 26 | | 500 | |
| RF crystal frequency | | | 26 | 27 | MHz |
| RF crystal tolerance | Total tolerance including initial tolerance, crystal loading, aging and temperature dependency. ⁽³⁾ | | ±40 | | ppm |
| RF crystal load capacitance | | 10 | 13 | 20 | pF |
| RF crystal effective series resistance | | | | 100 | Ω |

(1) If using a 27-MHz crystal, the lower frequency limit for this band is 392 MHz.

(2) If using optional Manchester encoding, the data rate in kbps is half the baud rate.

(3) The acceptable crystal tolerance depends on frequency band, channel bandwidth, and spacing. Also see Design Note *DN005 -- CC11xx Sensitivity versus Frequency Offset and Crystal Accuracy (SWRA122)*.

RF Crystal Oscillator, XT2

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|-----------------|-----|-----|-----|------|
| Start-up time ⁽²⁾ | | | 150 | 810 | μs |
| Duty cycle | | 45 | 50 | 55 | % |

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see [Table 49](#)).

(2) The start-up time depends to a very large degree on the used crystal.

Current Consumption, Reduced-Power Modes

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-----|-----|------|
| Current consumption | RF crystal oscillator only (for example, SLEEP state with MCSM0.OSC_FORCE_ON = 1) | | 100 | | μA |
| | IDLE state (including RF crystal oscillator) | | 1.7 | | mA |
| | FSTXON state (only the frequency synthesizer is running) ⁽²⁾ | | 9.5 | | mA |

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see [Table 49](#)).

(2) This current consumption is also representative of other intermediate states when going from IDLE to RX or TX, including the calibration state.

Current Consumption, Receive Mode

 $T_A = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$ (unless otherwise noted)^{(1) (2)}

| PARAMETER | FREQUENCY (MHz) | DATA RATE (kBaud) | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|-------------------------|-----------------|-------------------|--|---|--|------|-----|-----|------|
| | | | | | | | | | |
| Current consumption, RX | 315 | 1.2 | Register settings optimized for reduced current | Input at -100 dBm (close to sensitivity limit) | | 17 | | mA | |
| | | | | Input at -40 dBm (well above sensitivity limit) | | 16 | | | |
| | | 38.4 | | Input at -100 dBm (close to sensitivity limit) | | 17 | | | |
| | | | | Input at -40 dBm (well above sensitivity limit) | | 16 | | | |
| | | 250 | | Input at -100 dBm (close to sensitivity limit) | | 18 | | | |
| | | | | Input at -40 dBm (well above sensitivity limit) | | 16.5 | | | |
| | 433 | 1.2 | Register settings optimized for reduced current | Input at -100 dBm (close to sensitivity limit) | | 18 | | | |
| | | | | Input at -40 dBm (well above sensitivity limit) | | 17 | | | |
| | | 38.4 | | Input at -100 dBm (close to sensitivity limit) | | 18 | | | |
| | | | | Input at -40 dBm (well above sensitivity limit) | | 17 | | | |
| | | 250 | | Input at -100 dBm (close to sensitivity limit) | | 18.5 | | | |
| | | | | Input at -40 dBm (well above sensitivity limit) | | 17 | | | |
| | 868, 915 | 1.2 | Register settings optimized for reduced current ⁽³⁾ | Input at -100 dBm (close to sensitivity limit) | | 16 | | | |
| | | | | Input at -40 dBm (well above sensitivity limit) | | 15 | | | |
| | | 38.4 | | Input at -100 dBm (close to sensitivity limit) | | 16 | | | |
| | | | | Input at -40 dBm (well above sensitivity limit) | | 15 | | | |
| | | 250 | | Input at -100 dBm (close to sensitivity limit) | | 16 | | | |
| | | | | Input at -40 dBm (well above sensitivity limit) | | 15 | | | |

- (1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see [Table 49](#)).
- (2) Reduced current setting (MDMCFG2.DEM_DCFILT_OFF = 1) gives a slightly lower current consumption at the cost of a reduction in sensitivity. See tables "RF Receive" for additional details on current consumption and sensitivity.
- (3) For 868 or 915 MHz, see [Figure 23](#) for current consumption with register settings optimized for sensitivity.

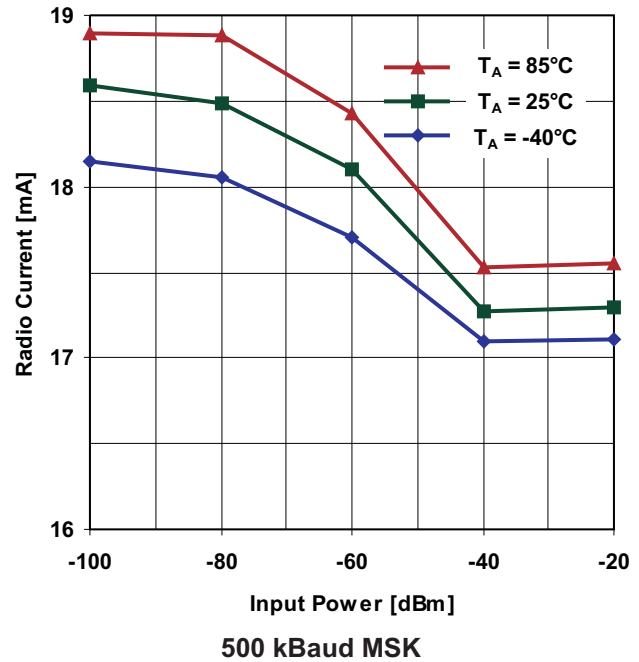
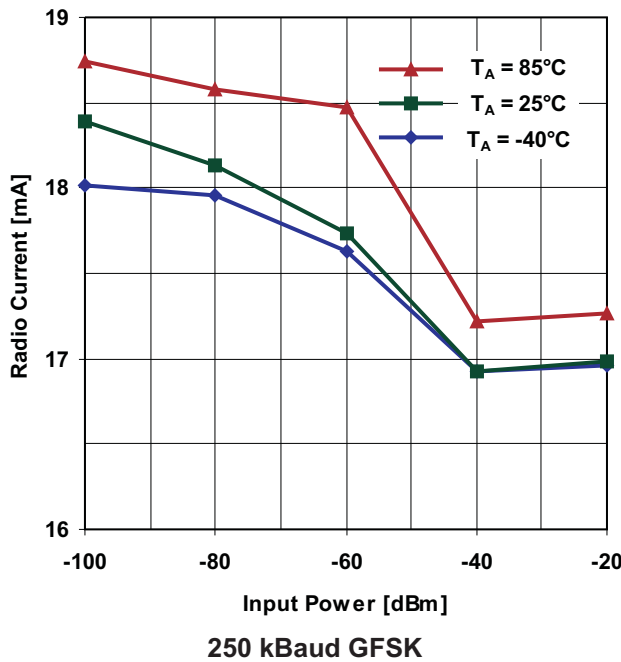
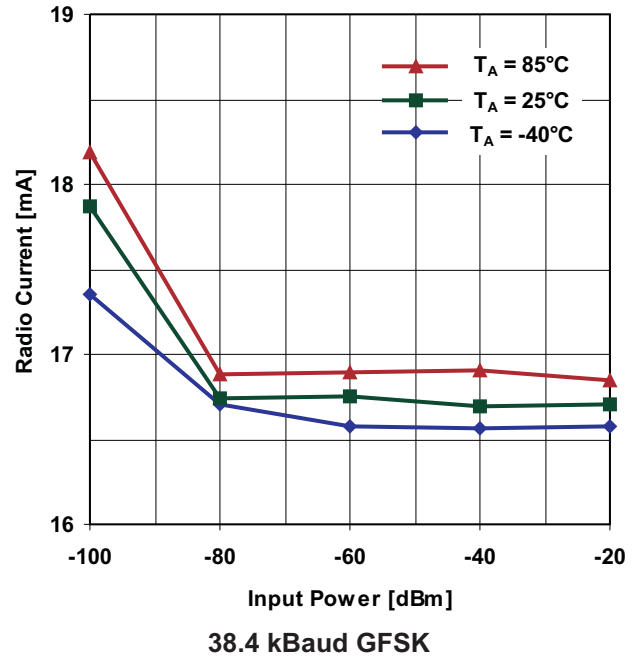
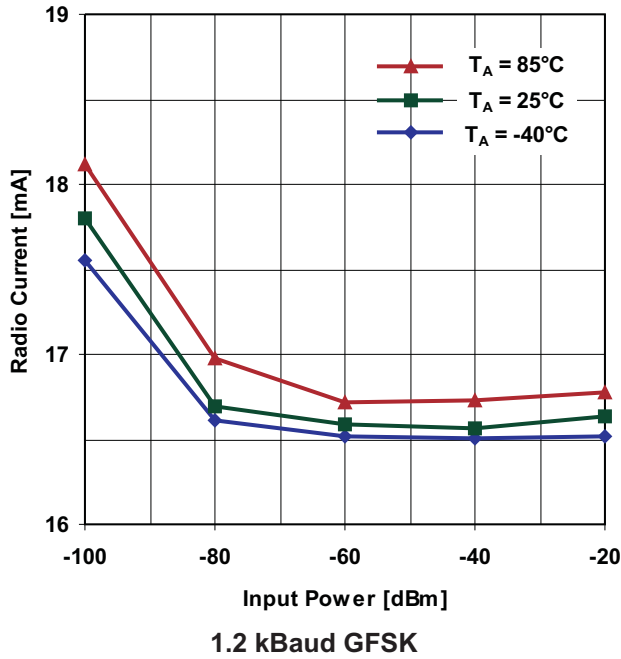


Figure 23. Typical RX Current Consumption Over Temperature and Input Power Level, 868 MHz, Sensitivity-Optimized Setting

Current Consumption, Transmit Mode

$T_A = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$ (unless otherwise noted)^{(1) (2)}

| PARAMETER | FREQUENCY [MHz] | PATABLE Setting | OUTPUT POWER (dBm) | MIN | TYP | MAX | UNIT | |
|-------------------------|-----------------|-----------------|--------------------|-----|-----|-----|------|----|
| Current consumption, TX | 315 | 0xC0 | max. | | 26 | | mA | |
| | | 0xC4 | +10 | | 25 | | mA | |
| | | 0x51 | 0 | | 15 | | mA | |
| | | 0x29 | -6 | | 15 | | mA | |
| | 433 | 0xC0 | max. | | | 33 | | mA |
| | | 0xC6 | +10 | | | 29 | | mA |
| | | 0x50 | 0 | | | 17 | | mA |
| | | 0x2D | -6 | | | 17 | | mA |
| | 868 | 0xC0 | max. | | | 36 | | mA |
| | | 0xC3 | +10 | | | 33 | | mA |
| | | 0x8D | 0 | | | 18 | | mA |
| | | 0x2D | -6 | | | 18 | | mA |
| | 915 | 0xC0 | max. | | | 35 | | mA |
| | | 0xC3 | +10 | | | 32 | | mA |
| | | 0x8D | 0 | | | 18 | | mA |
| | | 0x2D | -6 | | | 18 | | mA |

- (1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see [Table 49](#)).
 (2) Reduced current setting (MDMCFG2.DEM_DCFILT_OFF = 1) gives a slightly lower current consumption at the cost of a reduction in sensitivity. See tables "RF Receive" for additional details on current consumption and sensitivity.

Typical TX Current Consumption, 315 MHz, 25°C

| PARAMETER | PATABLE Setting | Output Power (dBm) | V _{CC} | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|-------------------------|-----------------|--------------------|-----------------|-------|------|--|-------|------|--|-------|------|----|------|
| | | | | | | | | | | | | | |
| Current consumption, TX | 0xC0 | max. | | | 27.5 | | | 26.4 | | | 28.1 | mA | |
| | 0xC4 | +10 | | | 25.1 | | | 25.2 | | | 25.3 | | |
| | 0x51 | 0 | | | 14.4 | | | 14.6 | | | 14.7 | | |
| | 0x29 | -6 | | | 14.2 | | | 14.7 | | | 15.0 | | |

Typical TX Current Consumption, 433 MHz, 25°C

| PARAMETER | PATABLE Setting | Output Power (dBm) | V _{CC} | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|-------------------------|-----------------|--------------------|-----------------|-------|------|--|-------|------|--|-------|------|----|------|
| | | | | | | | | | | | | | |
| Current consumption, TX | 0xC0 | max. | | | 33.1 | | | 33.4 | | | 33.8 | mA | |
| | 0xC6 | +10 | | | 28.6 | | | 28.8 | | | 28.8 | | |
| | 0x50 | 0 | | | 16.6 | | | 16.8 | | | 16.9 | | |
| | 0x2D | -6 | | | 16.8 | | | 17.5 | | | 17.8 | | |

Typical TX Current Consumption, 868 MHz

| PARAMETER | PATABLE Setting | Output Power (dBm) | V _{CC} | T _A | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|-------------------------|-----------------|--------------------|-----------------|----------------|-------|------|------|-------|------|------|-------|------|------|------|
| | | | | | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | |
| Current consumption, TX | 0xC0 | max. | | | 36.7 | 35.2 | 34.2 | 38.5 | 35.5 | 34.9 | 37.1 | 35.7 | 34.7 | mA |
| | 0xC3 | +10 | | | 34.0 | 32.8 | 32.0 | 34.2 | 33.0 | 32.5 | 34.3 | 33.1 | 32.2 | |
| | 0x8D | 0 | | | 18.0 | 17.6 | 17.5 | 18.3 | 17.8 | 18.1 | 18.4 | 18.0 | 17.7 | |
| | 0x2D | -6 | | | 17.1 | 17.0 | 17.2 | 17.8 | 17.8 | 18.3 | 18.2 | 18.1 | 18.1 | |

Typical TX Current Consumption, 915 MHz

| PARAMETER | PATABLE Setting | Output Power (dBm) | V _{CC} | T _A | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|-------------------------|-----------------|--------------------|-----------------|----------------|-------|------|------|-------|------|------|-------|------|------|------|
| | | | | | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | |
| Current consumption, TX | 0xC0 | max. | | | 35.5 | 33.8 | 33.2 | 36.2 | 34.8 | 33.6 | 36.3 | 35.0 | 33.8 | mA |
| | 0xC3 | +10 | | | 33.2 | 32.0 | 31.0 | 33.4 | 32.1 | 31.2 | 33.5 | 32.3 | 31.3 | |
| | 0x8D | 0 | | | 17.8 | 17.4 | 17.1 | 18.1 | 17.6 | 17.3 | 18.2 | 17.8 | 17.5 | |
| | 0x2D | -6 | | | 17.0 | 16.9 | 16.9 | 17.7 | 17.6 | 17.6 | 18.1 | 18.0 | 18.0 | |

RF Receive, Overall

$T_A = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$ (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---------------------------------|-----|-----|-----|------|
| Digital channel filter bandwidth ⁽²⁾ | | 58 | | 812 | kHz |
| Spurious emissions ^{(3) (4)} | 25 MHz to 1 GHz | | -68 | -57 | dBm |
| | Above 1 GHz | | -66 | -47 | |
| RX latency | Serial operation ⁽⁵⁾ | | 9 | | bit |

- (1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see [Table 49](#)).
- (2) User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0 MHz crystal)
- (3) Typical radiated spurious emission is -49 dBm measured at the VCO frequency
- (4) Maximum figure is the ETSI EN 300 220 limit
- (5) Time from start of reception until data is available on the receiver data output pin is equal to 9 bit.

RF Receive, 315 MHz

$T_A = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$ (unless otherwise noted)⁽¹⁾

2-FSK, 1% packet error rate, 20-byte packet length, Sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF = 0 (unless otherwise noted)

| PARAMETER | DATA RATE (kBaoud) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--------------------|--|-----|------|-----|------|
| Receiver sensitivity | 0.6 | 14.3-kHz deviation, 58-kHz digital channel filter bandwidth | | -117 | | dBm |
| | 1.2 | 5.2-kHz deviation, 58-kHz digital channel filter bandwidth ⁽²⁾ | | -111 | | |
| | 38.4 | 20-kHz deviation, 100-kHz digital channel filter bandwidth ⁽³⁾ | | -103 | | |
| | 250 | 127-kHz deviation, 540-kHz digital channel filter bandwidth ⁽⁴⁾ | | -95 | | |
| | 500 | MSK, 812-kHz digital channel filter bandwidth ⁽⁴⁾ | | -86 | | |

- (1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see [Table 49](#)).
- (2) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -109 dBm.
- (3) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -102 dBm.
- (4) MDMCFG2.DEM_DCFILT_OFF=1 can not be used for data rates ≥ 250 kBaoud.

RF Receive, 433 MHz

$T_A = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$ (unless otherwise noted)⁽¹⁾

2-FSK, 1% packet error rate, 20-byte packet length, Sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF = 0 (unless otherwise noted)

| PARAMETER | DATA RATE (kBaoud) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--------------------|--|-----|------|-----|------|
| Receiver sensitivity | 0.6 | 14.3-kHz deviation, 58-kHz digital channel filter bandwidth | | -114 | | dBm |
| | 1.2 | 5.2-kHz deviation, 58-kHz digital channel filter bandwidth ⁽²⁾ | | -111 | | |
| | 38.4 | 20-kHz deviation, 100-kHz digital channel filter bandwidth ⁽³⁾ | | -104 | | |
| | 250 | 127-kHz deviation, 540-kHz digital channel filter bandwidth ⁽⁴⁾ | | -93 | | |
| | 500 | MSK, 812-kHz digital channel filter bandwidth ⁽⁴⁾ | | -85 | | |

- (1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see [Table 49](#)).
- (2) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -109 dBm.
- (3) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -101 dBm.
- (4) MDMCFG2.DEM_DCFILT_OFF=1 can not be used for data rates ≥ 250 kBaoud.

RF Receive, 868 MHz and 915 MHz

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)⁽¹⁾

1% packet error rate, 20-byte packet length, Sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF = 0 (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----------------|------|-----|------|
| 0.6-kBaud data rate, 2-FSK, 14.3-kHz deviation, 58-kHz digital channel filter bandwidth (unless otherwise noted) | | | | | |
| Receiver sensitivity | | | -115 | | dBm |
| 1.2-kBaud data rate, 2-FSK, 5.2-kHz deviation, 58-kHz digital channel filter bandwidth (unless otherwise noted) | | | | | |
| Receiver sensitivity ⁽²⁾ | 2-GFSK modulation by setting MDMCFG2.MOD_FORMAT=2, Gaussian filter with BT = 0.5 | | -109 | | dBm |
| | | | -109 | | |
| Saturation | FIFOTHR.CLOSE_IN_RX=0 ⁽³⁾ | | -28 | | dBm |
| Adjacent channel rejection | Desired channel 3 dB above the sensitivity limit, 100 kHz channel spacing ⁽⁴⁾ | -100-kHz offset | 39 | | dB |
| | | +100-kHz offset | 39 | | |
| Image channel rejection | IF frequency 152 kHz, desired channel 3 dB above the sensitivity limit | | 29 | | dB |
| Blocking | Desired channel 3 dB above the sensitivity limit ⁽⁵⁾ | ±2 MHz offset | -48 | | dBm |
| | | ±10 MHz offset | -40 | | dBm |
| 38.4-kBaud data rate, 2-FSK, 20-kHz deviation, 100-kHz digital channel filter bandwidth (unless otherwise noted) | | | | | |
| Receiver sensitivity ⁽⁶⁾ | 2-GFSK modulation by setting MDMCFG2.MOD_FORMAT = 2, Gaussian filter with BT = 0.5 | | -102 | | dBm |
| | | | -101 | | |
| Saturation | FIFOTHR.CLOSE_IN_RX=0 ⁽³⁾ | | -19 | | dBm |
| Adjacent channel rejection | Desired channel 3 dB above the sensitivity limit, 200 kHz channel spacing ⁽⁵⁾ | -200-kHz offset | 20 | | dB |
| | | +200-kHz offset | 25 | | |
| Image channel rejection | IF frequency 152 kHz, Desired channel 3 dB above the sensitivity limit | | 23 | | dB |
| Blocking | Desired channel 3 dB above the sensitivity limit ⁽⁵⁾ | ±2-MHz offset | -48 | | dBm |
| | | ±10-MHz offset | -40 | | dBm |
| 250-kBaud data rate, 2-FSK, 127-kHz deviation, 540-kHz digital channel filter bandwidth (unless otherwise noted) | | | | | |
| Receiver sensitivity ⁽⁷⁾ | 2-GFSK modulation by setting MDMCFG2.MOD_FORMAT = 2, Gaussian filter with BT = 0.5 | | -90 | | dBm |
| | | | -90 | | |
| Saturation | FIFOTHR.CLOSE_IN_RX=0 ⁽³⁾ | | -19 | | dBm |
| Adjacent channel rejection | Desired channel 3 dB above the sensitivity limit, 750-kHz channel spacing ⁽⁸⁾ | -750-kHz offset | 24 | | dB |
| | | +750-kHz offset | 30 | | |
| Image channel rejection | IF frequency 304 kHz, Desired channel 3 dB above the sensitivity limit | | 18 | | dB |
| Blocking | Desired channel 3 dB above the sensitivity limit ⁽⁸⁾ | ±2-MHz offset | -53 | | dBm |
| | | ±10-MHz offset | -39 | | dBm |
| 500-kBaud data rate, MSK, 812-kHz digital channel filter bandwidth (unless otherwise noted) | | | | | |
| Receiver sensitivity ⁽⁷⁾ | | | -84 | | dBm |
| Image channel rejection | IF frequency 355 kHz, Desired channel 3 dB above the sensitivity limit | | -2 | | dB |
| Blocking | Desired channel 3 dB above the sensitivity limit ⁽⁹⁾ | ±2-MHz offset | -53 | | dBm |
| | | ±10-MHz offset | -38 | | dBm |

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 49).

(2) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -107 dBm

(3) See Design Note *DN010 Close-in Reception with CC1101 (SWRA147)*.

(4) See Figure 24 for blocking performance at other offset frequencies.

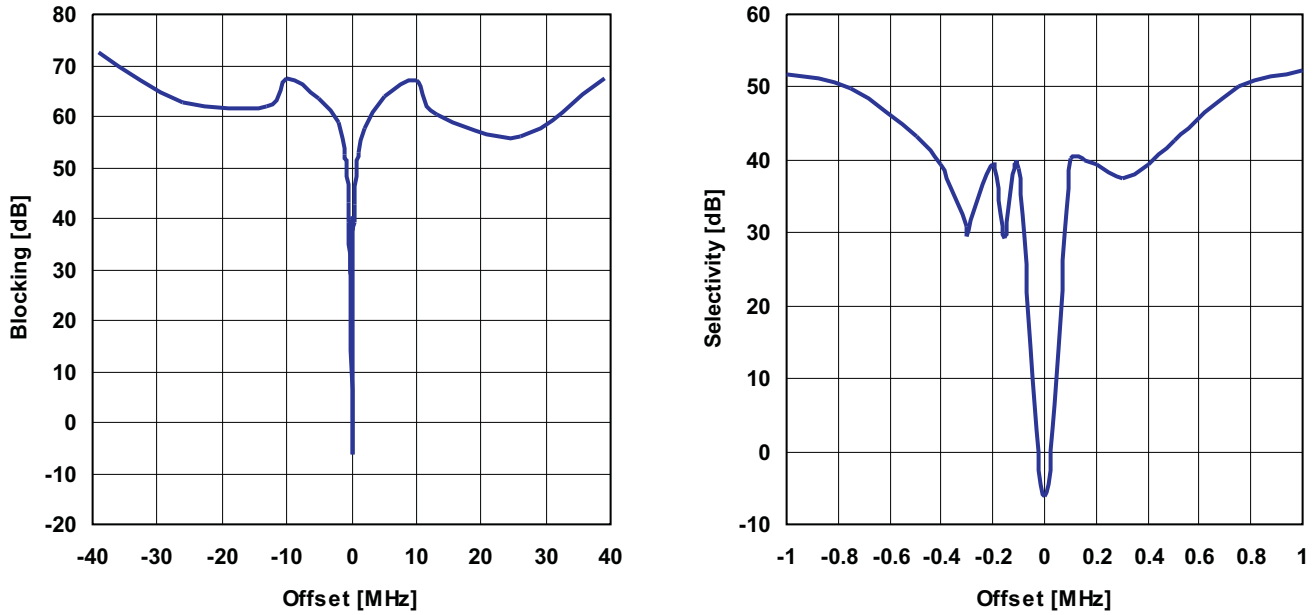
(5) See Figure 25 for blocking performance at other offset frequencies.

(6) Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced by approximately 2 mA close to the sensitivity limit. The sensitivity is typically reduced to -100dBm.

(7) MDMCFG2.DEM_DCFILT_OFF = 1 cannot be used for data rates ≥ 250 kbaud.

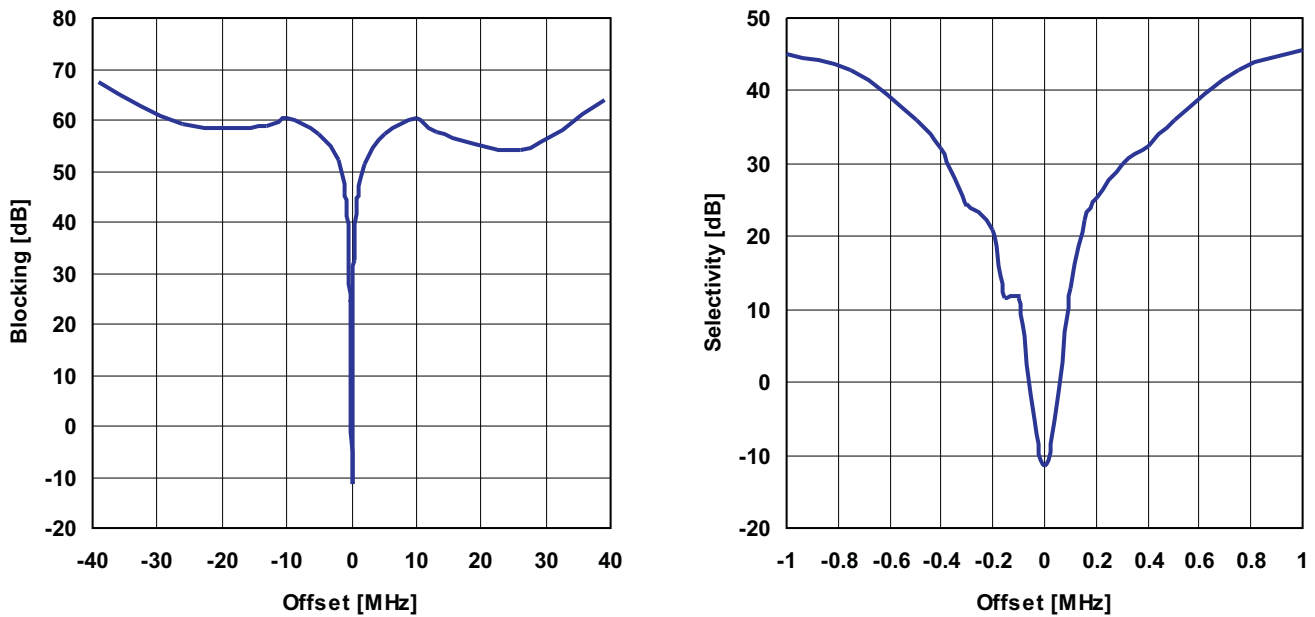
(8) See Figure 26 for blocking performance at other offset frequencies.

(9) See Figure 27 for blocking performance at other offset frequencies.



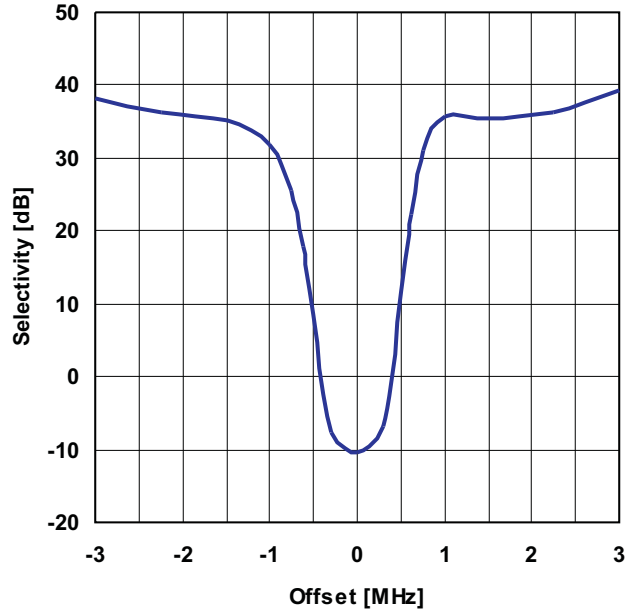
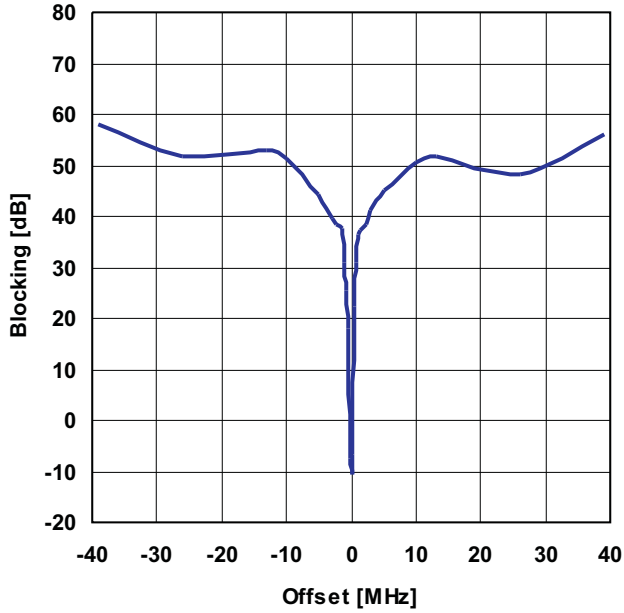
NOTE: 868.3 MHz, 2-FSK, 5.2-kHz deviation, IF frequency is 152.3 kHz, digital channel filter bandwidth is 58 kHz

Figure 24. Typical Selectivity at 1.2-kBaud Data Rate



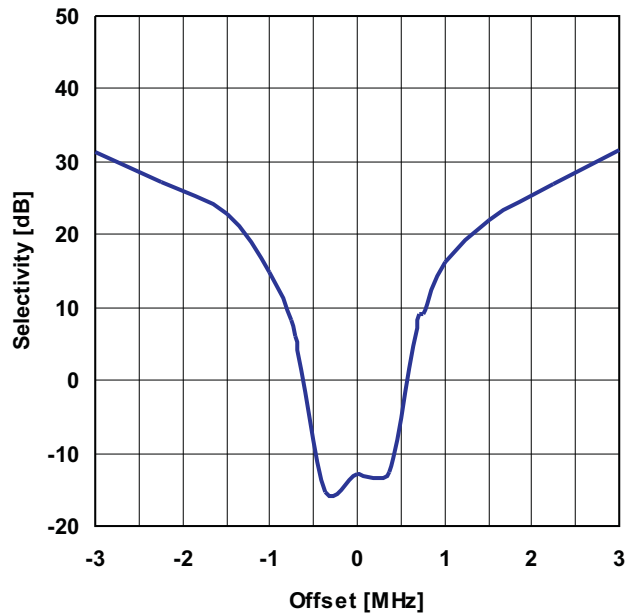
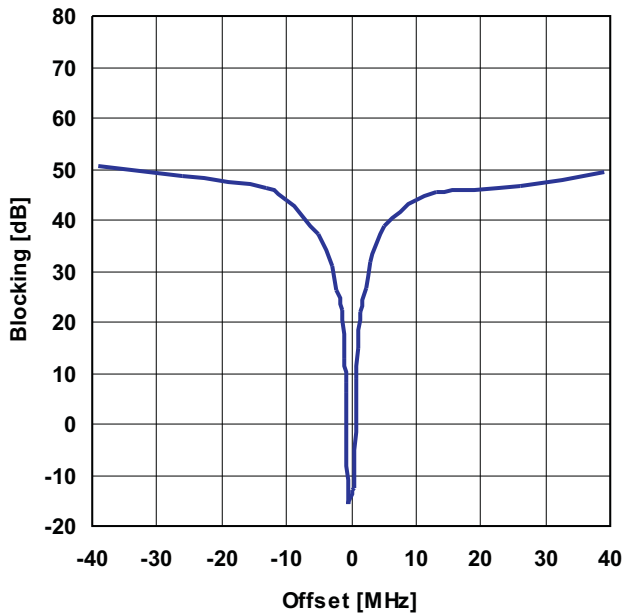
NOTE: 868 MHz, 2-FSK, 20 kHz deviation, IF frequency is 152.3 kHz, digital channel filter bandwidth is 100 kHz

Figure 25. Typical Selectivity at 38.4-kBaud Data Rate



NOTE: 868 MHz, 2-FSK, IF frequency is 304 kHz, digital channel filter bandwidth is 540 kHz

Figure 26. Typical Selectivity at 250-kBaud Data Rate



NOTE: 868 MHz, 2-FSK, IF frequency is 355 kHz, digital channel filter bandwidth is 812 kHz

Figure 27. Typical Selectivity at 500-kBaud Data Rate

Typical Sensitivity, 315 MHz, Sensitivity Optimized Setting

| PARAMETER | DATA RATE (kBaud) | V _{CC} | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|-------------------------|-------------------|-----------------|-------|------|------|-------|------|------|-------|------|------|------|
| | | T _A | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | |
| Sensitivity, 315 MHz | 1.2 | | -112 | -112 | -110 | -112 | -111 | -109 | -112 | -111 | -108 | dBm |
| | 38.4 | | -105 | -105 | -104 | -105 | -103 | -102 | -105 | -104 | -102 | |
| | 250 | | -95 | -95 | -92 | -94 | -95 | -92 | -95 | -94 | -91 | |

Typical Sensitivity, 433 MHz, Sensitivity Optimized Setting

| PARAMETER | DATA RATE (kBaud) | V _{CC} | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|-------------------------|-------------------|-----------------|-------|------|------|-------|------|------|-------|------|------|------|
| | | T _A | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | |
| Sensitivity, 433 MHz | 1.2 | | -111 | -110 | -108 | -111 | -111 | -108 | -111 | -110 | -107 | dBm |
| | 38.4 | | -104 | -104 | -101 | -104 | -104 | -101 | -104 | -103 | -101 | |
| | 250 | | -93 | -94 | -91 | -93 | -93 | -90 | -93 | -93 | -90 | |

Typical Sensitivity, 868 MHz, Sensitivity Optimized Setting

| PARAMETER | DATA RATE (kBaud) | V _{CC} | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|-------------------------|-------------------|-----------------|-------|------|------|-------|------|------|-------|------|------|------|
| | | T _A | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | |
| Sensitivity, 868 MHz | 1.2 | | -109 | -109 | -107 | -109 | -109 | -106 | -109 | -108 | -106 | dBm |
| | 38.4 | | -102 | -102 | -100 | -102 | -102 | -99 | -102 | -101 | -99 | |
| | 250 | | -90 | -90 | -88 | -89 | -90 | -87 | -89 | -90 | -87 | |
| | 500 | | -84 | -84 | -81 | -84 | -84 | -80 | -84 | -84 | -80 | |

Typical Sensitivity, 915 MHz, Sensitivity Optimized Setting

| PARAMETER | DATA RATE (kBaud) | V _{CC} | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|-------------------------|-------------------|-----------------|-------|------|------|-------|------|------|-------|------|------|------|
| | | T _A | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | |
| Sensitivity, 915 MHz | 1.2 | | -109 | -109 | -107 | -109 | -109 | -106 | -109 | -108 | -105 | dBm |
| | 38.4 | | -102 | -102 | -100 | -102 | -102 | -99 | -103 | -102 | -99 | |
| | 250 | | -92 | -92 | -89 | -92 | -92 | -88 | -92 | -92 | -88 | |
| | 500 | | -87 | -86 | -81 | -86 | -86 | -81 | -86 | -85 | -80 | |

RF Transmit

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)⁽¹⁾, P_{TX} = +10 dBm (unless otherwise noted)

| PARAMETER | FREQ (MHz) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|--|--|---|---------------------------|---------------------------|------------|-------|------|--|
| Differential load impedance ⁽²⁾ | 315 | | | 122 + j31 | | | Ω | |
| | 433 | | | 116 + j41 | | | | |
| | 868, 915 | | | 86.5 + j43 | | | | |
| Output power, highest setting ⁽³⁾ | 315 | Delivered to a 50Ω single-ended load via CC430 reference design's RF matching network | | +12 | | | dBm | |
| | 433 | | | +13 | | | | |
| | 868 | | | +11 | | | | |
| | 915 | | | +11 | | | | |
| Output power, lowest setting ⁽³⁾ | | Delivered to a 50Ω single-ended load via CC430 reference design's RF matching network | | -30 | | | dBm | |
| Harmonics, radiated ⁽⁴⁾⁽⁵⁾⁽⁶⁾ | 433 | Second harmonic | | -56 | | | dBm | |
| | | Third harmonic | | -57 | | | | |
| | 868 | Second harmonic | | -50 | | | | |
| | | Third harmonic | | -52 | | | | |
| | 915 | Second harmonic | | -50 | | | | |
| | | Third harmonic | | -54 | | | | |
| Harmonics, conducted | 315 | Frequencies below 960 MHz | | +10 dBm CW | < -38 | | | |
| | | Frequencies above 960 MHz | | | < -48 | | | |
| | 433 | Frequencies below 1 GHz | | +10 dBm CW | -45 | | | |
| | | Frequencies above 1 GHz | | | < -48 | | | |
| | 868 | Second harmonic | | +10 dBm CW | -59 | | | |
| | | Other harmonics | | | < -71 | | | |
| | 915 | Second harmonic | | +11 dBm CW ⁽⁷⁾ | -53 | | | |
| | | Other harmonics | | | < -47 | | | |
| | Spurious emissions, conducted, harmonics not included ⁽⁸⁾ | 315 | Frequencies below 960 MHz | | +10 dBm CW | < -58 | | |
| | | | Frequencies above 960 MHz | | | < -53 | | |
| 433 | | Frequencies below 1 GHz | | +10 dBm CW | < -54 | | | |
| | | Frequencies above 1 GHz | | | < -54 | | | |
| | | Frequencies within 47 to 74, 87.5 to 118, 174 to 230, 470 to 862 MHz | | | < -63 | | | |
| 868 | | Frequencies below 1 GHz | | +10 dBm CW | < -46 | | | |
| | | Frequencies above 1 GHz | | | < -59 | | | |
| | | Frequencies within 47 to 74, 87.5 to 118, 174 to 230, 470 to 862 MHz | | | < -56 | | | |
| 915 | | Frequencies below 960 MHz | | +11 dBm CW | < -49 | | | |
| | | Frequencies above 960 MHz | | | < -63 | | | |
| TX latency ⁽⁹⁾ | | Serial operation | | 8 | | | bits | |

- (1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 49).
- (2) Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna. Follow the CC430 reference designs available from the TI website.
- (3) Output power is programmable, and full range is available in all frequency bands. Output power may be restricted by regulatory limits. See also application note AN050 Using the CC1101 in the European 868 MHz SRD Band (SWRA146) and design note DN013 Programming Output Power on CC1101 (SWRA151), which gives the output power and harmonics when using multi-layer inductors. The output power is then typically +10 dBm when operating at 868 or 915 MHz.
- (4) The antennas used during the radiated measurements (SMAFF-433 from R.W.Badland and Nearson S331 868 or 915) play a part in attenuating the harmonics.
- (5) Measured on EM430F6137RF900 with CW, maximum output power
- (6) All harmonics are below -41.2 dBm when operating in the 902 to 928 MHz band.
- (7) Requirement is -20 dBc under FCC 15.247
- (8) All radiated spurious emissions are within the limits of ETSI. Also see design note DN017 CC11xx 868/915 MHz RF Matching (SWRA168).
- (9) Time from sampling the data on the transmitter data input pin until it is observed on the RF output ports

Optimum PATABLE Settings for Various Output Power Levels and Frequency Bands

$T_A = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$ (unless otherwise noted)⁽¹⁾

| OUTPUT POWER (dBm) | PATABLE SETTING | | | |
|--------------------|-----------------|---------|---------|---------|
| | 315 MHz | 433 MHz | 868 MHz | 915 MHz |
| -30 | 0x12 | 0x05 | 0x03 | 0x03 |
| -12 | 0x33 | 0x26 | 0x25 | 0x25 |
| -6 | 0x29 | 0x2D | 0x2D | 0x2D |
| 0 | 0x51 | 0x50 | 0x8D | 0x8D |
| 10 | 0xC4 | 0xC4 | 0xC3 | 0xC3 |
| max. | 0xC0 | 0xC0 | 0xC0 | 0xC0 |

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see [Table 49](#)).

Typical Output Power, 315 MHz⁽¹⁾

| PARAMETER | PATABLE Setting | V _{CC} | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|--------------------------|-----------------|-----------------|-------|------|------|-------|------|------|-------|------|------|------|
| | | T _A | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | |
| Output power, 315 MHz | 0xC0 (max) | | | 11.9 | | | 11.8 | | | 11.8 | | dBm |
| | 0xC4 (10 dBm) | | | 10.3 | | | 10.3 | | | 10.3 | | |
| | 0xC6 (default) | | | | | | 9.3 | | | | | |
| | 0x51 (0 dBm) | | | 0.7 | | | 0.6 | | | 0.7 | | |
| | 0x29 (-6 dBm) | | | -6.8 | | | -5.6 | | | -5.3 | | |

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 49).

Typical Output Power, 433 MHz⁽¹⁾

| PARAMETER | PATABLE Setting | V _{CC} | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|--------------------------|-----------------|-----------------|-------|------|------|-------|------|------|-------|------|------|------|
| | | T _A | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | |
| Output power, 433 MHz | 0xC0 (max) | | | 12.6 | | | 12.6 | | | 12.6 | | dBm |
| | 0xC4 (10 dBm) | | | 10.3 | | | 10.2 | | | 10.2 | | |
| | 0xC6 (default) | | | | | | 10.0 | | | | | |
| | 0x50 (0 dBm) | | | 0.3 | | | 0.3 | | | 0.3 | | |
| | 0x2D (-6 dBm) | | | -6.4 | | | -5.4 | | | -5.1 | | |

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 49).

Typical Output Power, 868 MHz⁽¹⁾

| PARAMETER | PATABLE Setting | V _{CC} | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|--------------------------|-----------------|-----------------|-------|------|------|-------|------|------|-------|------|------|------|
| | | T _A | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | |
| Output power, 868 MHz | 0xC0 (max) | | 11.9 | 11.2 | 10.5 | 11.9 | 11.2 | 10.5 | 11.9 | 11.2 | 10.5 | dBm |
| | 0xC3 (10 Bm) | | 10.8 | 10.1 | 9.4 | 10.8 | 10.1 | 9.4 | 10.7 | 10.1 | 9.4 | |
| | 0xC6 (default) | | | | | | 8.8 | | | | | |
| | 0x8D (0 dBm) | | 1.0 | 0.3 | -0.3 | 1.1 | 0.3 | -0.3 | 1.1 | 0.3 | -0.3 | |
| | 0x2D (-6 dBm) | | -6.5 | -6.8 | -7.3 | -5.3 | -5.8 | -6.3 | -4.9 | -5.4 | -6.0 | |

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 49).

Typical Output Power, 915 MHz⁽¹⁾

| PARAMETER | PATABLE Setting | V _{CC} | 2.0 V | | | 3.0 V | | | 3.6 V | | | UNIT |
|--------------------------|-----------------|-----------------|-------|------|------|-------|------|------|-------|------|------|------|
| | | T _A | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | -40°C | 25°C | 85°C | |
| Output power, 915 MHz | 0xC0 (max) | | 12.2 | 11.4 | 10.6 | 12.1 | 11.4 | 10.7 | 12.1 | 11.4 | 10.7 | dBm |
| | 0xC3 (10 dBm) | | 11.0 | 10.3 | 9.5 | 11.0 | 10.3 | 9.5 | 11.0 | 10.3 | 9.6 | |
| | 0xC6 (default) | | | | | | 8.8 | | | | | |
| | 0x8D (0 dBm) | | 1.9 | 1.0 | 0.3 | 1.9 | 1.0 | 0.3 | 1.9 | 1.1 | 0.3 | |
| | 0x2D (-6 dBm) | | -5.5 | -6.0 | -6.5 | -4.3 | -4.8 | -5.5 | -3.9 | -4.4 | -5.1 | |

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 49).

Frequency Synthesizer Characteristics

$T_A = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$ (unless otherwise noted)⁽¹⁾

MIN figures are given using a 27-MHz crystal. TYP and MAX figures are given using a 26-MHz crystal.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------------|------|--------------------------|------|--------|
| Programmed frequency resolution ⁽²⁾ | 26 to 27 MHz crystal | 397 | $f_{\text{XOSC}}/2^{16}$ | 412 | Hz |
| Synthesizer frequency tolerance ⁽³⁾ | | | ±40 | | ppm |
| RF carrier phase noise | 50 kHz offset from carrier | | -95 | | dBc/Hz |
| | 100 kHz offset from carrier | | -94 | | |
| | 200 kHz offset from carrier | | -94 | | |
| | 500 kHz offset from carrier | | -98 | | |
| | 1 MHz offset from carrier | | -107 | | |
| | 2 MHz offset from carrier | | -112 | | |
| | 5 MHz offset from carrier | | -118 | | |
| | 10 MHz offset from carrier | | -129 | | |
| PLL turn-on and hop time ⁽⁴⁾ | Crystal oscillator running | 85.1 | | 88.4 | µs |
| PLL RX to TX settling time ⁽⁵⁾ | | 9.3 | | 9.6 | µs |
| PLL TX to RX settling time ⁽⁶⁾ | | 20.7 | | 21.5 | µs |
| PLL calibration time ⁽⁷⁾ | | 694 | | 721 | µs |

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see [Table 49](#)).

(2) The resolution (in Hz) is equal for all frequency bands.

(3) Depends on crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing.

(4) Time from leaving the IDLE state until arriving in the RX, FSTXON, or TX state when not performing calibration.

(5) Settling time for the 1-IF frequency step from RX to TX

(6) Settling time for the 1-IF frequency step from TX to RX

(7) Calibration can be initiated manually or automatically before entering or after leaving RX/TX

Typical RSSI_offset Values

T_A = 25°C, V_{CC} = 3 V (unless otherwise noted)⁽¹⁾

| DATA RATE (kBaud) | RSSI_OFFSET (dB) | |
|-------------------|------------------|---------|
| | 433 MHz | 868 MHz |
| 1.2 | 74 | 74 |
| 38.4 | 74 | 74 |
| 250 | 74 | 74 |
| 500 | 74 | 74 |

(1) All measurement results are obtained using the EM430F6137RF900 with BOM according to tested frequency range (see Table 49).

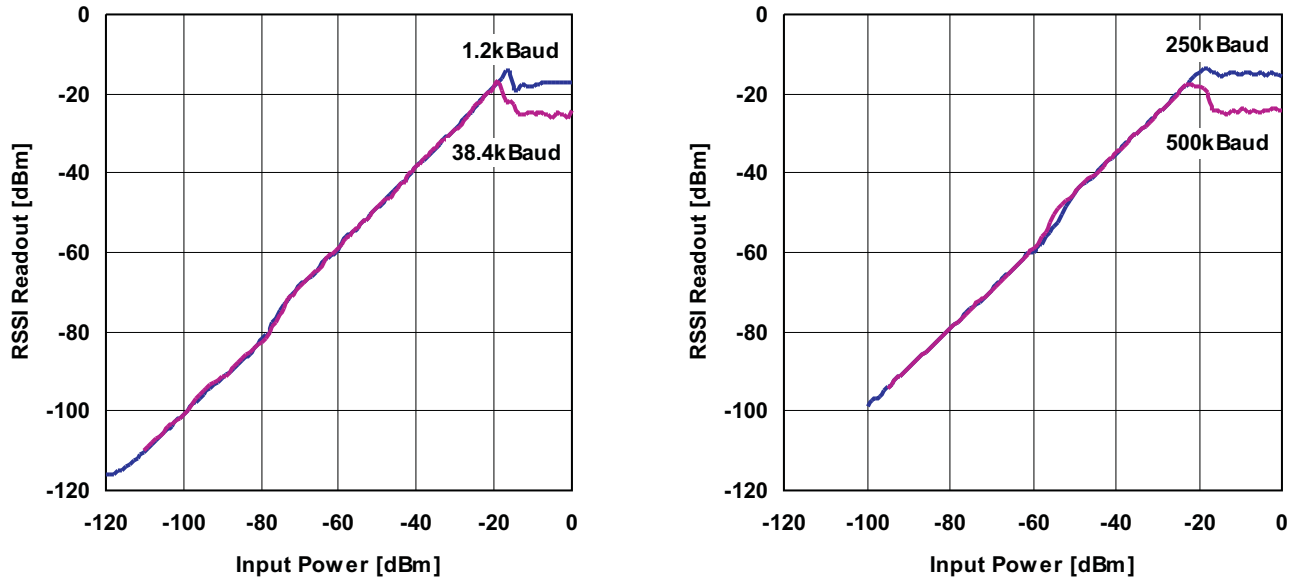
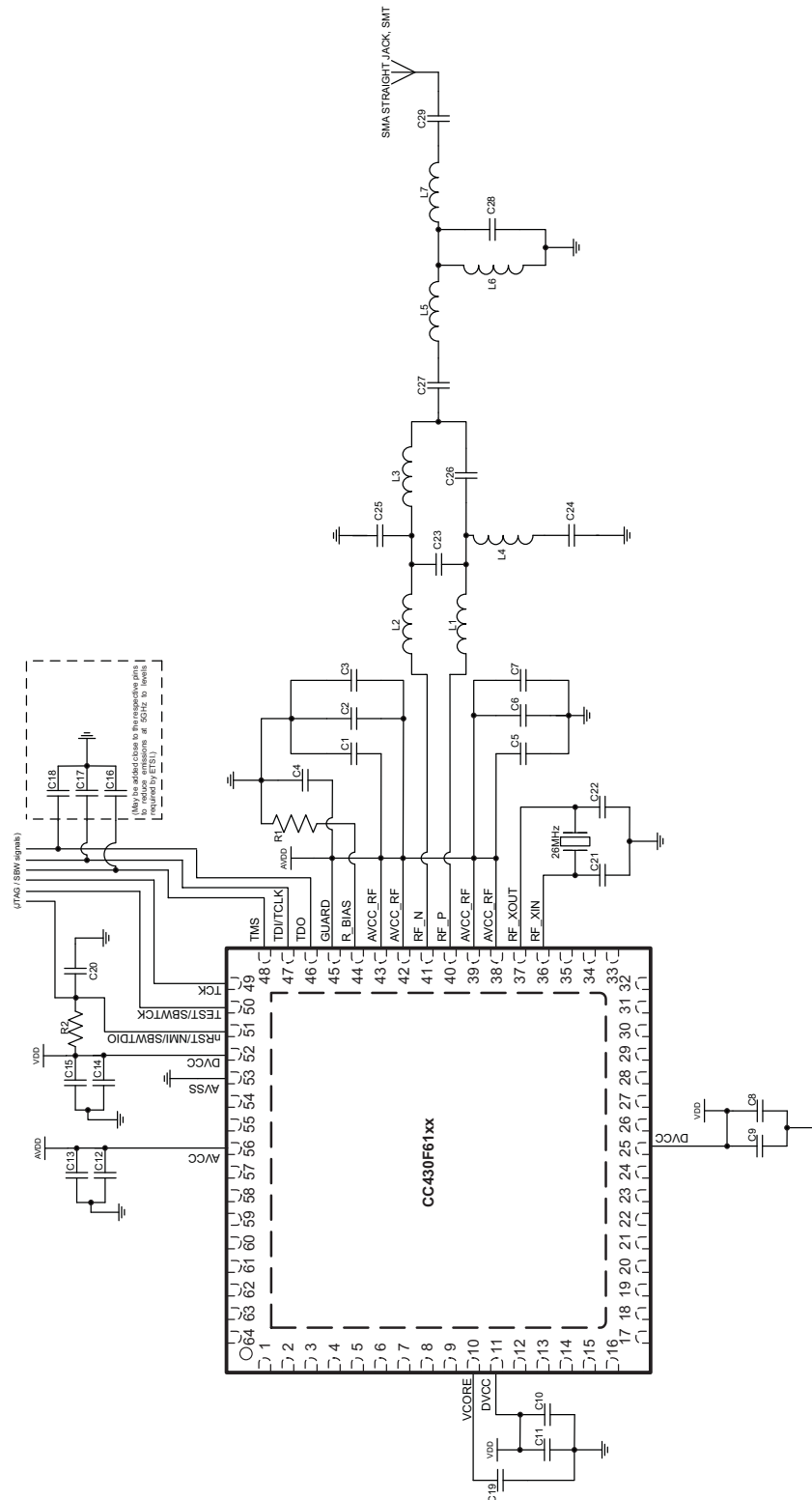


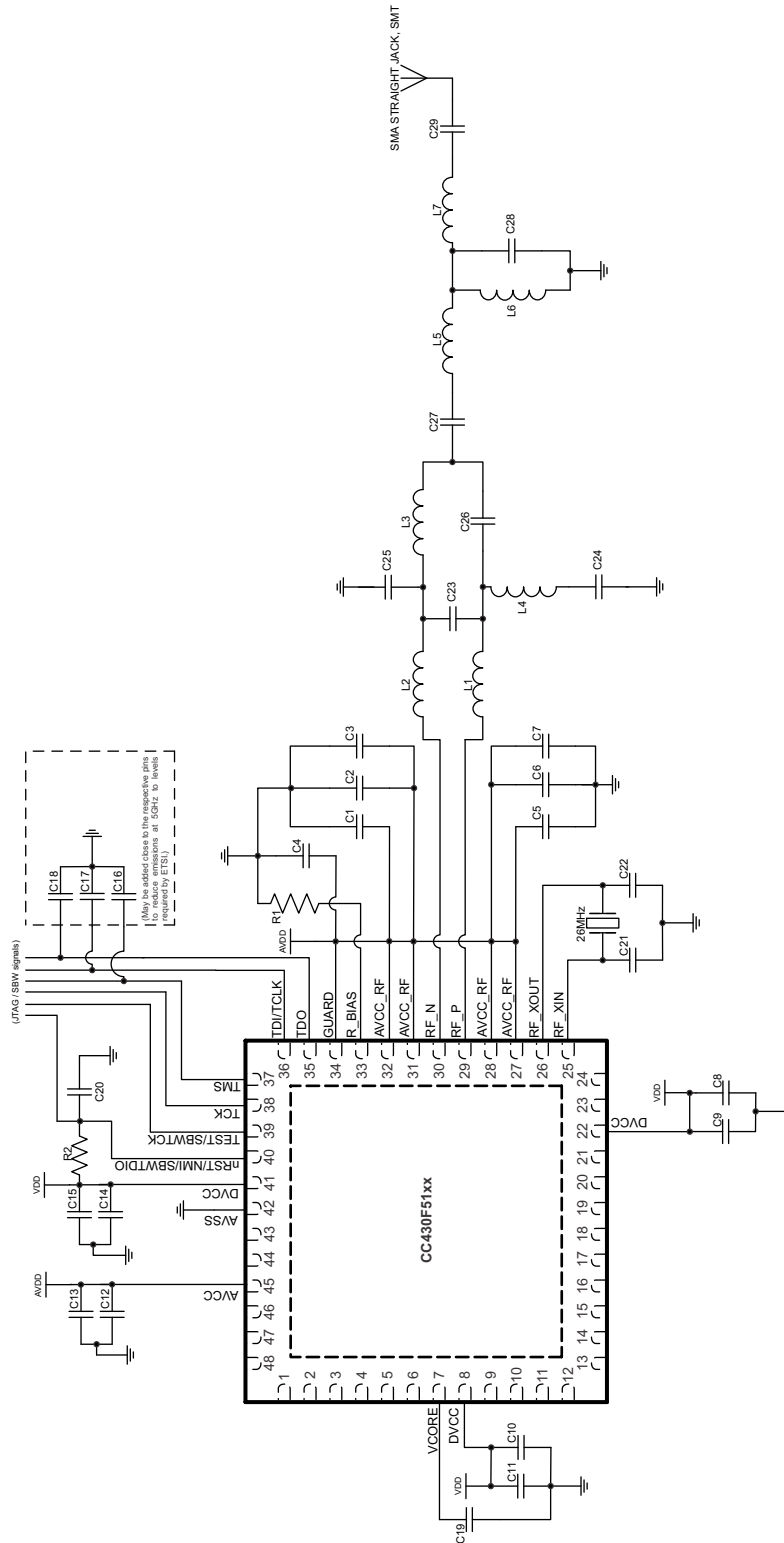
Figure 28. Typical RSSI Value vs Input Power Level for Different Data Rates at 868 MHz

APPLICATION CIRCUIT



For a complete reference design including layout see the CC430 Wireless Development Tools and related documentation.

Figure 29. Typical Application Circuit CC430F61xx



For a complete reference design including layout, see the CC430 Wireless Development Tools and related documentation.

Figure 30. Typical Application Circuit CC430F51xx

Table 49. Bill of Materials

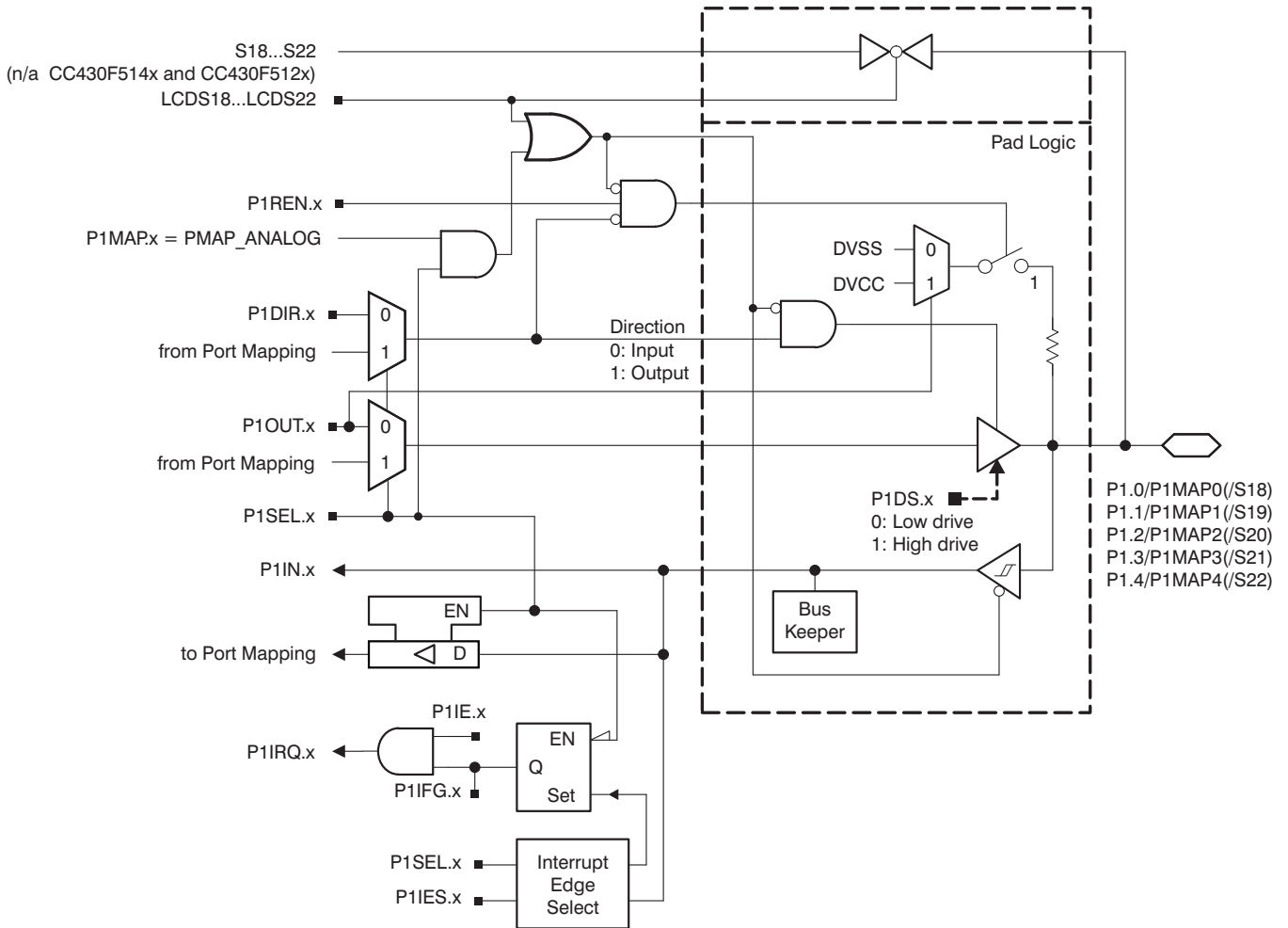
| COMPONENTS | FOR 315 MHz | FOR 433 MHz | FOR 868, 915 MHz | COMMENT |
|-----------------------|--------------------|--------------------|------------------|--|
| C1,3,4,5,7,9,11,13,15 | | 100 nF | | Decoupling capacitors |
| C8,10,12,14 | | 10 μ F | | Decoupling capacitors |
| C2,6,16,17,18 | | 2 pF | | Decoupling capacitors |
| C19 | | 470 nF | | V _{CORE} capacitor |
| C20 | | 2.2 nF | | $\overline{\text{RST}}$ decoupling cap (optimized for SBW) |
| C21,22 | | 27 pF | | Load capacitors for 26 MHz crystal ⁽¹⁾ |
| R1 | | 56 k Ω | | R_BIAS ($\pm 1\%$ required) |
| R2 | | 47k Ω | | $\overline{\text{RST}}$ pullup |
| L1,2 | Capacitors: 220 pF | 0.016 μ H | 0.012 μ H | |
| L3,4 | 0.033 μ H | 0.027 μ H | 0.018 μ H | |
| L5 | 0.033 μ H | 0.047 μ H | 0.015 μ H | |
| L6 | dnp ⁽²⁾ | dnp ⁽²⁾ | 0.0022 μ H | |
| L7 | 0.033 μ H | 0.051 μ H | 0.015 μ H | |
| C23 | dnp ⁽²⁾ | 2.7 pF | 1 pF | |
| C24 | 220 pF | 220 pF | 100 pF | |
| C25 | 6.8 pF | 3.9 pF | 1.5 pF | |
| C26 | 6.8 pF | 3.9 pF | 1.5 pF | |
| C27 | 220 pF | 220 pF | 1.5 pF | |
| C28 | 10 pF | 4.7 pF | 8.2 pF | |
| C29 | 220 pF | 220 pF | 1.5 pF | |

(1) The load capacitance C_L seen by the crystal is $C_L = 1/((1/C_{21})+(1/C_{22})) + C_{\text{parasitic}}$. The parasitic capacitance $C_{\text{parasitic}}$ includes pin capacitance and PCB stray capacitance. It can be typically estimated to be approximately 2.5 pF.

(2) dnp = do not populate

INPUT/OUTPUT SCHEMATICS

Port P1, P1.0 to P1.4, Input/Output With Schmitt Trigger



NOTE: CC430F514x and CC430F512x devices do not provide LCD functionality.

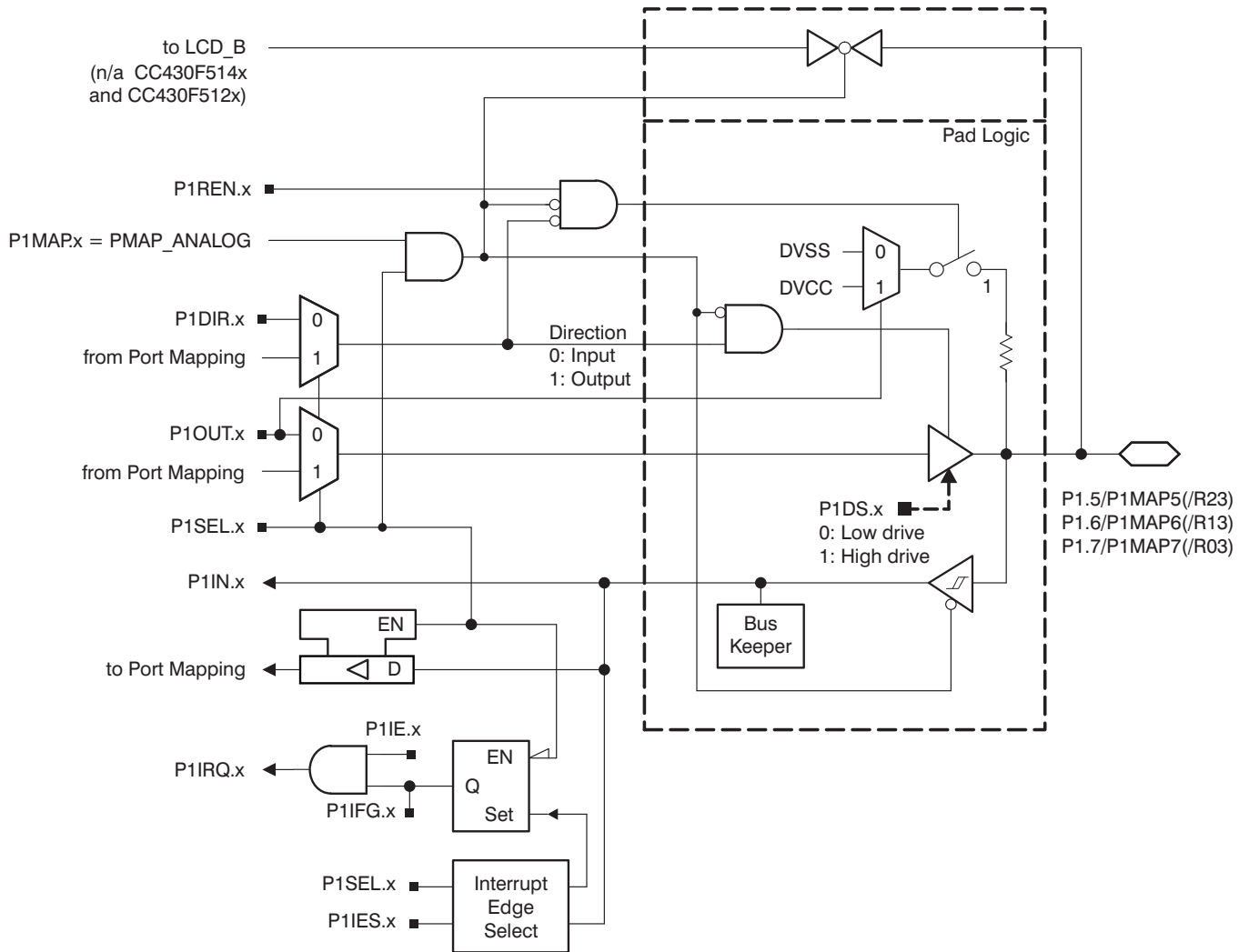
Table 50. Port P1 (P1.0 to P1.4) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | | |
|-----------------|---|---|----------------------|---------|---------------------|---------------------------------|
| | | | P1DIR.x | P1SEL.x | P1MAPx | LCDS19 to LCDS22 ⁽¹⁾ |
| P1.0/P1MAP/S18 | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S18 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P1.1/P1MAP1/S19 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S19 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P1.2/P1MAP2/S20 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S22 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P1.3/P1MAP3/S21 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S21 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P1.4/P1MAP4/S22 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S22 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |

(1) LCDSx not available in CC430F514x and CC430F512x.

(2) According to mapped function (see [Table 10](#))

Port P1, P1.5 to P1.7, Input/Output With Schmitt Trigger



NOTE: CC430F514x and CC430F512x devices do not provide LCD functionality.

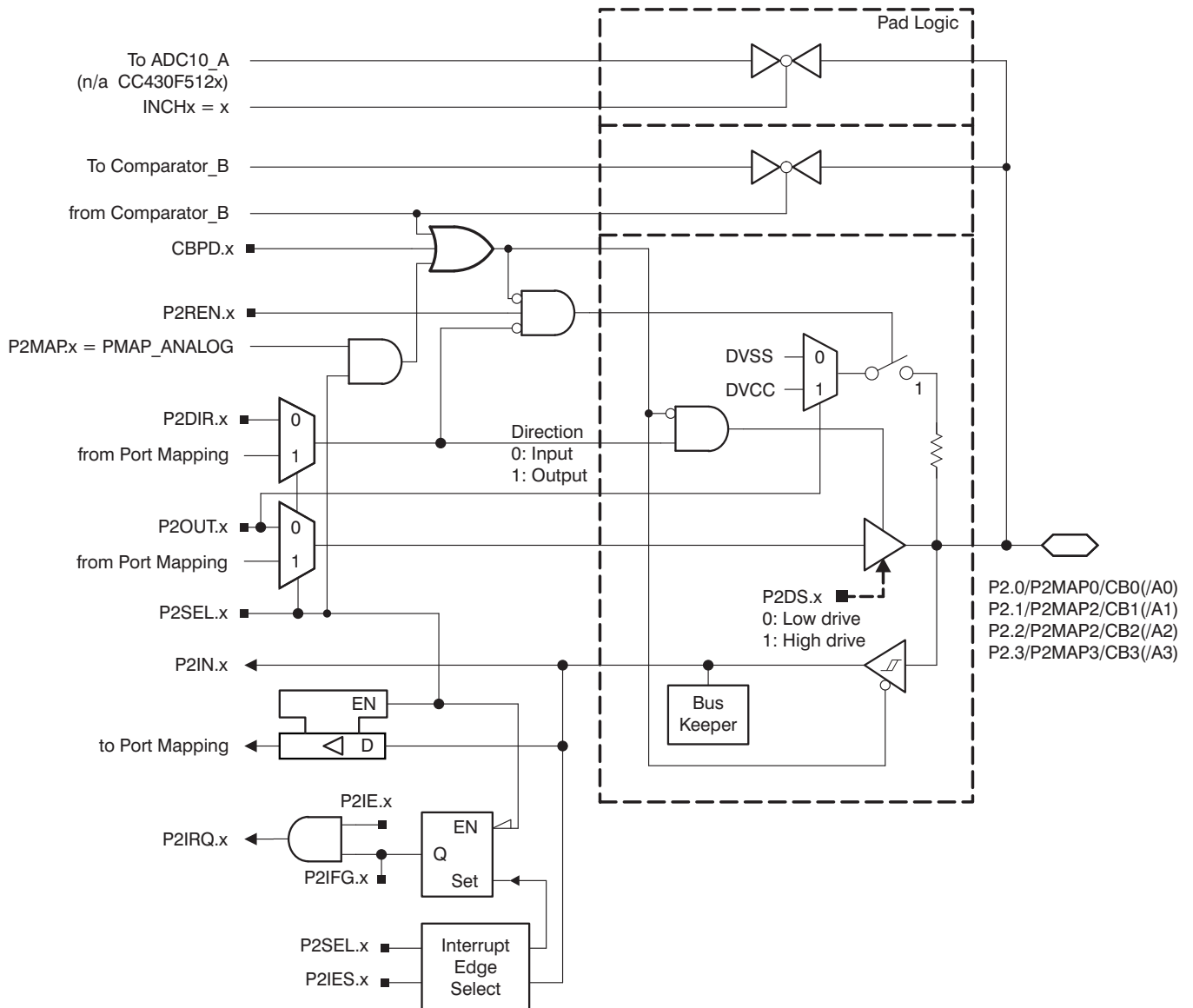
Table 51. Port P1 (P1.5 to P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|----------------------------|---|--|----------------------|---------|---------------------|
| | | | P1DIR.x | P1SEL.x | P1MAPx |
| P1.5/P1MAP5/R23 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ |
| | | R23 ⁽²⁾ (not available on CC430F514x and CC430F512x) | X | 1 | = 31 |
| P1.6/P1MAP6/R13/ LCDREF | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ |
| | | R13/LCDREF ⁽²⁾ (not available on CC430F514x and CC430F512x) | X | 1 | = 31 |
| P1.7/P1MAP7/R03 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ |
| | | R03 ⁽²⁾ (not available on CC430F514x and CC430F512x) | X | 1 | = 31 |

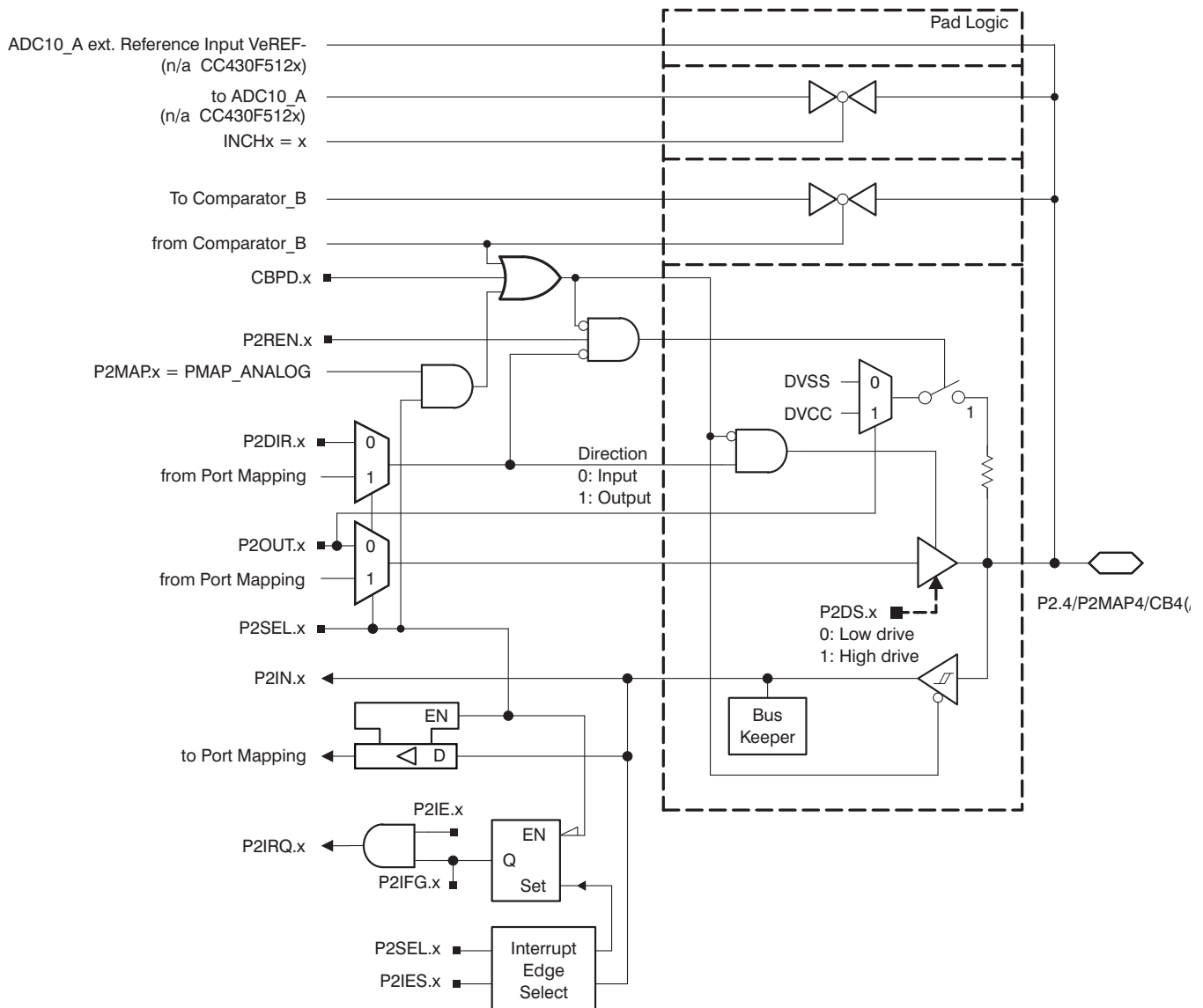
(1) According to mapped function (see [Table 10](#))

(2) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger.

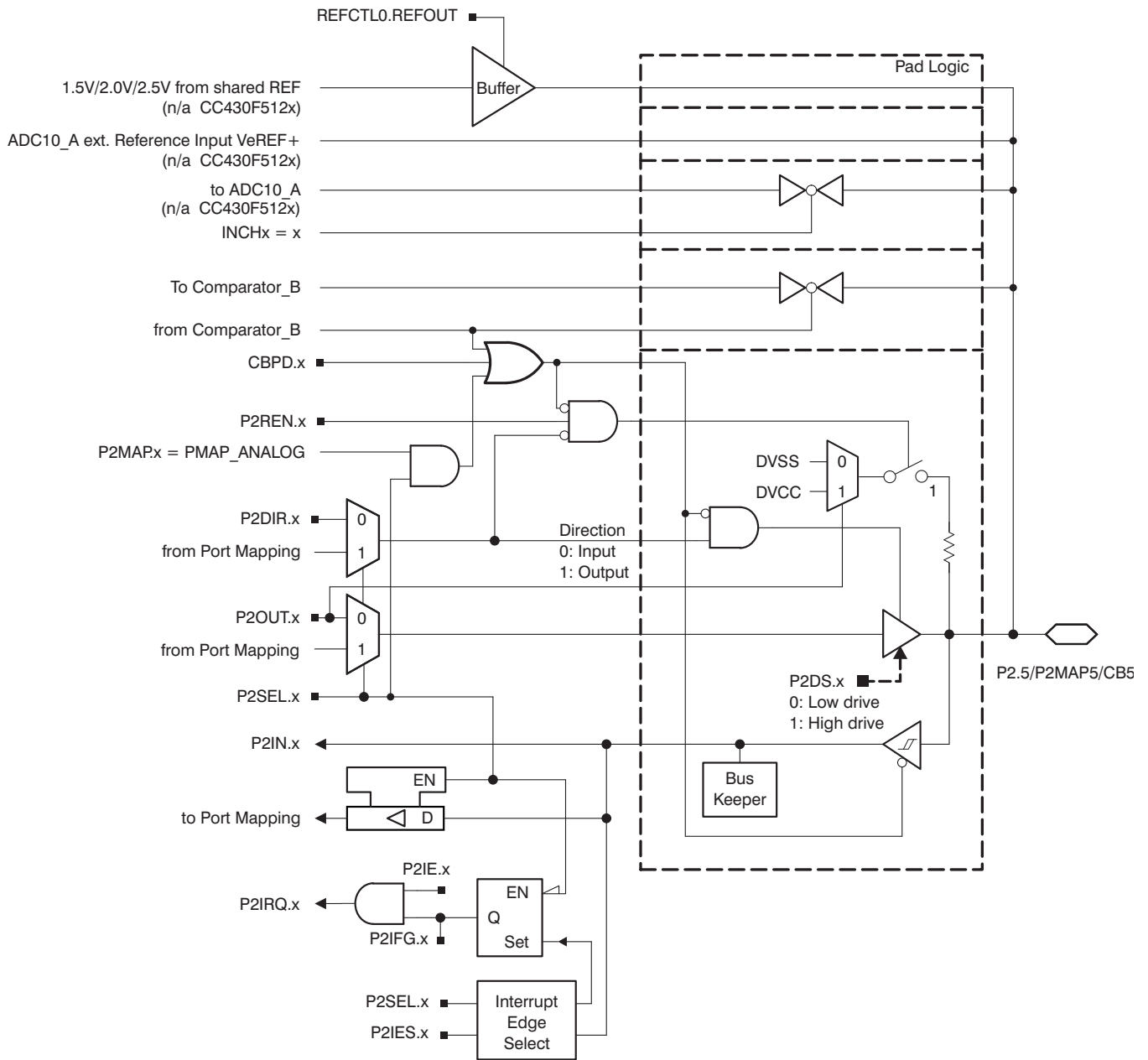
Port P2, P2.0 to P2.3, Input/Output With Schmitt Trigger



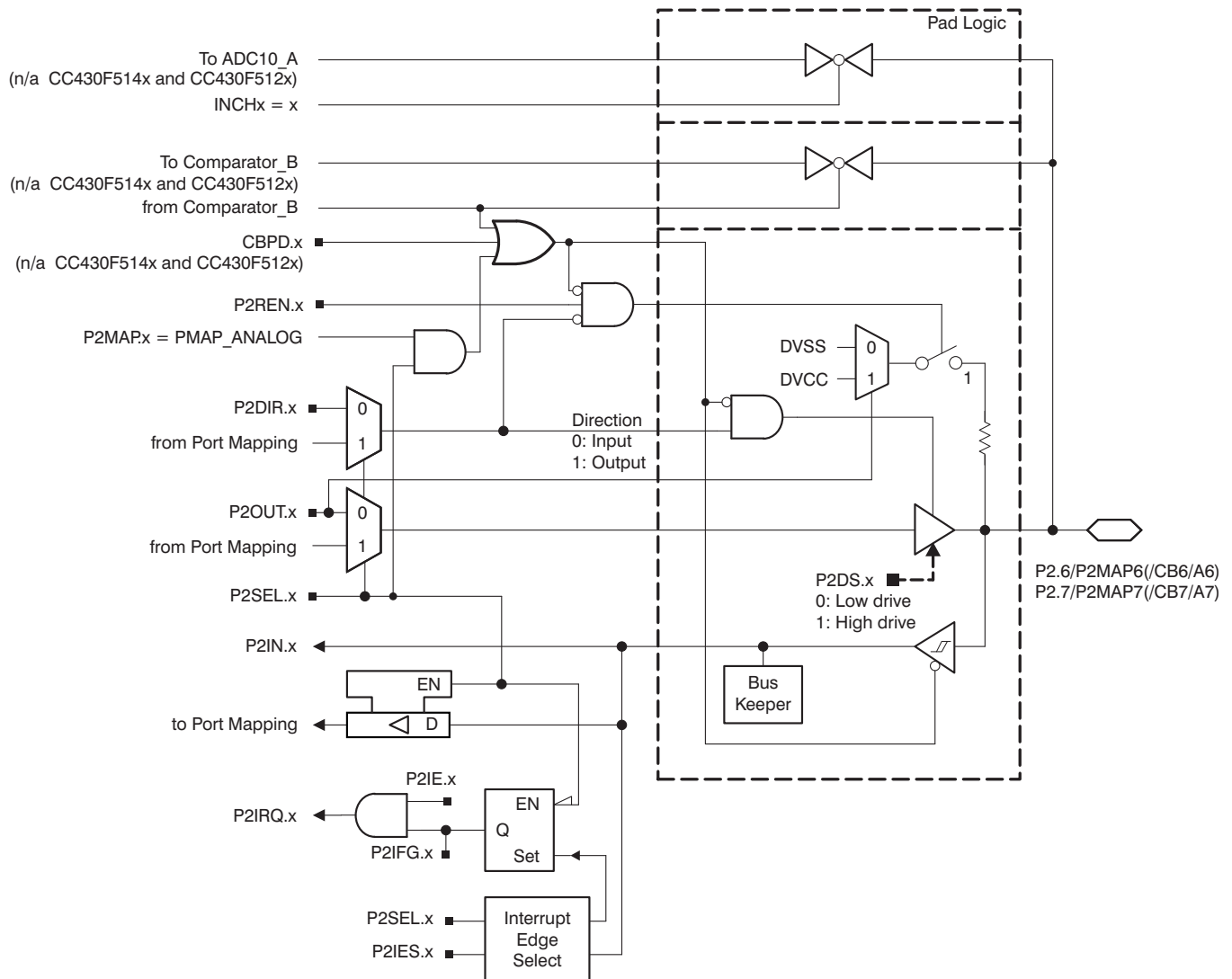
Port P2, P2.4, Input/Output With Schmitt Trigger



Port P2, P2.5, Input/Output With Schmitt Trigger



Port P2, P2.6 and P2.7, Input/Output With Schmitt Trigger



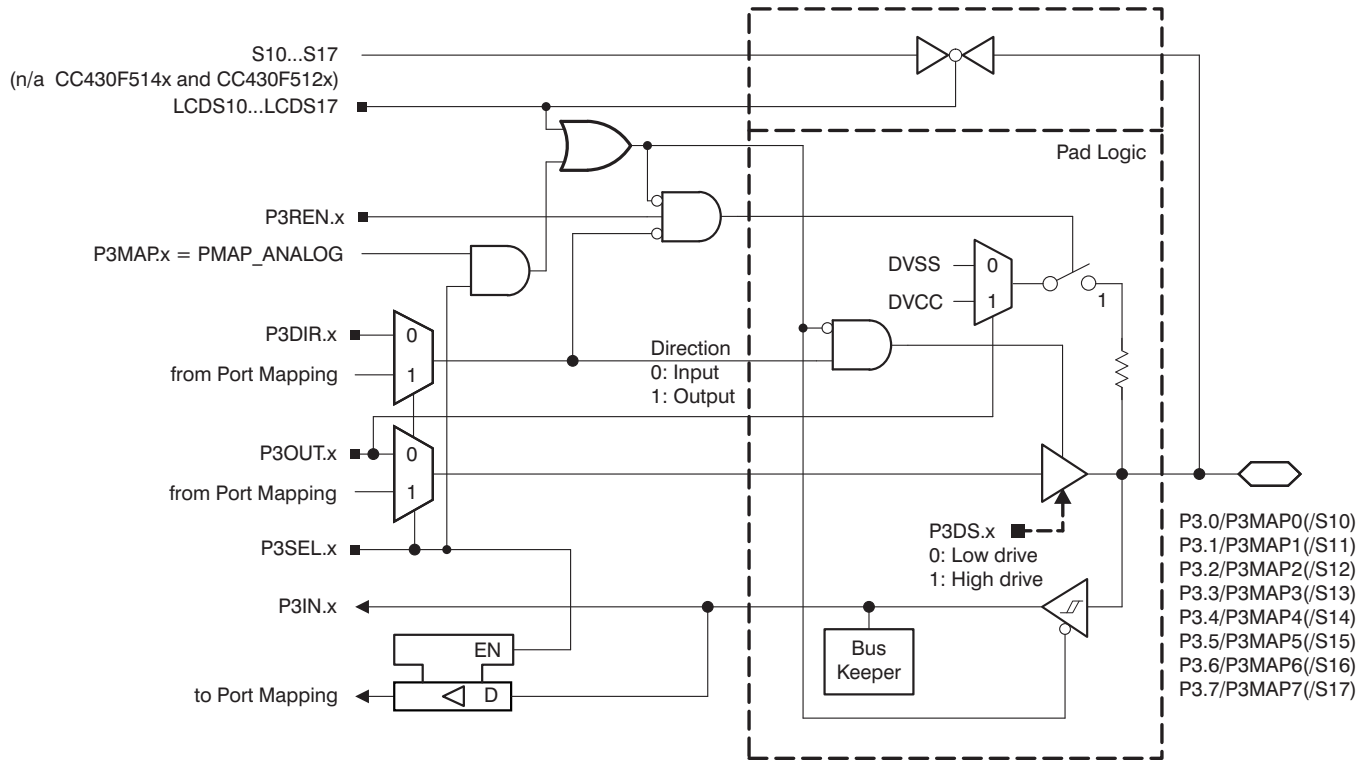
CC430F514x and CC430F512x devices do not provide analog functionality on port P2.6 and P2.7 pins.

Table 52. Port P2 (P2.0 to P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | | |
|---------------------------------------|---|---|----------------------|---------|---------------------|--------|
| | | | P2DIR.x | P2SEL.x | P2MAPx | CBPD.x |
| P2.0/P2MAP0/CB0 (/A0) | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ | 0 |
| | | A0 (not available on CC430F512x) ⁽²⁾ | X | 1 | = 31 | X |
| | | CB0 ⁽³⁾ | X | X | X | 1 |
| P2.1/P2MAP1/CB1 (/A1) | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ | 0 |
| | | A1 (not available on CC430F512x) ⁽²⁾ | X | 1 | = 31 | X |
| | | CB1 ⁽³⁾ | X | X | X | 1 |
| P2.2/P2MAP2/CB2 (/A2) | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ | 0 |
| | | A2 (not available on CC430F512x) ⁽²⁾ | X | 1 | = 31 | X |
| | | CB2 ⁽³⁾ | X | X | X | 1 |
| P2.3/P2MAP3/CB3 (/A3) | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ | 0 |
| | | A3 (not available on CC430F512x) ⁽²⁾ | X | 1 | = 31 | X |
| | | CB3 ⁽³⁾ | X | X | X | 1 |
| P2.4/P2MAP4/CB4 (/A4/VeREF-) | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ | 0 |
| | | A4/VeREF- (not available on CC430F512x) ⁽²⁾ | X | 1 | = 31 | X |
| | | CB4 ⁽³⁾ | X | X | X | 1 |
| P2.5/P2MAP5/CB5 (/A5/VREF+/VeREF+) | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ | 0 |
| | | A5/VREF+VeREF+ (not available on CC430F512x) ⁽²⁾ | X | 1 | = 31 | X |
| | | CB5 ⁽³⁾ | X | X | X | 1 |
| P2.6/P2MAP6/(CB6) (/A6) | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ | 0 |
| | | A6 (not available on CC430F514x and CC430F512x) ⁽²⁾ | X | 1 | = 31 | X |
| | | CB6 (not available on CC430F514x and CC430F512x) ⁽³⁾ | X | X | X | 1 |
| P2.7/P2MAP7/(CB7) (/A7) | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽¹⁾ | 1 | ≤ 30 ⁽¹⁾ | 0 |
| | | A7 (not available on CC430F514x and CC430F512x) ⁽²⁾ | X | 1 | = 31 | X |
| | | CB7 (not available on CC430F514x and CC430F512x) ⁽³⁾ | X | X | X | 1 |

- (1) According to mapped function (see Table 10)
- (2) Setting P2SEL.x bit together with P2MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger.
- (3) Setting the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger



CC430F514x and CC430F512x devices do not provide LCD functionality.

Table 53. Port P3 (P3.0 to P3.7) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | | |
|-----------------|---|---|----------------------|---------|---------------------|--------------------------------|
| | | | P3DIR.x | P3SEL.x | P3MAPx | LCDS10... 17 ⁽¹⁾ |
| P3.0/P3MAP0/S10 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S10 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P3.1/P3MAP1/S11 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S11 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P3.2/P3MAP7/S12 | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S12 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P3.3/P3MAP3/S13 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S13 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P3.4/P3MAP4/S14 | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S14 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P3.5/P3MAP5/S15 | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S15 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P3.6/P3MAP6/S16 | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S16 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |
| P3.7/P3MAP7/S17 | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | Mapped secondary digital function (see Table 10) | 0; 1 ⁽²⁾ | 1 | ≤ 30 ⁽²⁾ | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S17 (not available on CC430F514x and CC430F512x) | X | X | X | 1 |

(1) LCDSx not available in CC430F514x and CC430F512x.

(2) According to mapped function (see [Table 10](#))

Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger (CC430F614x only)

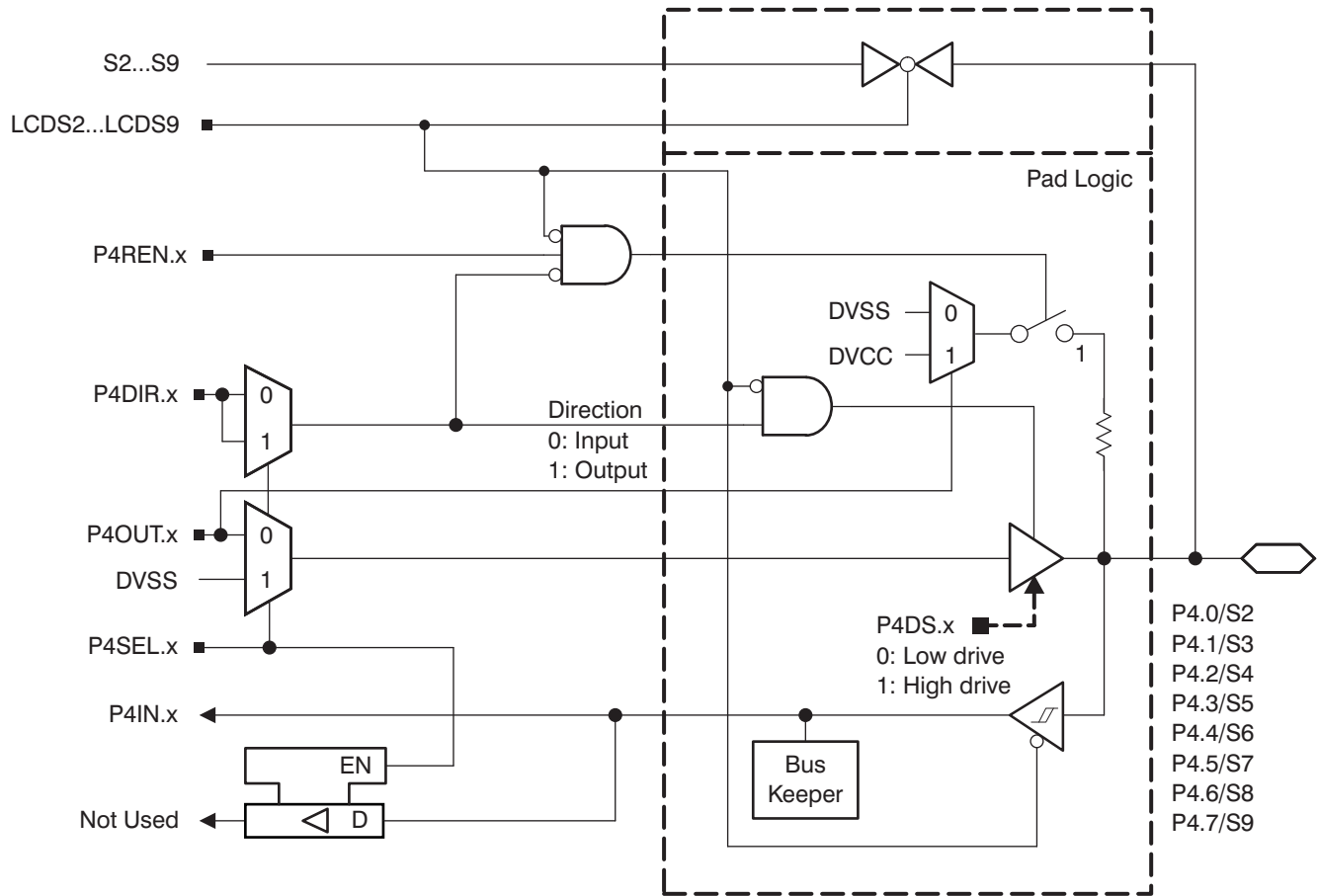
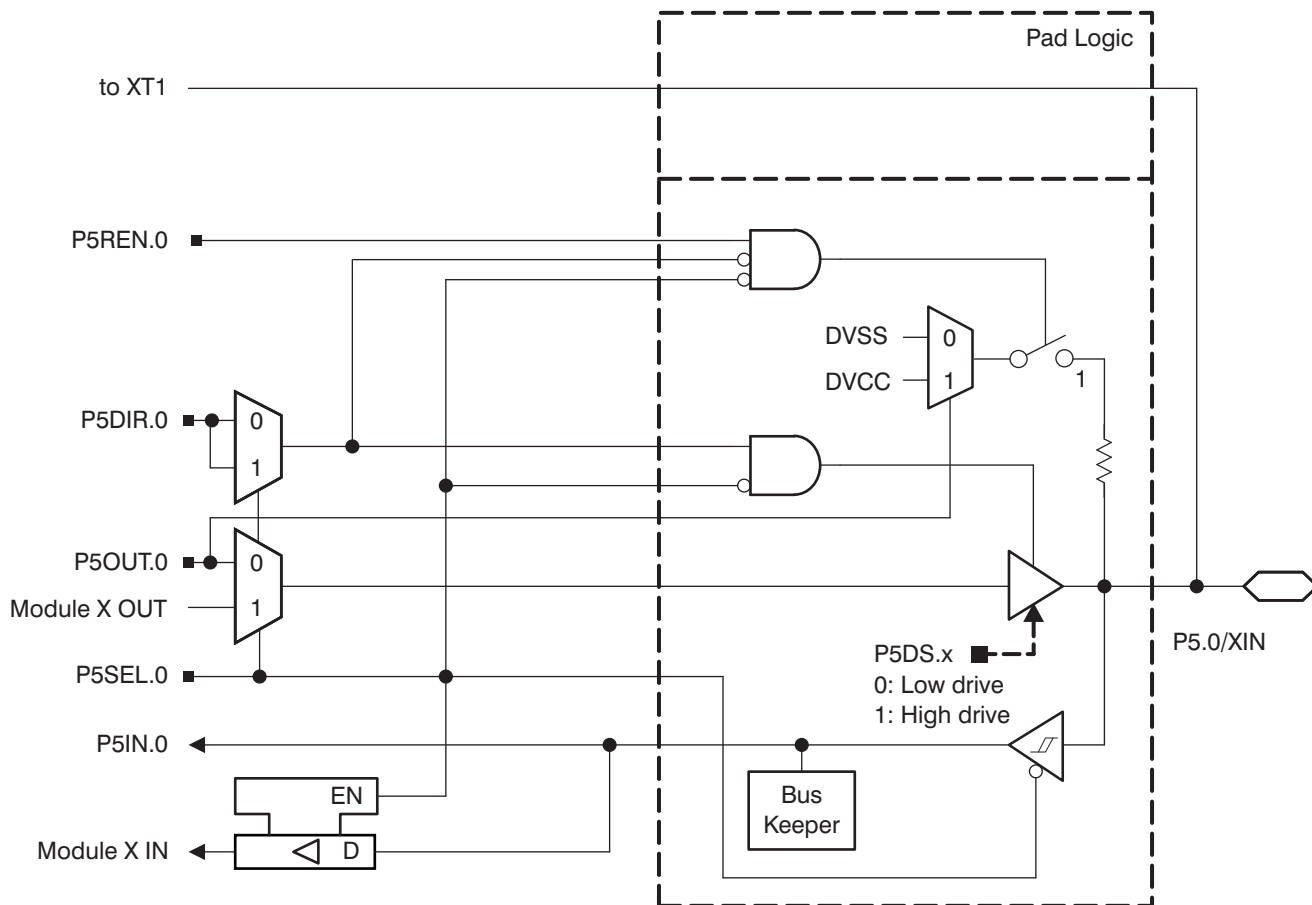


Table 54. Port P4 (P4.0 to P4.7) Pin Functions (CC430F614x only)

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|-----------------|---|------------|----------------------|---------|-----------|
| | | | P4DIR.x | P4SEL.x | LCDS2...7 |
| P4.0/P4MAP0/S2 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S2 | X | X | 1 |
| P4.1/P4MAP1/S3 | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S3 | X | X | 1 |
| P4.2/P4MAP7/S4 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S4 | X | X | 1 |
| P4.3/P4MAP3/S5 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S5 | X | X | 1 |
| P4.4/P4MAP4/S6 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S6 | X | X | 1 |
| P4.5/P4MAP5/S7 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S7 | X | X | 1 |
| P4.6/P4MAP6/S8 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S8 | X | X | 1 |
| P4.7/P4MAP7/S9 | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S9 | X | X | 1 |

Port P5, P5.0, Input/Output With Schmitt Trigger



Port P5, P5.1, Input/Output With Schmitt Trigger

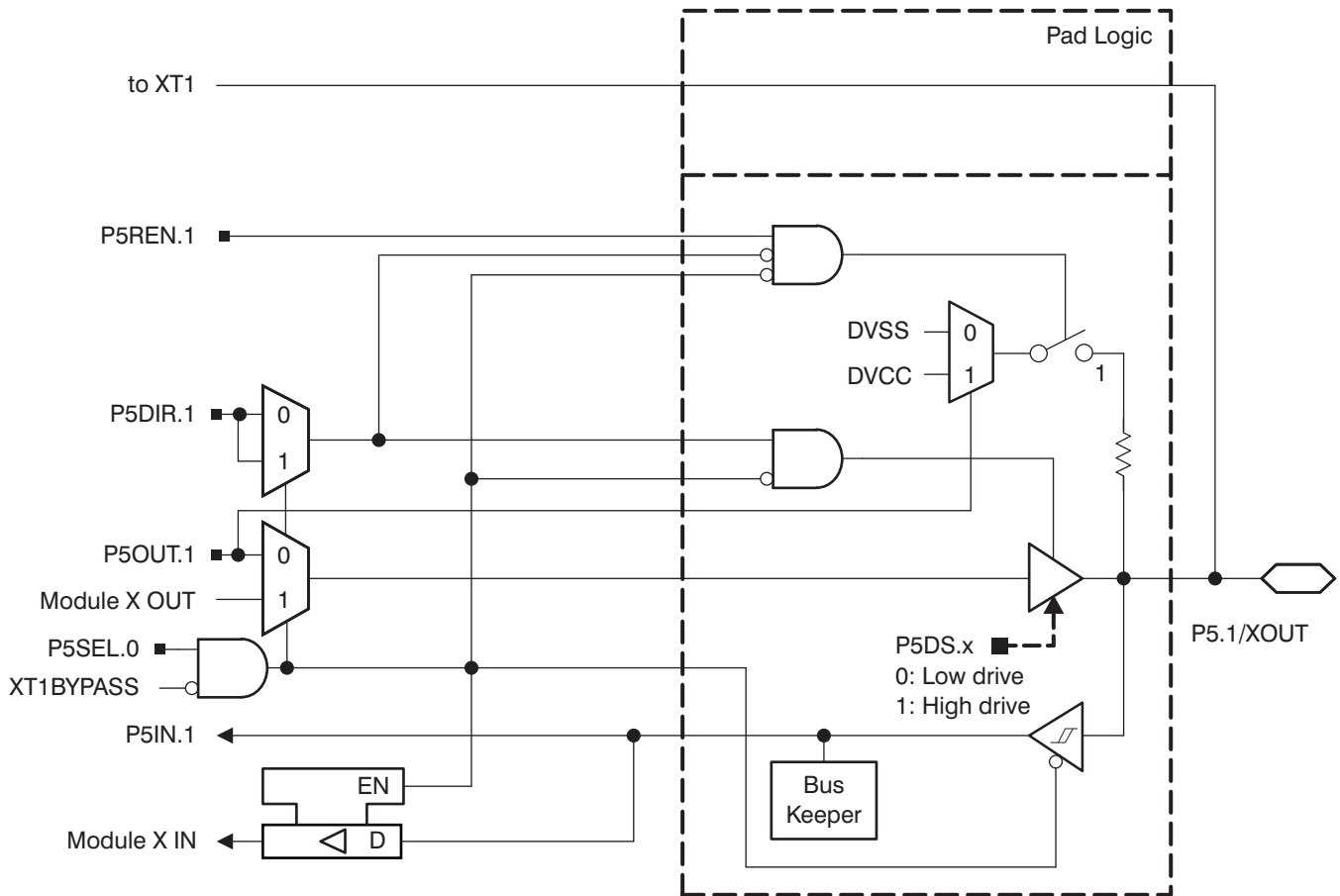


Table 55. Port P5 (P5.0 and P5.1) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS/SIGNALS ⁽¹⁾ | | | |
|-----------------|---|----------------------------------|-------------------------------------|---------|---------|-----------|
| | | | P5DIR.x | P5SEL.0 | P5SEL.1 | XT1BYPASS |
| P5.0/XIN | 0 | P5.0 (I/O) | I: 0; O: 1 | 0 | X | X |
| | | XIN crystal mode ⁽²⁾ | X | 1 | X | 0 |
| | | XIN bypass mode ⁽²⁾ | X | 1 | X | 1 |
| P5.1/XOUT | 1 | P5.1 (I/O) | I: 0; O: 1 | 0 | X | X |
| | | XOUT crystal mode ⁽³⁾ | X | 1 | X | 0 |
| | | P5.1 (I/O) ⁽³⁾ | X | 1 | X | 1 |

(1) X = Don't care

(2) Setting P5SEL.0 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.0 is configured for crystal mode or bypass mode.

(3) Setting P5SEL.0 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.1 can be used as general-purpose I/O.

Port P5, P5.2 to P5.4, Input/Output With Schmitt Trigger (CC430F614x only)

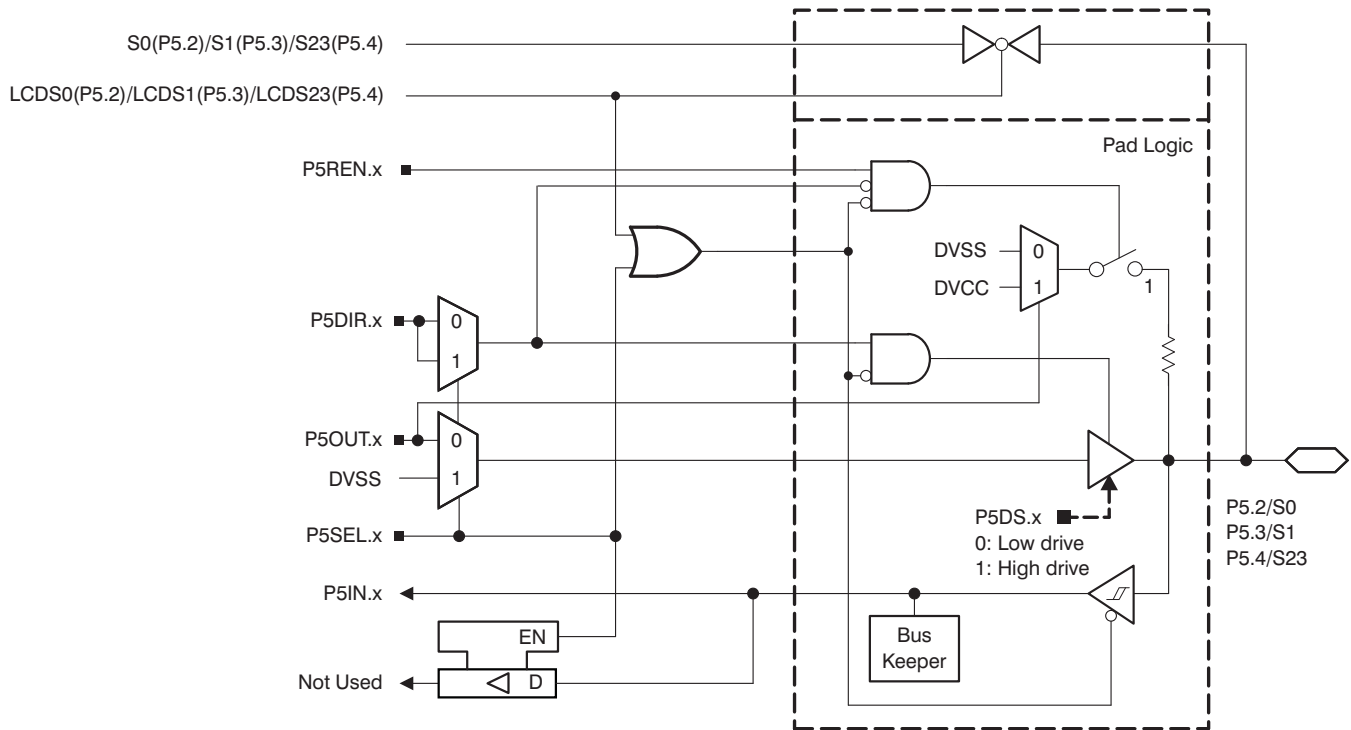


Table 56. Port P5 (P5.2 to P5.3) Pin Functions (CC430F614x only)

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|-----------------|---|------------|----------------------|---------|-----------|
| | | | P5DIR.x | P5SEL.x | LCDS0...1 |
| P5.2/S0 | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S0 | X | X | 1 |
| P5.3/S1 | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S1 | X | X | 1 |

Table 57. Port P5 (P5.4) Pin Functions (CC430F614x only)

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|-----------------|---|------------|----------------------|---------|--------|
| | | | P5DIR.x | P5SEL.x | LCDS23 |
| P5.4/S23 | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S23 | X | X | 1 |

Port P5, P5.5 to P5.7, Input/Output With Schmitt Trigger (CC430F614x only)

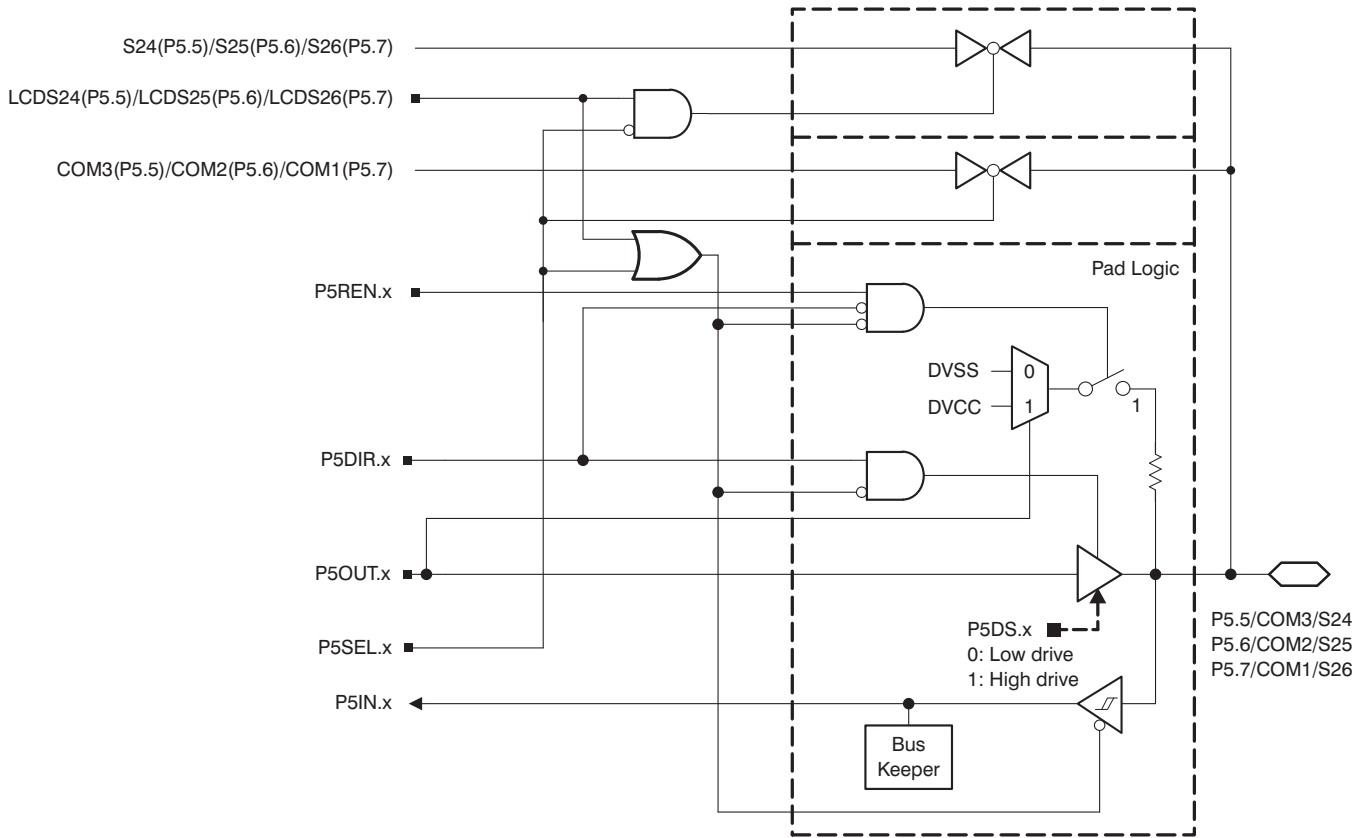
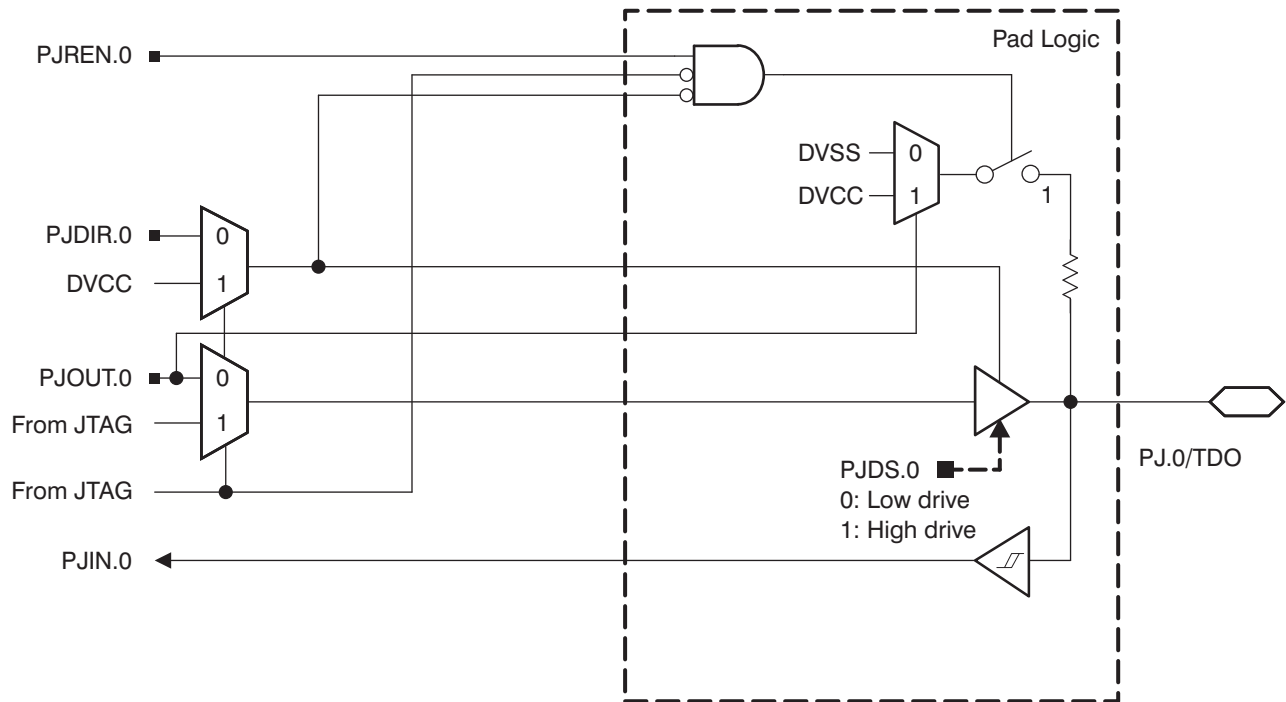


Table 58. Port P5 (P5.5 to P5.7) Pin Functions (CC430F614x only)

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|-----------------|---|---------------------|----------------------|---------|------------------|
| | | | P5DIR.x | P5SEL.x | LCDS24 to LCDS26 |
| P5.5/COM3/S24 | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | COM3 ⁽¹⁾ | X | 1 | X |
| | | S24 ⁽¹⁾ | X | 0 | 1 |
| P5.6/COM2/S25 | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | COM2 ⁽¹⁾ | X | 1 | X |
| | | S25 ⁽¹⁾ | X | 0 | 1 |
| P5.7/COM1/S26 | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | COM1 ⁽¹⁾ | X | 1 | X |
| | | S26 ⁽¹⁾ | X | 0 | 1 |

(1) Setting P5SEL.x bit disables the output driver and the input Schmitt trigger.

Port J, J.0 JTAG pin TDO, Input/Output With Schmitt Trigger or Output



Port J, J.1 to J.3 JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

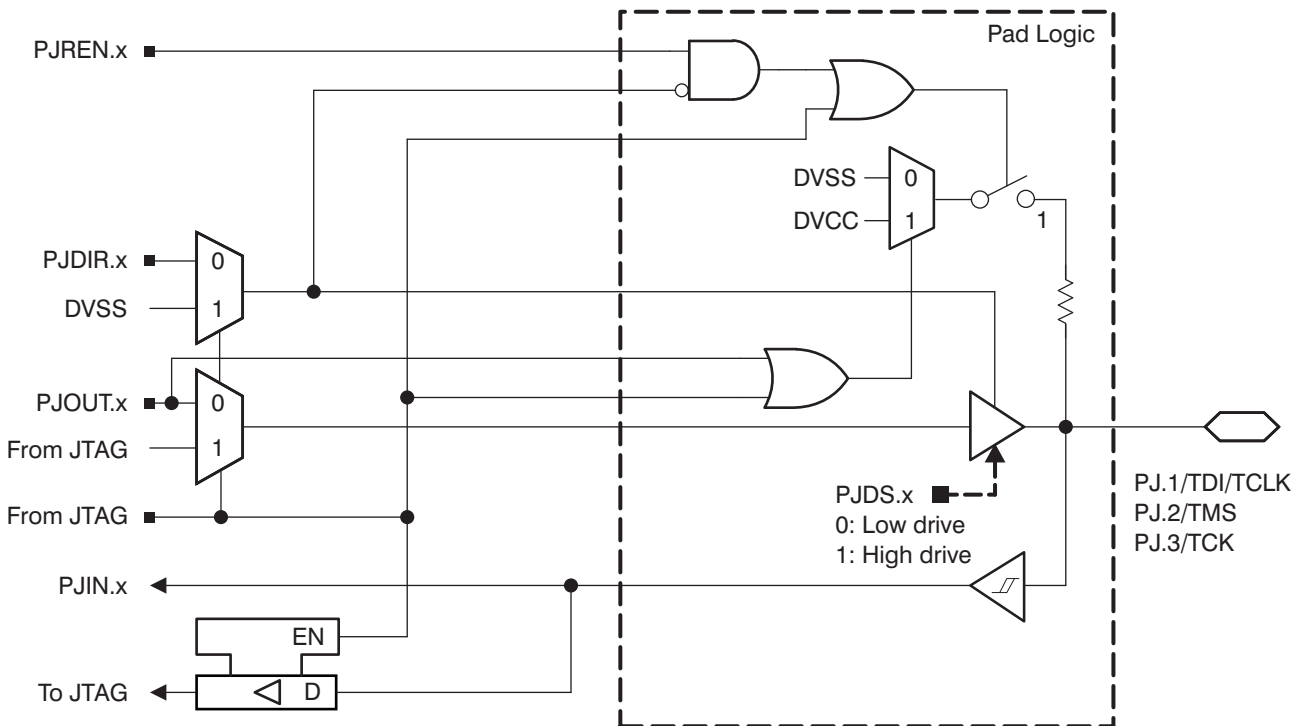


Table 59. Port PJ (PJ.0 to PJ.3) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS/ SIGNALS ⁽¹⁾ |
|-----------------|---|-----------------------------|---|
| | | | PJDIR.x |
| PJ.0/TDO | 0 | PJ.0 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TDO ⁽³⁾ | X |
| PJ.1/TDI/TCLK | 1 | PJ.1 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TDI/TCLK ^{(3) (4)} | X |
| PJ.2/TMS | 2 | PJ.2 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TMS ^{(3) (4)} | X |
| PJ.3/TCK | 3 | PJ.3 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TCK ^{(3) (4)} | X |

- (1) X = Don't care
- (2) Default condition
- (3) The pin direction is controlled by the JTAG module.
- (4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

Device Descriptor Structures

Table 60 lists the content of the device descriptor tag-length-value (TLV) structure for CC430F614x and CC430F514x device types.

Table 61 lists the content of the device descriptor tag-length-value (TLV) structure for CC430F512x device types.

Table 60. Device Descriptor Table CC430F614x and CC430F514x

| | Description | Address | Size bytes | F6147 | F6145 | F6143 | F5147 | F5145 | F5143 |
|--------------------------|--------------------------------------|---------|------------|----------|----------|----------|----------|----------|----------|
| | | | | Value | Value | Value | Value | Value | Value |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 1 | 035h | 036h | 037h | 038h | 039h | 03Ah |
| | Device ID | 01A05h | 1 | 081h | 081h | 081h | 081h | 081h | 081h |
| | Hardware revision | 01A06h | 1 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Firmware revision | 01A07h | 1 | per unit | per unit | per unit | per unit | per unit | per unit |
| Die Record | Die Record Tag | 01A08h | 1 | 08h | 08h | 08h | 08h | 08h | 08h |
| | Die Record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/Wafer ID | 01A0Ah | 4 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | Test results | 01A12h | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| ADC10 Calibration | ADC10 Calibration Tag | 01A14h | 1 | 13h | 13h | 13h | 13h | 13h | 13h |
| | ADC10 Calibration length | 01A15h | 1 | 10h | 10h | 10h | 10h | 10h | 10h |
| | ADC Gain Factor | 01A16h | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC Offset | 01A18h | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 1.5V Reference Temp. Sensor 30°C | 01A1Ah | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 1.5V Reference Temp. Sensor 85°C | 01A1Ch | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.0V Reference Temp. Sensor 30°C | 01A1Eh | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.0V Reference Temp. Sensor 85°C | 01A20h | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.5V Reference Temp. Sensor 30°C | 01A22h | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | ADC 2.5V Reference Temp. Sensor 85°C | 01A24h | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| REF Calibration | REF Calibration Tag | 01A26h | 1 | 12h | 12h | 12h | 12h | 12h | 12h |
| | REF Calibration length | 01A27h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |

Table 60. Device Descriptor Table CC430F614x and CC430F514x (continued)

| | Description | Address | Size bytes | F6147 | F6145 | F6143 | F5147 | F5145 | F5143 |
|----------------------------|------------------------------|---------|------------|----------|----------|----------|----------|----------|----------|
| | | | | Value | Value | Value | Value | Value | Value |
| | 1.5V Reference Factor | 01A28h | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | 2.0V Reference Factor | 01A2Ah | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| | 2.5V Reference Factor | 01A2Ch | 2 | per unit | per unit | per unit | per unit | per unit | per unit |
| Peripheral Descriptor (PD) | Peripheral Descriptor Tag | 01A2Eh | 1 | 02h | 02h | 02h | 02h | 02h | 02h |
| | Peripheral Descriptor Length | 01A2Fh | 1 | 5Dh | 5Dh | 5Dh | 5Bh | 5Bh | 5Bh |
| | Peripheral Descriptors | 01A30h | PD Length | ... | ... | ... | ... | ... | ... |

Table 61. Device Descriptor Table CC430F512x

| | Description | Address | Size bytes | F5125 | F5123 |
|----------------------------|------------------------------|---------|------------|-----------|-----------|
| | | | | Value | Value |
| Info Block | Info length | 01A00h | 1 | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h |
| | CRC value | 01A02h | 2 | per unit | per unit |
| | Device ID | 01A04h | 1 | 03Bh | 03Ch |
| | Device ID | 01A05h | 1 | 081h | 081h |
| | Hardware revision | 01A06h | 1 | per unit | per unit |
| | Firmware revision | 01A07h | 1 | per unit | per unit |
| Die Record | Die Record Tag | 01A08h | 1 | 08h | 08h |
| | Die Record length | 01A09h | 1 | 0Ah | 0Ah |
| | Lot/Wafer ID | 01A0Ah | 4 | per unit | per unit |
| | Die X position | 01A0Eh | 2 | per unit | per unit |
| | Die Y position | 01A10h | 2 | per unit | per unit |
| | Test results | 01A12h | 2 | per unit | per unit |
| Empty Descriptor | Empty Tag | 01A14h | 1 | 05h | 05h |
| | Empty Tag length | 01A15h | 1 | 10h | 10h |
| | | 01A16h | 16 | undefined | undefined |
| | ADC Offset | 01A18h | 2 | per unit | per unit |
| REF Calibration | REF Calibration Tag | 01A26h | 1 | 12h | 12h |
| | REF Calibration length | 01A27h | 1 | 06h | 06h |
| | 1.5V Reference Factor | 01A28h | 2 | per unit | per unit |
| | 2.0V Reference Factor | 01A2Ah | 2 | per unit | per unit |
| | 2.5V Reference Factor | 01A2Ch | 2 | per unit | per unit |
| Peripheral Descriptor (PD) | Peripheral Descriptor Tag | 01A2Eh | 1 | 02h | 02h |
| | Peripheral Descriptor Length | 01A2Fh | 1 | 59h | 59h |
| | Peripheral Descriptors | 01A30h | PD Length | ... | ... |

REVISION HISTORY

| REVISION | COMMENTS |
|-----------------|-------------------------|
| SLAS555 | Production Data release |

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| CC430F5123IRGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F5123IRGZT | ACTIVE | VQFN | RGZ | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F5125IRGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F5125IRGZT | ACTIVE | VQFN | RGZ | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F5143IRGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F5143IRGZT | ACTIVE | VQFN | RGZ | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F5145IRGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F5145IRGZT | ACTIVE | VQFN | RGZ | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F5147IRGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F5147IRGZT | ACTIVE | VQFN | RGZ | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F6143IRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F6143IRGCT | ACTIVE | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F6145IRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F6145IRGCT | ACTIVE | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F6147IRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| CC430F6147IRGCT | ACTIVE | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGZ (S-PVQFN-N48)

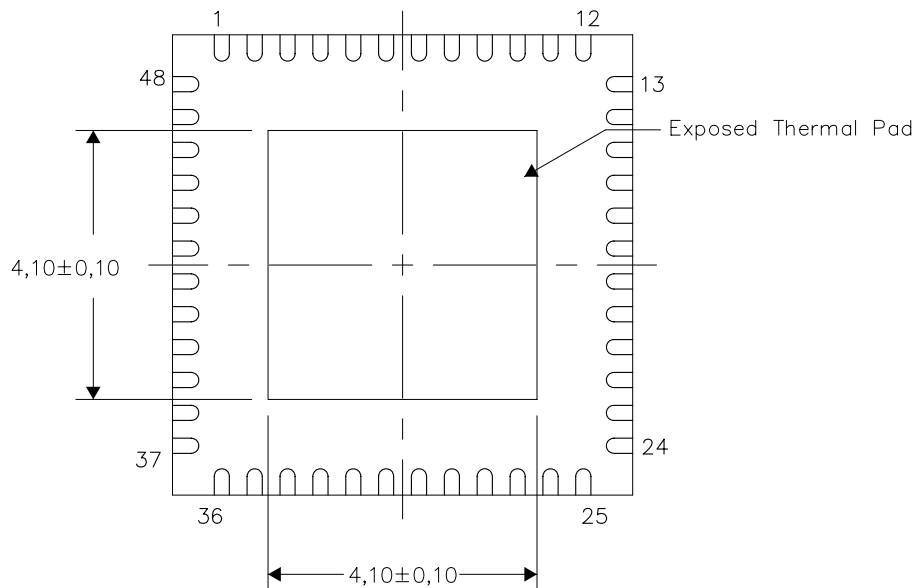
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

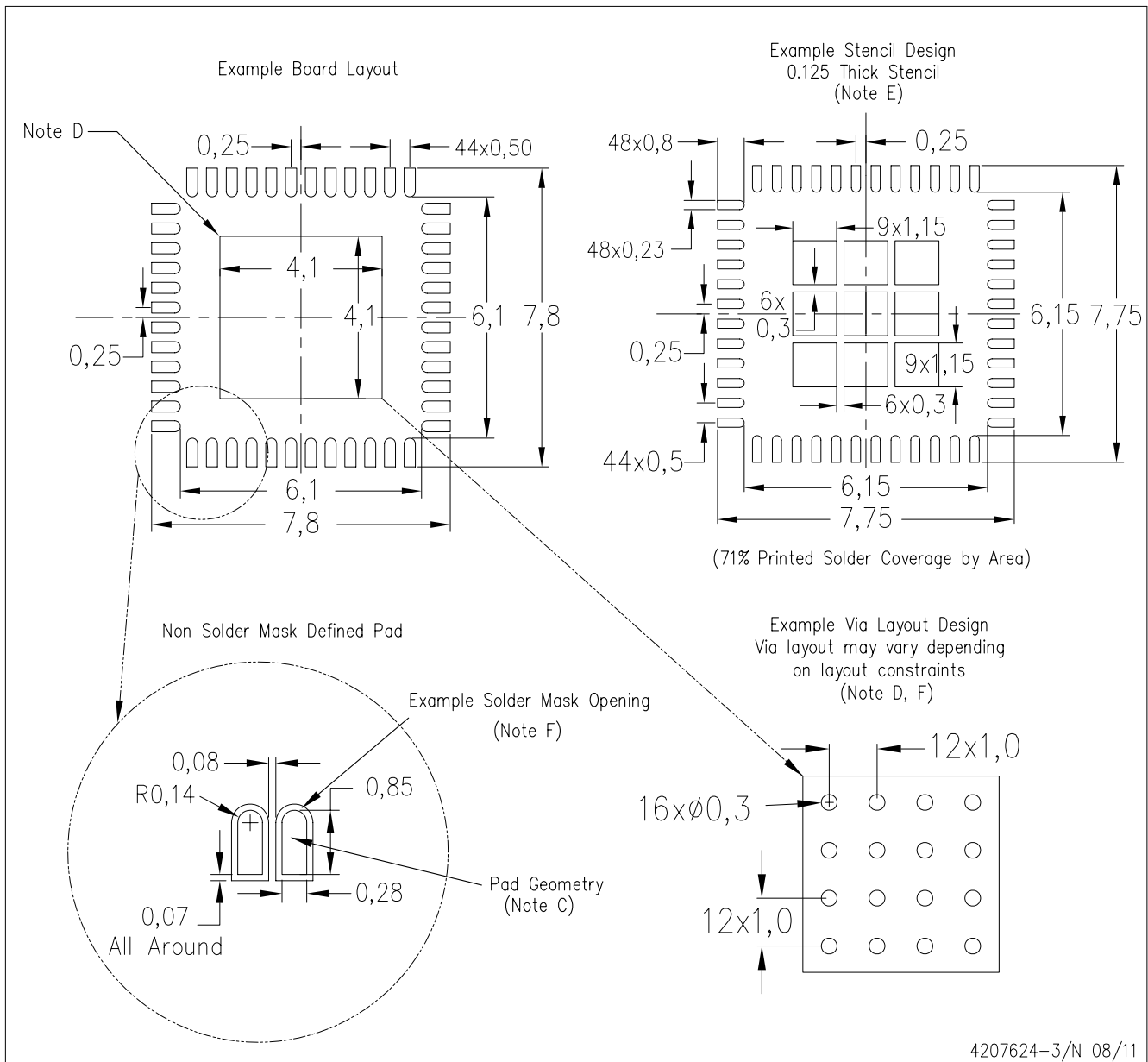
Exposed Thermal Pad Dimensions

4206354-3/R 08/11

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48)

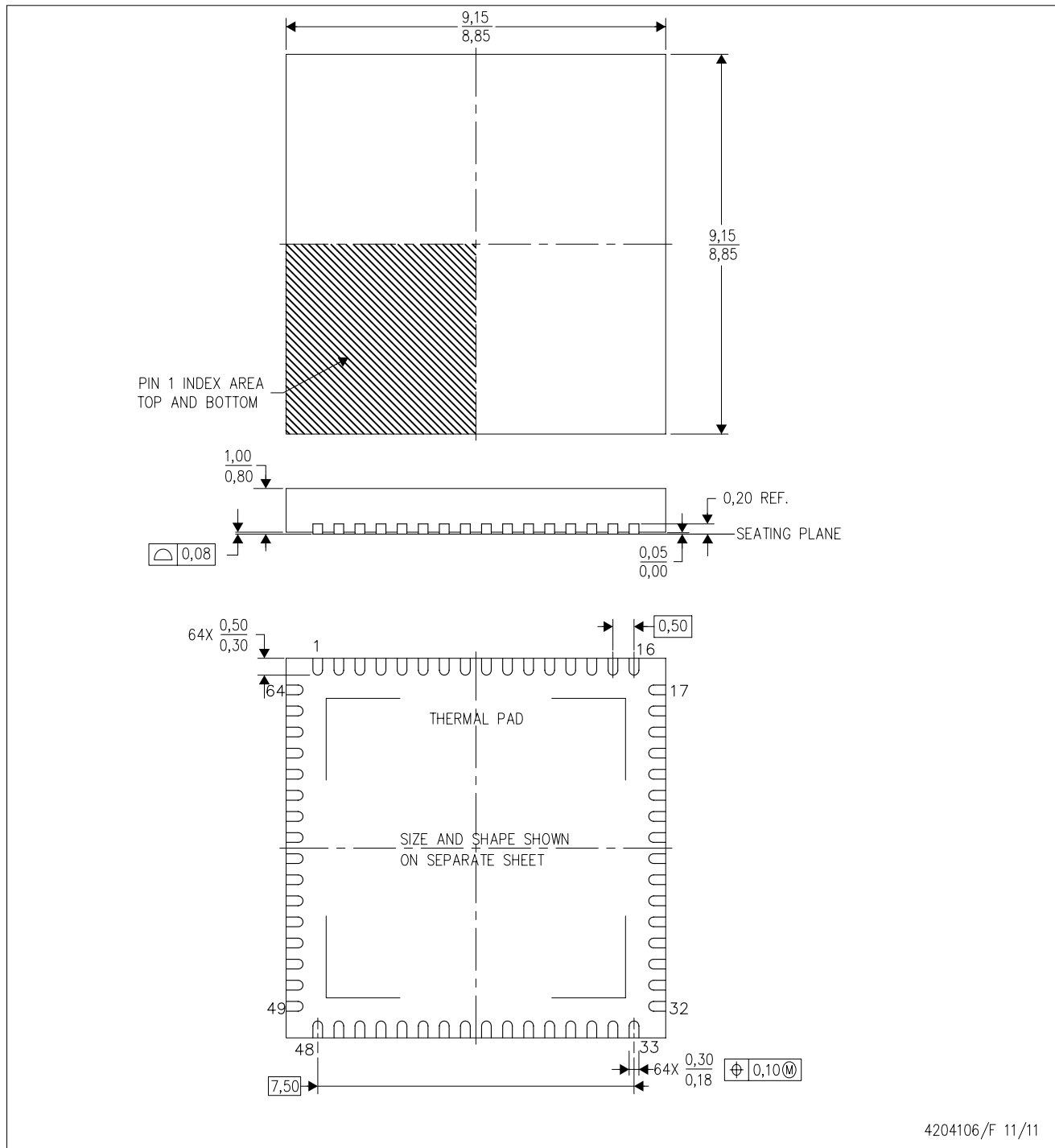
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

MECHANICAL DATA

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RGC (S-PVQFN-N64)

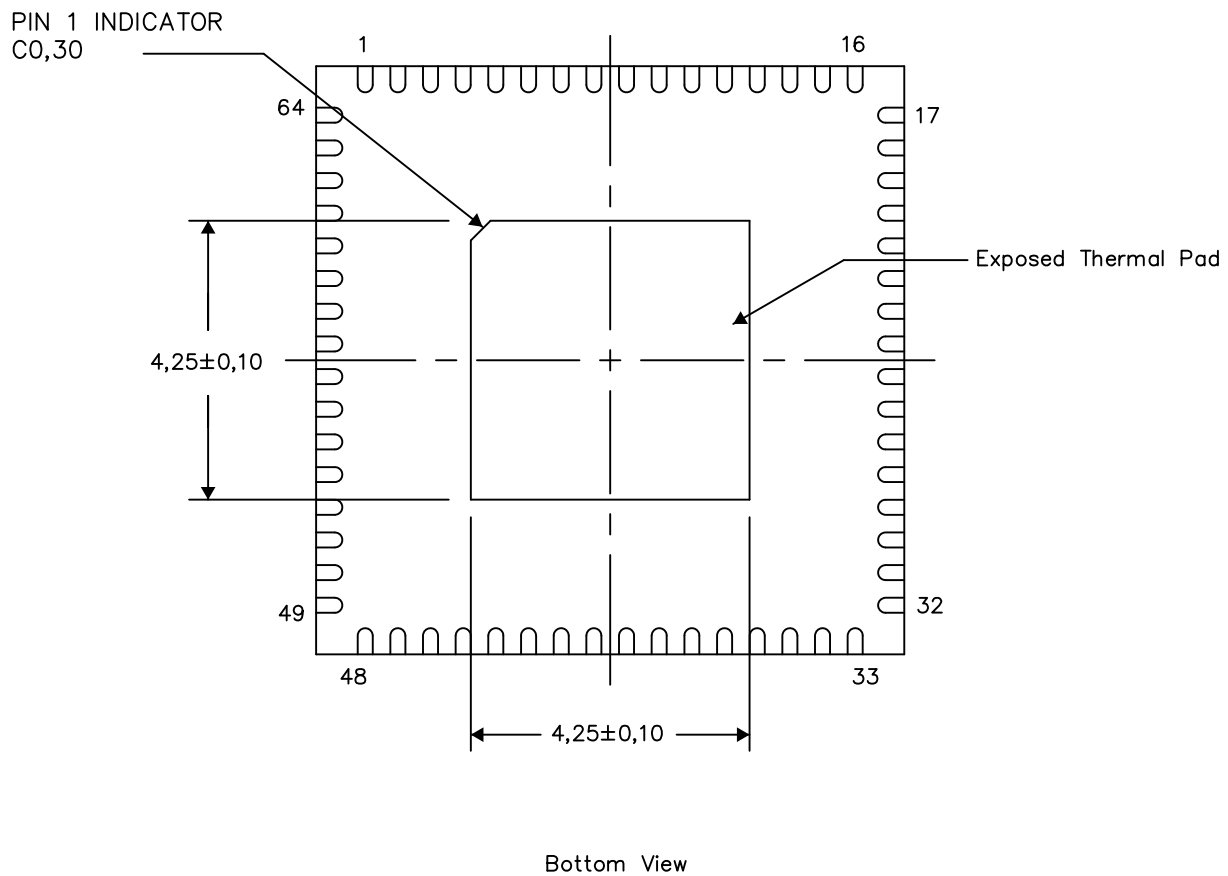
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



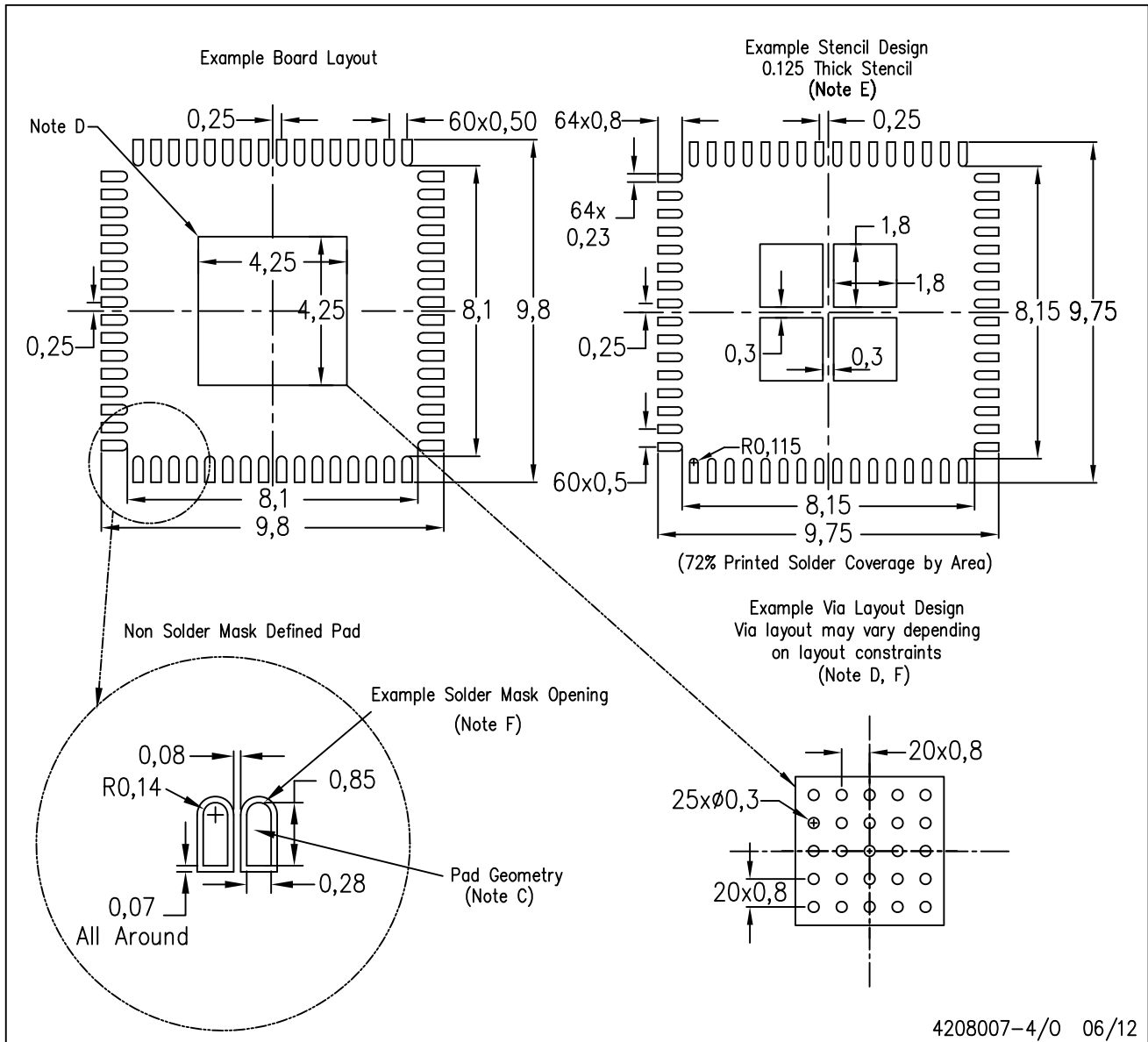
Exposed Thermal Pad Dimensions

4206192-3/S 06/12

NOTE: A. All linear dimensions are in millimeters

RGC (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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