Servo Signal Processors for CD
BU9317K/BU9317KS

The BU9317K and BU9317KS, both single-chip ICs with a double-speed adjustment-free PLL circuit, program servo and signal processing block, are servo signal processors for CD players and are designed for low voltage and low power consumption. These ICs are ideal for compact, low-power-consumption applications.

●Applications

Portable CD players, radio-cassette recorders, mini and component stereos

●Features

1) Internal PLL circuit and bit clock sampling with a minimal number of attached components, for EFM data modulation.
2) Detects and protects frame synchronization signals.
3) Internal servo filters for focusing, tracking and threading. Characteristics are controlled by commands from the controller.
4) Serial output pins for subcodes.
5) Separate output pins for P codes and Q codes.
6) Internal CLV sequencer that automatically sets the CLV mode.
7) Internal track jump sequencer, for jumping to the desired track.
8) Combines the track jump path with tracking error components for output.
9) A single chip with an internal deinterleaving function and channel 1/channel 2 double error detection, correction and flagging processor.
10) Signals to DAC devices are output MSB first through SCOMP serial output, for control of interpolation circuit ON/OFF operations for CD-ROM devices.
11) Internal 16-Kbit SRAM absorbs jitter of up to ±4 frames.
12) Double speed playback.

●Absolute maximum ratings (Ta=25℃)

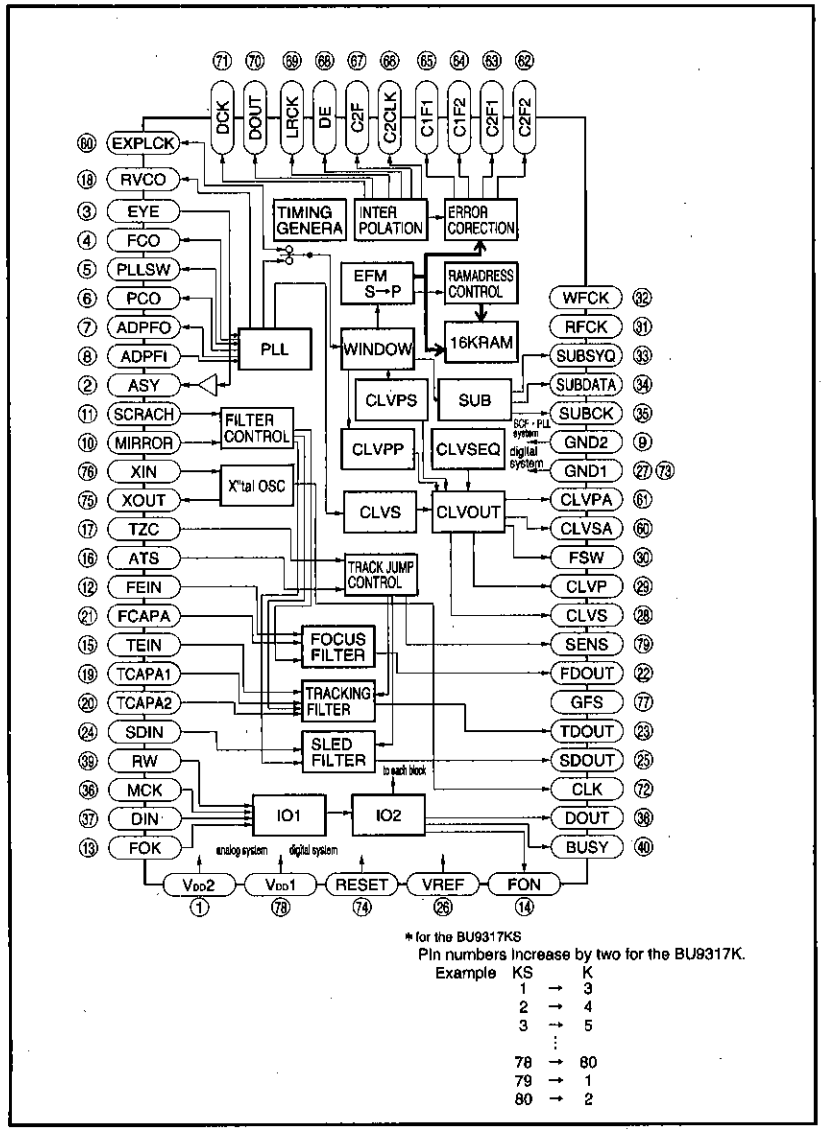
Parameter		Symbol	Limits	Unit
Power supply voltage		Vcc	7	V
Power dissipation	BU9317K	Pd	900*1	mW
	BU9317KS		800*2	
Operating temperature		Topr	−25~75	℃
Storage temperature		Tstg	−55~125	℃

*1. Reduced by 9.0 mW for each increase in Ta of 1℃ over 25℃.
*2. Reduced by 8.0 mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	3.0	—	5.5	V

●Block diagram



* for the BU9317KS
Pin numbers increase by two for the BU9317K.

Example	KS		K
	1	→	3
	2	→	4
	3	→	5
	⋮		
	78	→	80
	79	→	1
	80	→	2

●Pin description

Pin No.	Pin name	Analog/ digital	I/O	Function	input/output cicuit diagram
1 (3)	$V_{DD}2$			PLL servo filter block power supply	
2 (4)	ASY	Digital	O	Output for EFM signal slice level control	Fig.5
3 (5)	EYE	Digital	I	Input of EFM signals from the RF amplifier	Fig.4
4 (6)	FCO	Analog	O	Output of PLL frequency comparison error voltage	Fig.7
5 (7)	PLLSW	Digital	O	PLL time constant switching	Fig.3
6 (8)	PCO	Analog	O	Output of PLL phase comparison error voltage	Fig.7
7 (9)	ADPFO	Analog	O	PLL adding amplifier output	Fig.2
8 (10)	ADPFI	Analog	I	PLL adding amplifier inverted input	Fig.1
9 (11)	GND2			PLL servo filter block ground	
10 (12)	MIRROR	Digital	I	Miller signal input	Fig.4
11 (13)	SCRACH	Digital	I	Scratch signal input	Fig.4
12 (14)	FEIN	Analog	I	Focus error signal input	Fig.1
13 (15)	FOK	Digital	I	Focus OK signal input	Fig.4
14 (16)	FON	Digital	O	Focus ON signal output	Fig.5
15 (17)	TEIN	Analog	I	Tracking error signal input	Fig.1
16 (18)	ATS	Analog	I	Anti-shock detection window comparator input	Fig.1
17 (19)	TZC	Analog	I	Tracking zero cross comparator input	Fig.1
18 (20)	RVCO	Analog	O	PLL VCO free running resistor	Fig.2
19 (21)	TCAPA1	Analog	I/O	Connecting the trackIng servo filter capacitor	Fig.6
20 (22)	TCAPA2	Analog	I/O	Connecting the tracking servo filter capacitor	Fig.6
21 (23)	FCAPA	Analog	I/O	Connecting the focus servo filter capacitor	Fig.6
22 (24)	FDOUT	Analog	O	Focus drive output	Fig.2
23 (25)	TDOUT	Analog	O	Tracking drive output	Fig.2
24 (26)	SDIN	Analog	I	Thread amplifier input	Fig.1
25 (27)	SDOUT	Analog	O	Thread drive output	Fig.2
26 (28)	VREF	Analog	I	Bias voltage input	Fig.6
27 (29)	GND1			Digital ground	
28 (30)	CLVS	Digital	O	Spindle motor drive output and speed control output	Fig.7
29 (31)	CLVP	Digital	O	Spindle motor drive output and output for ?rough? control and phase control	Fig.7
30 (32)	FSW	Digital	O	Spindle motor output and filter time constant switching output	Fig.3
31 (33)	RFCK	Digital	O	Read frame clock output (7.35 kHz crystal)	Fig.5
32 (34)	WFCK	Digital	O	Write frame clock output (7.35 kHz when locked onto crystal)	Fig.5
33 (35)	SUBSYQ	Digital	O	Subcode synchronization S0 + S1 output	Fig.5
34 (36)	SUBDATA	Digital	O	Subcode serial output	Fig.5
35 (37)	SUBCK	Digital	I	Subcode readout clock	Fig.4
36 (38)	MCK	Digital	I	Clock for readout of CPU serial data and sub Q code	Fig.4
37 (39)	DIN	Digital	I	CPU serial data input	Fig.4
38 (40)	DOUT	Digital	O	Serial output of sub Q code and internal status	Fig.7

Pin No.	Pin name	Analog/ digital	I/O	Function	Input/output circuit diagram
39 (41)	RW	Digital	I	Read/write switching and input of the track jump command Data is output from DOUT at "H" and input to DIN at "L"	Fig.4
40 (42)	BUSY	Digital	O	Busy output Linear output of the CLV speed	Fig.5
41~59 (43)~(61)	NC				
60 (62)	CLVPA	Analog	O	Linear output of the CLV phase	Fig.1
61 (63)	CLVSA	Analog	O	Linear output of the CLV speed	Fig.1
62 (64)	C2F2	Digital	O	Channel 2 double error correction flag	Fig.5
63 (65)	C2F1	Digital	O	Channel 2 single error correction flag	Fig.5
64 (66)	C1F2	Digital	O	Channel 1 double error correction flag	Fig.5
65 (67)	C1F1	Digital	O	Channel 1 single error correction flag	Fig.5
66 (68)	C2CLK	Digital	O	Strobe signal (f = 176.4 kHz)	Fig.5
67 (69)	C2F	Digital	O	Corrected state output	Fig.5
68 (70)	DE	Digital	O	Strobe signal (f = 88.2 kHz)	Fig.5
69 (71)	LRCK	Digital	O	Strobe signal (f = 44.1 kHz)	Fig.5
70 (72)	DOUTA	Digital	O	Audio data output (2' SCOMP)	Fig.5
71 (73)	DOCK	Digital	O	DOUTA bit clock (f = 2.1168 MHz)	Fig.5
72 (74)	CLK	Digital	O	Clock output (one of four selected with &hE4 command)	Fig.5
73 (75)	GND1			Digital ground	
74 (76)	RESET	Digital	I	Internal circuit reset (pulled up by internal resistor (100kΩ)	Fig.8
75 (77)	XOUT	Digital	O	Crystal oscillator circuit output (f = 16.9 MHz)	Fig.9
76 (78)	XIN	Digital	I	Crystal oscillator circuit input (f = 16.9 MHz)	Fig.9
77 (79)	GFS	Digital	O	GFS monitor output (one of four selected with &hE4 command)	Fig.5
78 (80)	VDD1			Digital power supply	
79 (1)	SENS	Digital	O	Output of status of signal selected with &hE4 command	Fig.5
80 (2)	EXPLCK	Digital	I/O	PLL output and input of playback clock when attached PLL is in use	Fig.10

* BU9317K pin numbers are in parentheses ( ).

●Input/output circuits

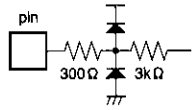


Fig. 1

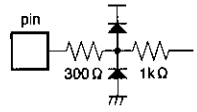


Fig. 2

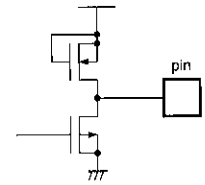


Fig. 3

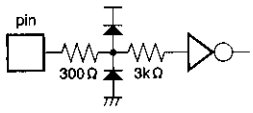


Fig. 4

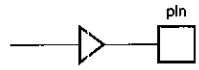


Fig. 5

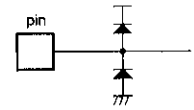


Fig. 6

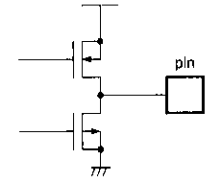


Fig. 7

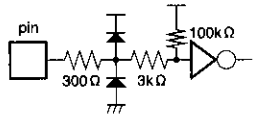


Fig. 8

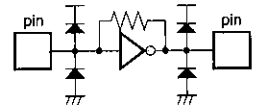


Fig. 9

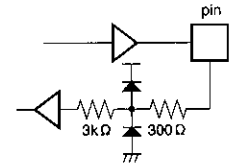


Fig. 10

●Electrical characteristic curves (unless otherwise noted Ta=25℃, V_{DD}=5V) (BU9317KS)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Suitable pins
Input voltage (high level)	V_{IH}	3.5	—	—	V		*1
Input voltage (low level)	V_{IL}	—	—	0.3	V		*1
Output voltage (high level)	V_{OH}	4.0	—	V_{DD}	V	I_{OH}=−1mA	*2
Output voltage (low level)	V_{OL}	0	—	0.4	V	I_{OL}=1mA	*2, 5
Input resistance 1	V_{O1}	80	100	120	kΩ	Between V_{DD1} pins	*3
Input resistance 2	V_{O2}	60	75	90	kΩ	Between bias pins	TZC
Input resistance 3	V_{O3}	180	230	280	kΩ	Between bias pins	ATS
Input resistance 4	V_{O4}	20	25	30	kΩ	Between bias pins	*6
Input leak current	I_{LI}	—	—	±5	μA	V_I=0~5.25V	*1, 2
Output leak current	I_{LO}	—	—	±5	μA	V_O=0~5.25V	*4, 5

Suitable pins

*1 MIRROR, SCRACH, FOK, SUBCK, MCK, DIN, RW, RESET, EXPLCK, EYE

*2 FON, CLVS, CLVP, RFCK, WFCK, SUBSYQ, SUBDATA, DOUT, BUSY, XOUT, SENS, GFS, ASY, C1F1, C1F2, C2F1, C2F2, C2CLK, C2F, DE, LRCK, DOCK, CLK

*3 RESET

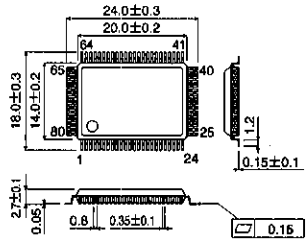
*4 CLVS, CLVP

*5 PLLSW, TCAPA2, FSW

*6 FEIN, TEIN

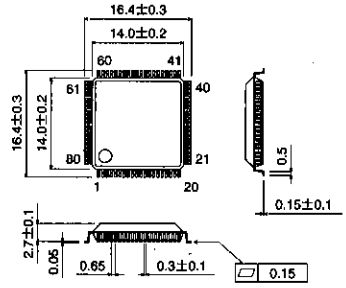
●External dimensions (Units: mm)

BU9317K



QFP80

BU9317KS



SQFP80

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