DTMF receiver for telephones
BU8874/BU8874F

The BU8874 and BU8874F are DTMF receiver ICs developed for use in telephone answering machines, and convert 16 different types of DTMF signals into 4-bit binary serial data. In addition to a compact 8-pin DIP (BU8874) package, these receivers feature a wide dynamic range, eliminating the need for an external input amplifier. Expertise from a number of companies has been incorporated into these products to enable guard time control through a host microcomputer.
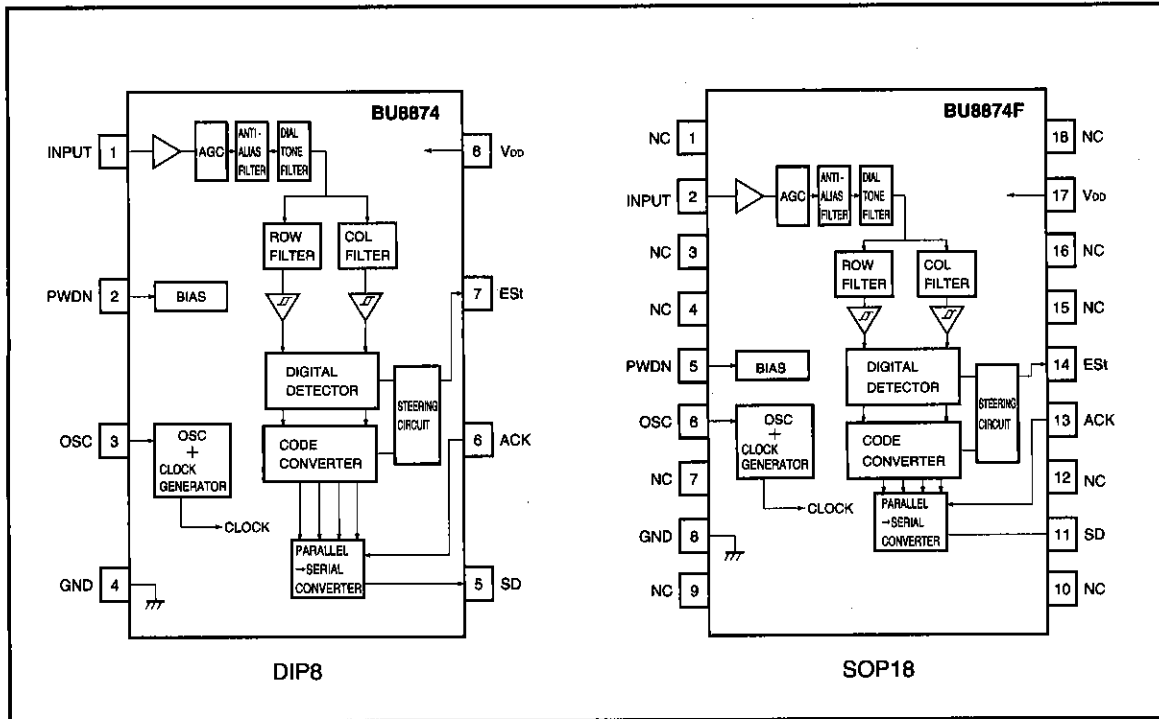
●Applications
Telephone answering machines

●Features
1) Dynamic range of 45dB. (internal AGC)
2) Power down mode.
3) 4-bit binary serial data output.
4) Guard time can be controlled through host micro-computer.
5) Input pins equipped with hysteresis. (ACK pin)

6) 4.19MHz crystal resonator can be used
7) 8-pin DIP package. (BU8874)

●Block diagram

DIP8   SOP18

●Absolute maximum ratings (Ta=25℃)

Parameter		Symbol	Limits	Unit
Power supply voltage		V$_{DD}$	7	V
Input voltage		V$_{IN}$	GND−0.3~V$_{DD}$+0.3	V
Output voltage		V$_{OUT}$	GND−0.3~V$_{DD}$+0.3	V
Power dissipation	BU8874	Pd	500*1	mW
	BU8874F		550*2	
Operating temperature		Topr	−10~70	℃
Storage temperature		Tstg	−55~125	℃

*1 Reduced by 5mW for each increase in Ta of 1℃ over 25℃.

*2 Reduced by 5.5mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	V$_{DD}$	4.75~5.25	V
Oscillation frequency	fosc	4.194304	MHz
Oscillation frequency deviation	Δfosc	−0.1~0.1	%

●Pin description

Pin No. BU8874	Pin No. BU8874F	Pin Name	Function
1	2	INPUT	This is the audio signal input pin, and should be coupled.
2	5	PWDN	Power down signal input pin. "L" level is the normal operation mode. "H" level enters the power down mode and lowers power consumption. When setting this pin to the "H" level, first set the ACK pin to the "L" level.
3	6	OSC	This is the input pin for the internal oscillator. Connect a 4.194304 MHz crystal resonator between this pin and GND, or use input from an external oscillator.
4	8	GND	This is the ground pin.
5	11	SD	This is the serial data output pin. If a series of pulses is input to the ACK pin while the ESt pin is HIGH, the SD output pin outputs a 4-bit binary code corresponding to the DTMF signal shown in Table 1.
6	13	ACK	This is the acknowledgement pulse input pin. It is equipped with hysteresis. After the ESt pin goes HIGH, the four consecutive pulses input to the ACK pin cause the 4-bit data corresponding to the DTMF signal of the SD pin output to be output. The rising edge of the first pulse is latched before the data is shifted.
7	14	EST	This is the steering signal output pin. When there is a valid DTMF signal, this pin goes HIGH.
8	17	V$_{DD}$	This is the power supply pin.
	1,3,4,7 9,10,12 15,16,18	NC	This is the NC pin. It is not connected inside the IC.

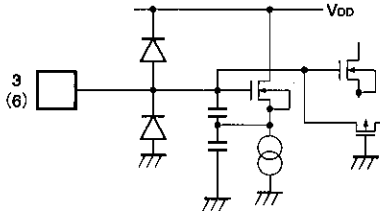● Input/output circuits

INPUT
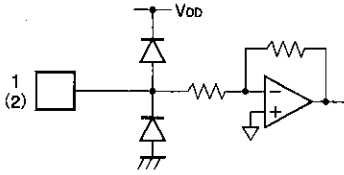
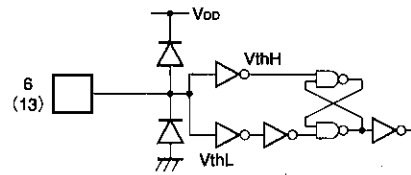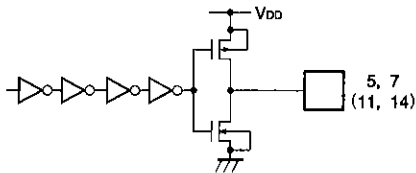

PWDN
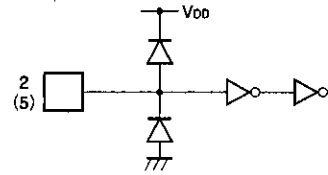
OSC

ACK

SD ESt

DTMF receiver

Telephones

●Electrical characteristics (Unless otherwise noted, Ta=25℃, V_DD=5.0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions	ʋ in (dBm)
Supply current		I_DD	1.0	2.2	3.4	mA	PWDN=GND operation	
PWDN pin input voltage "H"		V_IH2	V_DD+1.0	—	V_DD	V		
PWDN pin input voltage "L"		V_IL2	GND	—	GND+1.0	V		
ACK pin input voltage "H"		V_IH6	V_DD−0.8	—	V_DD	V		
ACK pin input voltage "L"		V_IL6	GND	—	GND+0.8	V		
"H" input current		I_IH	—	0.1	1.0	μA	*1	
"L" input current		I_IL	—	0.1	1.0	μA	*1	
Pin 1 input impedance		Z_IN	10	30	50	kΩ	ʋ in=0dBm, fin=1kHz	
"H" output saturation voltage		V_OH	4.6	—	—	V	I_OH=0.4mA *2	
"L" output saturation voltage		V_OL	—	—	0.4	V	I_OL=1mA *2	
Valid input level range		VIV	−42	—	3	dBm	*3, 4, 5	—
Dual tone level difference	Positive	VTWP	—	—	6	dB	*4	−15
	Negative	VTWN	—	—	6	dB	*4	−15
Frequency detection range		BWA	±1.5%±2Hz	—	—	—	*5	−27
Frequency rejection range		BWR	—	—	±4	%	*5	−27
Third tone tolerance range		TTT	—	—	−16	dB	*5, 6	−27
Noise tolerance range		TN	—	−12	—	dB		−27
Dial tone tolerance range		TDT	—	14	7	dB	*7	−27
Signal presence detection time		tDP	5	12	20	mS		−27
Signal absence detection time		tDA	0.5	5	15	mS		−27
Data shift rate		fDS	—	—	1	MHz	ACK Duty 40%~60%	—
Output delay time		tPAD	—	70	150	nS	ACK→SD	—
Setup time		tDL	0	—	—	nS		—
Hold time		tDH	30	60	—	nS		—

*1 Applies to ACK pin and PWDN pin.

*2 Applies to ESt pin and SD pin.

*3 A DTMF signal is input, and the voltage level of the single tone component is set as VIV.

*4 Specified for a DTMF signal with a frequency deviation at the maximum standard frequency±0.73%

*5 No difference in level between the two tones

*6 Composite signal consisting of DTMF signals and the third harmonics of each input

*7 Specified for signals of 350 Hz and 440 Hz (± 2%)

ROHM

● Circuit operation

1) An overview of operation

A DTMF signal is supplied to the INPUT pin and applied to a pair of 6th-order bandpass filters, which separate the DTMF signal into its high (COL) and low (ROW) frequencies. The separated tonesre converted into square waves and fed to a DIGITAL DETECTOR. The DIGITAL DETECTOR checks the two tones to see if they are within the valid DTMF frequency bands. If they are, it sends a DETECT signal to the STEERING CIRCUIT, and sends the appropriate COLUMN and ROW address signals to a CODE CONVERTER.

The CODE CONVERTER encodes the received and detected DTMF signal, and outputs an ENABLE signal to the STEERING CIRCUIT.

Based on the DETECT and ENABLE signals, the STEERING CIRCUIT outputs an Early Steering (ESt) signal, which sets the ESt pin to HIGH, indicating that a valid DTMF signal has been detected.

If a series of pulses is input at the ACK pin while ESt is HIGH, a decoded DTMF signal is output to the SD pin as a binary code. (See Figure 6 for the overall timing.)

If a pulse sequence is input at the ACK pin, the data is latched at the rising edge of the first pulse by a PARALLEL→SERIAL CONVERTER, and at the same time, the LSB is output from the SD pin. Following this, three bits of data are output from the SD pin for each bit of each pulse in the pulse sequence input from the ACK pin. As a result, a total of four bits of data are output for the four pulses. (See Figure 5 for the ACK and SD timing.)

If the pulse sequence input to the ACK pin consists of three or fewer pulses, the next DTMF input cannot be decoded properly. Any ACK pulses in excess of four are ignored until ESt goes HIGH again. Table 1 shows the format of serial data output from the SD pin.
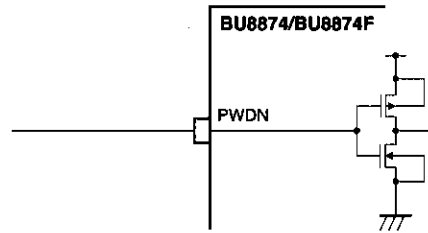
2) Power down interface

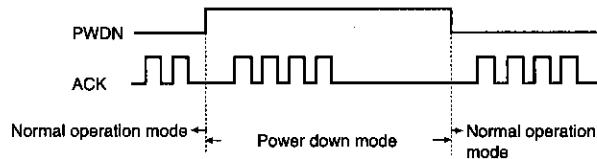Fig. 1 PWDN input circuit

Fig. 2 Power down timing chart

The power down mode is activated by applying a rising edge at the PWDN pin when the ACK pin is LOW. The ACK pin may be taken from LOW to HIGH and back to LOW again while the circuit is in the power down mode.

To return to the normal operation mode, set PWDN to LOW. After returning from the power down mode to the normal operation mode, if a valid DTMF signal is still being held (from prior to entering the power down mode), a second reading of the data can be performed (the first reading following recovery to the normal operation mode) by inputting the ACK pulse sequence. Figure 3 shows this status.
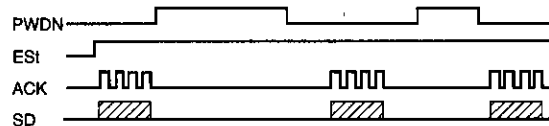

Fig. 3 SD multiple reading operation

If the circuit enters the power down mode n times, data can be read (n + 1) times (while ESt is HIGH), as long as input of the DTMF signal continues.
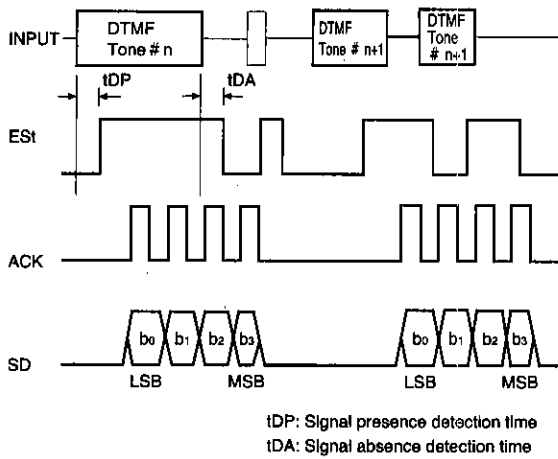
DTMF receiver

Telephones

3) Overall timing chart

tDP: Signal presence detection time
tDA: Signal absence detection time

Fig. 4 Overall timing chart

5) ACK and SD timing

tDL   : Setup time
tPAD : Output delay time
tDH   : Hold time

Fig. 5 ACK and SD timing

4) Serial data correspondence table

Table 1. Serial data correspondence table

ROW [Hz]	COL [Hz]	No.	b3 (MSB)	b2	b1	b0 (LSB)
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0 = "L" level , 1 = "H" level
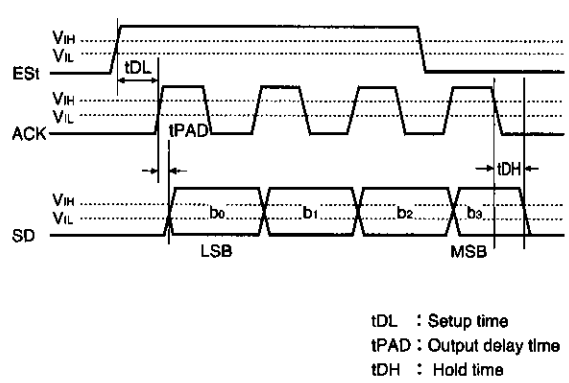
6) Operation mode input logic

Table 2. Operation mode input logic

ACK	PWDN	ACK PWDN Status
X	L	Normal operation mode
L	⌐H	Power down mode
H	H	Not defined

X=don't care

⌐=After an "L" level has been applied to the ACK pin, the power down mode is entered at the rising edge.
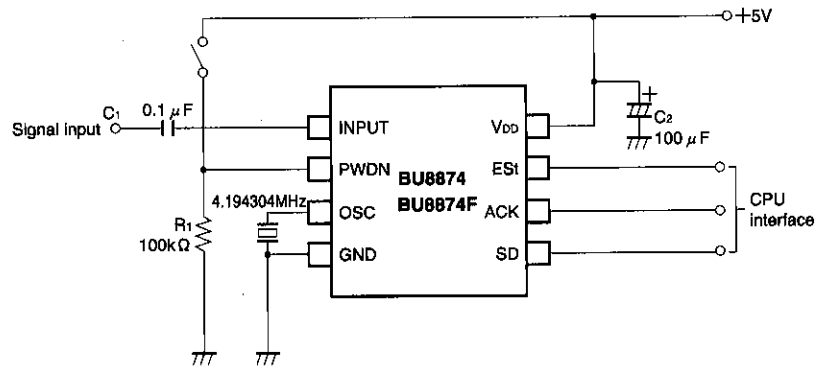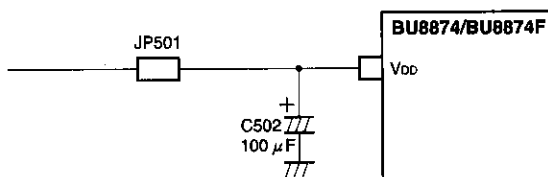
● Application example

Fig. 6

● Selecting attachment components

1) Power supply components

Fig. 7 Power supply circuit

C502 : This is the V_{DD} bypass capacitor, and is nor-
mally 100 μF.

JP501 : This is normally shorted. To test the current
consumption of the IC (at the point where the
power down mode is entered), insert a DC
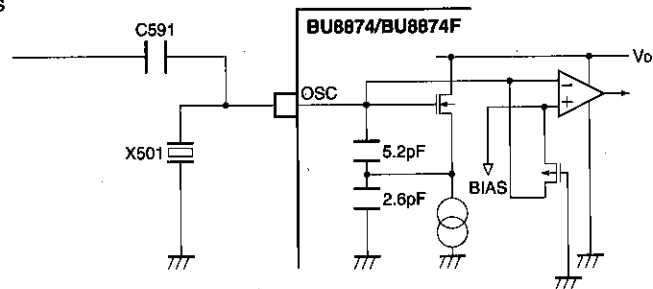ammeter in place of JP501.

2) Oscillation components

Fig. 8 Oscillation circuit

X501 : Use a crystal or ceramic resonator with an os-
cillation frequency of 4.194304MHz. If using a
ceramic resonator, there may be problems
with the precision of the oscillation frequency,
so we recommend using one of the ceramic
resonators listed below. ·

C591 : If you are using a dedicated resonator
X501 designed for DTMF receivers, capacitor
C591 should be left open. If you are injecting
an external clock, X501 should be omitted
and DC blocking capacitor C591 used in its
place. Typically, this capacitor should be 47 μ
nF.

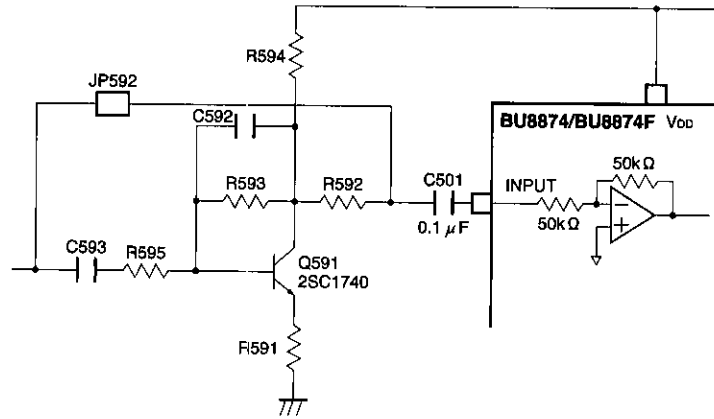DTMF receiver

Telephones

3) DTMF input

Fig. 9 DTMF input circuit

C501 ː This is the DC blocking capacitor. Select a capacitor that will pass DTMF signals (greater than 697Hz) without significantly attenuating the signals.

JP592 ː If DTMF signals are being input directly, both ends should be shorted.

Q591
R591 ~ R595 } Use these to increase the sensitivity of the DTMF receiver.
C592, C593

4) ESt output
The ESt guard time is determined by the CPU of the host computer, but to reduce the load on the host computer, the guard time can be set using an external circuit, as shown in Figure 10.
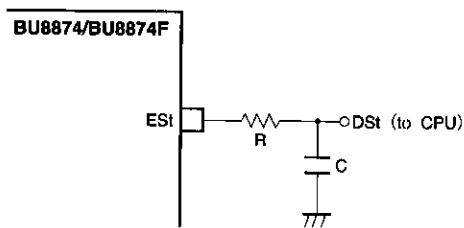
Fig. 10 Guard time setting circuit

The relation between a momentary falter in the ESt guard time (t_{GL}), a momentary HIGH level in the ESt guard time (t_{GH}), and the time constant is shown below. Figure 12 shows a timing diagram for guard times.
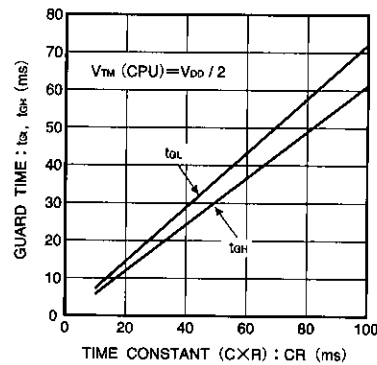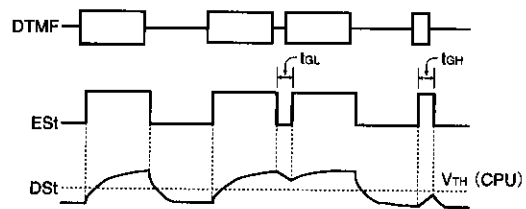

Fig. 11 Guard time vs.
constant (C × R)

Fig. 12 Timing indicating guard times

ROHM

●Operation notes

・Power down

When ACK is LOW, the power down mode can be entered by applying a rising edge to the PWDN pin. Current consumption drops from several seconds to several tens of seconds after the power down mode has been specified.

Operation with SD multiple reading is recommended.

・Oscillation

Oscillation frequency precision can be a problem with ceramic resonators. Before including a ceramic resonator in your design, please consult the resonator manufacturer to make sure this will not be a problem. Also, if an external clock is being injected, a DC blocking capacitor must be inserted. Select a capacitor that will neither attenuate the frequency components or put an excessive load on the drive side.
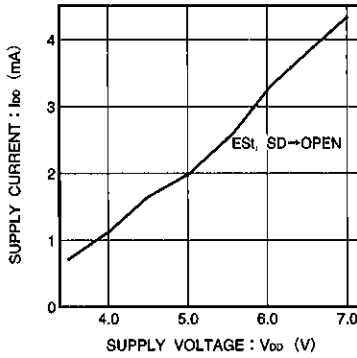
●Measurement data

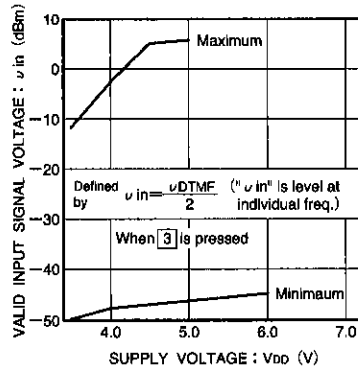Fig. 13 Supply current vs. supply voltage characteristic

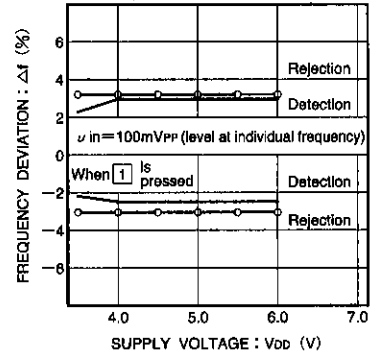Fig. 14 Valid input level range vs. supply voltage characteristics

Fig. 15 Frequency detection/rejection ranges vs. supply voltage characteristic
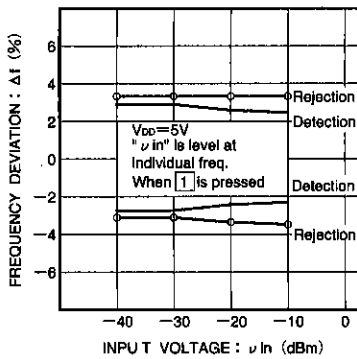
Fig. 16 Frequency detection/rejection ranges vs. input voltage characteristic
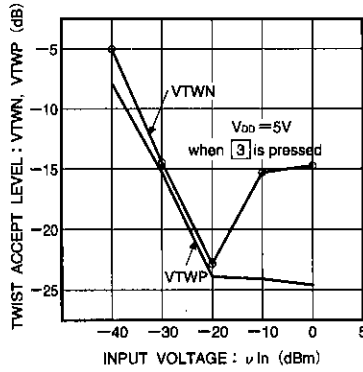
Fig. 17 2-frequency level vs. input voltage characteristic
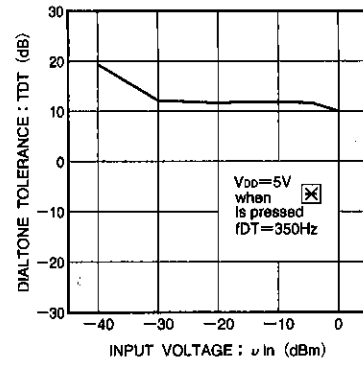
Fig. 18 Dial tone tolerance range vs. input voltage characteristic
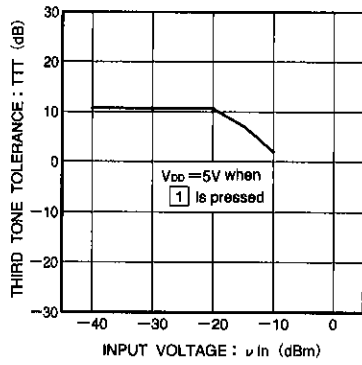
DTMF receiver

Telephones

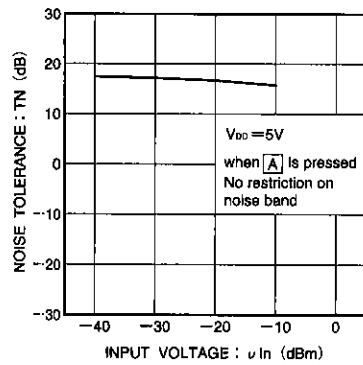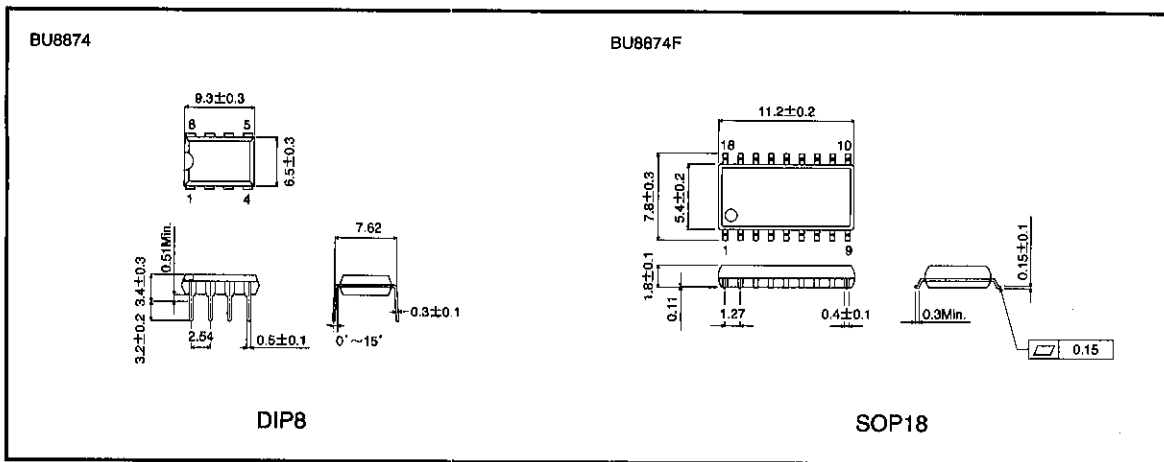Fig. 19 Third tone tolerance range vs. input voltage characteristic

Fig. 20 Noise tolerance range vs. input voltage characteristic

●External dimensions (Units: mm)

ROHM

Notes

- The contents described in this catalogue are correct as of March 1997.
- No unauthorized transmission or reproduction of this book, either in whole or in part, is permitted.
- The contents of this book are subject to change without notice. Always verify before use that the contents are the latest specifications. If, by any chance, a defect should arise in the equipment as a result of use without verification of the specifications, ROHM CO., LTD., can bear no responsibility whatsoever.
- Application circuit diagrams and circuit constants contained in this data book are shown as examples of standard use and operation. When designing for mass production, please pay careful attention to peripheral conditions.
- Any and all data, including, but not limited to application circuit diagrams, information, and various data, described in this catalogue are intended only as illustrations of such devices and not as the specifications for such devices. ROHM CO., LTD., disclaims any warranty that any use of such device shall be free from infringement of any third party's intellectual property rights or other proprietary rights, and further, assumes absolutely no liability in the event of any such infringement, or arising from or connected with or related to the use of such devices.
- Upon the sale of any such devices; other than for the buyer's right to use such devices itself, resell or otherwise dispose of the same; no express or implied right or license to practice or commercially exploit any intellectual property rights or other proprietary rights owned or controlled by ROHM CO., LTD., is granted to any such buyer.
- The products in this manual are manufactured with silicon as the main material.
- The products in this manual are not of radiation resistant design.

The products listed in this catalogue are designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys). Should you intend to use these products with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers, or other safety devices) please be sure to consult with our sales representatives in advance.

- Notes when exporting
    - It is essential to obtain export permission when exporting any of the above products when it falls under the category of strategic material (or labor) as determined by foreign exchange or foreign trade control laws.
    - Please be sure to consult with our sales representatives to ascertain whether any product is classified as a strategic material.