

Dual PLL frequency synthesizer

BU2630F/BU2630FV

The BU2630F/FV is a CMOS LSI with an internal dual PLL synthesizer.

VCOs for transmission and reception can be controlled independently, and the reference frequency and main counter settings can also be programmed separately. This product is designed for applications involving cordless telephones and communications equipment worldwide.

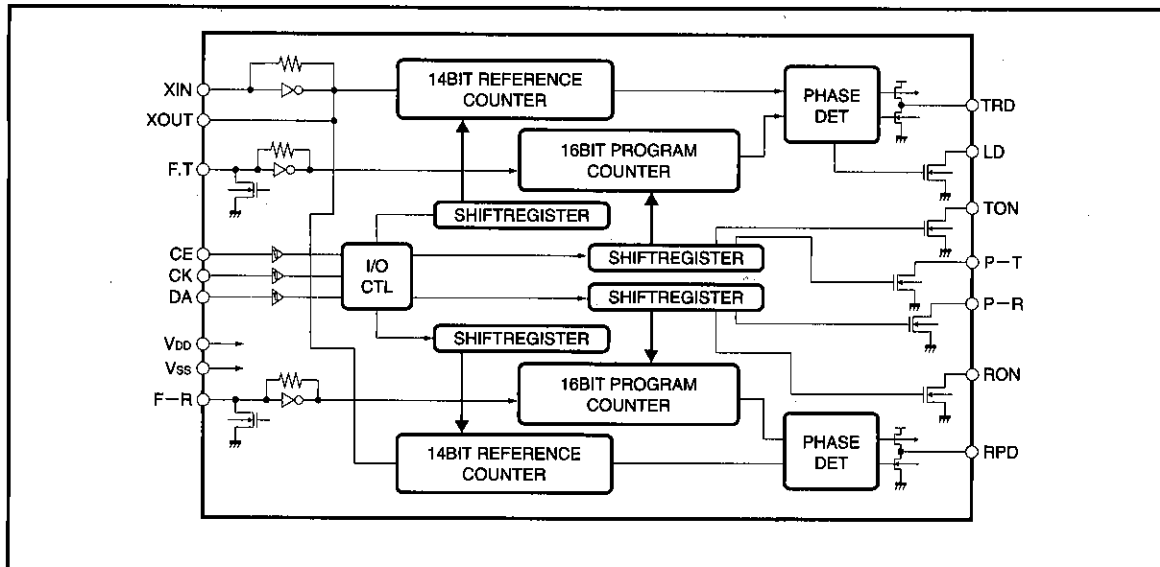
●Applications

Cordless telephones, amateur short wave radios, industrial transceivers, VHF/UHF frequency generators, and others

●Features

- | | |
|--|---|
| 1) Operation possible at up to 80MHz ($V_{DD} = 2.5$). | 3) 16-bit main counter. |
| 2) Low current consumption | 4) Internal 14-bit reference frequency counter. |
| Dual-system operation : 2.2mA (typ.), $V_{DD} = 3V$ | 5) Unlock detection possible. |
| Single-system operation : 1.2mA (typ.), $V_{DD} = 3V$ | 6) Four output ports. (open drain) |
| Non-operating state : 0.2mA (typ.), $V_{DD} = 3V$ | 7) Control possible using 3-wire serial input. |

●Block diagram



● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{DD}	-0.3~7.0	V
Power dissipation	BU2630F	Pd	mW
	BU2630FV		
Operating temperature	T _{opr}	-40~85	°C
Storage temperature	T _{stg}	-55~125	°C

*1 Reduced by 5.0mW for each increase in Ta of 1°C over 25°C.

*2 Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

● Recommended operating conditions (Ta=25°C)

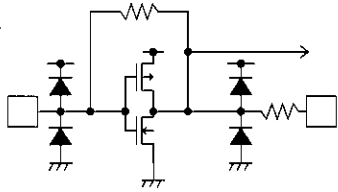
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V _{DD}	2.5	3.0	5.5	V

● Pin description

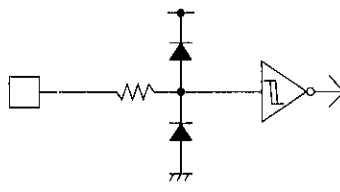
Pin No.	Symbol	Pin Name	Function	I/O circuit
16	XOUT	Liquid crystal resonator	For reference frequency	TYPE A
1	XIN			
2	V _{SS}			
3	RPD	Phase comparison output	This is LO if the locally divided value is higher than the reference frequency, HI if it is lower, and Z if it matches.	TYPE E
4	P-R	Output port	This is controlled by the input data.	TYPE D
5	RON			
6	F-R	VCO input	Local input for reception	TYPE F
7	CE	Chip enable clock signal serial data	When CE is HIGH, the DA synchronized to the rise of CK is read into the internal shift register, and is latched at the timing of the CE fall.	TYPE B
8	CK			
9	DA			
10	LD	Unlock output	This goes ON when the PLL is unlocked on the transmission side	TYPE D
11	F-T	VCO input	Local input for transmission	TYPE F
12	TON	Output port	This is controlled by the input data	TYPE D
13	P-T			
14	TPD	Phase comparison output	This is LO if the locally divided value is higher than the reference frequency, HI if it is lower, and Z if it matches.	TYPE E
15	V _{DD}	Power supply	2.5~5.5V	

● Input/output circuits

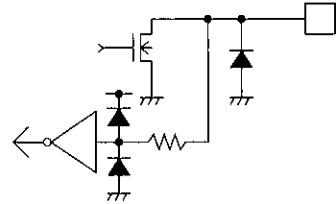
TYPE A



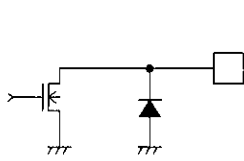
TYPE B



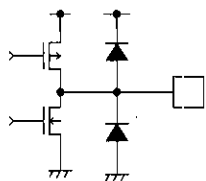
TYPE C



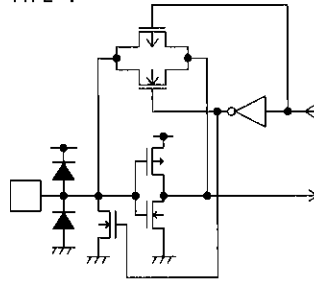
TYPE D



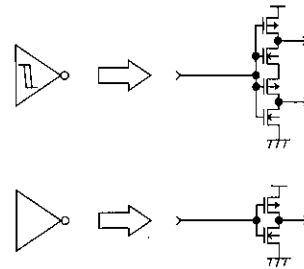
TYPE E



TYPE F



TYPE I



●Electrical characteristics (Unless otherwise noted, Ta=25°C, VDD=3.0V, VSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Circuit current 1	I _{DD1}	—	2.2	3.0	mA	Dual-system operation	F-T F-R=80MHz, 100mVrms XTAL=10.24MHz
Circuit current 2	I _{DD2}	—	1.2	2.0	mA	Single-system operation	
Circuit current 3	I _{DD3}	—	0.2	0.3	mA	With operation stopped: XTAL = 10.24 MHz	
"H" input voltage 1	V _{IH1}	0.8V _{DD}	—	—	V	CE CK DA	
"L" input voltage 1	V _{IL1}	—	—	0.2V _{DD}	V	CE CK DA	
"H" input current 1	I _{IH1}	—	—	1.0	μA	CE CK DA V _{IN} =V _{DD}	
"H" input current 2	I _{IH2}	—	0.3	—	μA	XIN V _{IN} =V _{DD}	
"H" input current 3	I _{IH3}	—	5.0	—	μA	F-T F-R V _{IN} =V _{DD}	
"L" input current 1	I _{IL1}	-1.0	—	—	μA	CE CK DA V _{IN} =V _{SS}	
"L" input current 2	I _{IL2}	—	-0.3	—	μA	XIN V _{IN} =V _{SS}	
"L" input current 3	I _{IL3}	—	-5.0	—	μA	F-T F-R V _{IN} =V _{SS}	
"L" output voltage 1	V _{OL1}	—	0.3	0.5	V	LD TON P-T RON P-R I _O =1.0mA	
"OFF" leakage current 1	I _{OFF1}	—	—	1.0	μA	LD TON P-T RON P-R V _O =10V	
"L" output voltage 2	V _{OL2}	—	—	0.3	V	F-T F-R I _{OUT} =0.1mA	
"H" output voltage	V _{OIH}	V _{DD} -50	V _{DD} -1.0	—	mV	TPD RPD I _{OUT} =-0 μA	
"L" output voltage	V _{OIL}	—	1.3	50	mV	TPD RPD I _{OUT} =0 μA	
"H" output voltage	V _{OIH}	V _{DD} -100	V _{DD} -40	—	mV	TPD RPD I _{OUT} =-100 μA	
"L" output voltage	V _{OIL}	—	30	100	mV	TPD RPD I _{OUT} =100 μA	
"OFF" leakage current 2	I _{OFF2}	—	—	100	nA	TPD RPD V _{OUT} =V _{DD}	
"OFF" leakage current 3	I _{OFF3}	-100	—	—	nA	TPD RPD V _{OUT} =V _{SS}	

PLL frequency synthesizers for radio communications

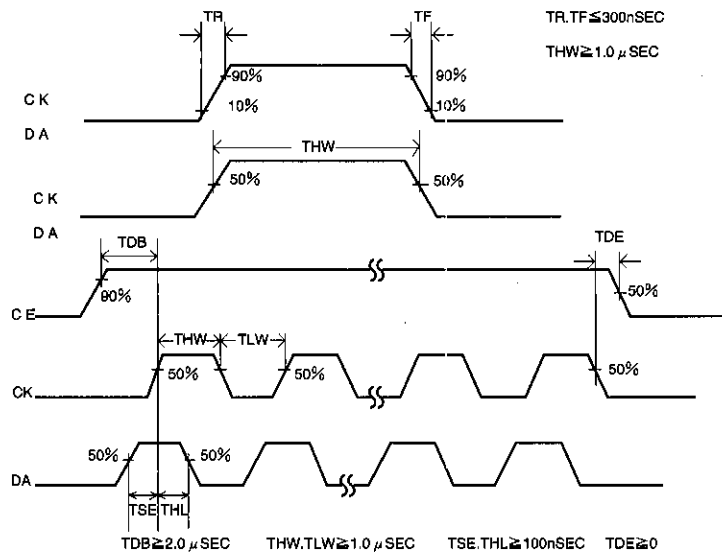
Cellular phones/PHS/Pagers

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Internal feedback resistance 1	R _{F1}	—	10	—	MΩ	XIN
Internal feedback resistance 2	R _{F2}	—	500	—	KΩ	F-T F-R
Input frequency 1	F _{IN1}	1.0	10.24	16.0	MHz	XIN, sine wave, C coupling
Input frequency 2	F _{IN2}	1.0	—	20	MHz	F-T F-R, sine wave, C coupling*2, V _{IN} = 100 mVrms
Input frequency 3	F _{IN3}	50	—	80	MHz	F-T F-R, sine wave, C coupling*2, V _{IN} = 100 mVrms
Input frequency 4	F _{IN4}	20	—	50	MHz	F-T F-R, sine wave, C coupling*2, V _{IN} = 50 mVrms
Input frequency 5 *1	F _{IN5}	0.4	—	20	MHz	F-T F-R, sine wave, C coupling*2, V _{IN} = 100mVrms
Maximum input amplitude	F _{INMax}	—	—	V _{DD} +0.3	V _{p-p}	XIN, F-T F-R
Input capacitance	C _{IN}	—	4	7	PF	F-T F-R
Minimum pulse width	TW	1.0	—	—	μSEC	CK, DA
Input data rise time	TR	—	—	300	nSEC	CK, DA
Input data fall time	TF	—	—	300	nSEC	CE, CK, DA

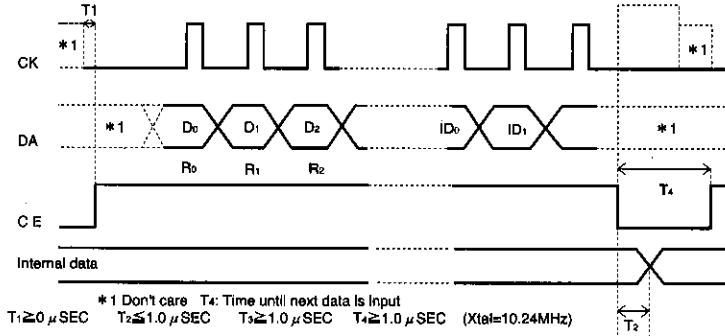
© Not designed for radiation resistance. *1 PS = 1
 *2 Minimum input level at which operation is possible
 Divider values which can be set
 Program divider: PS = 0: 256 ~ 65535, PS = 1: 3 ~ 4095
 Reference frequency divider: 3 ~ 16383

● Circuit operation

Input data switching characteristics



● Circuit operation
Input data format



Programmable divider and control data input: TX side (ID₀ = 0, ID₁ = 0), RX side (ID₀ = 1, ID₁ = 0)

LSB ← Input from D₀

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅		
								P-T	TON	OFF	PS	T ₀	T ₁	ID ₀	ID ₁	MSB	
								(P-R	TON	OFF	PS	T ₀	T ₁)				

Reference frequency divider data input: TX side (ID₀ = 0, ID₁ = 1), RX side (ID₀ = 1, ID₁ = 1)

R ₀	R ₁	R ₂	R ₃	R ₄	R ₅	R ₆	R ₇	R ₈	R ₉	R ₁₀	R ₁₁	R ₁₂	R ₁₃	PL	PH
LSB				*	*	LD ₀	LD ₁	*	*	ID ₀	ID ₁	MSB			

* Don't care (LD₀ and LD₁₀ are valid on TX side only)

Description of data

(1) Programmable divider data : D₀ ~ D₁₅

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅
0	1	0	1	0	1	1	0	0	0	1	0	0	1	0	0
A				6				4				2			

Example: For a transmission frequency of 46.610MHz and a reference frequency of 5.00 kHz
 No. of divisions: $46.610 \div 5.00 \text{ kHz} = 9322 \text{ (D)} = 246\text{A (H)}$

(2) Reference frequency data : R₀ ~ R₁₃

R ₀	R ₁	R ₂	R ₃	R ₄	R ₅	R ₆	R ₇	R ₈	R ₉	R ₁₀	R ₁₁	R ₁₂	R ₁₃		
0	0	0	0	0	0	0	0	0	0	0	1	0	0		
0				0				8				0			

Example: When XTAL = 10.24 MHz and reference frequency is 5.00 kHz
 No. of divisions: $10.24 \text{ MHz} \div 5.00 \text{ kHz} = 2048 \text{ (D)} = 800 \text{ (H)}$

● Electrical characteristic curves

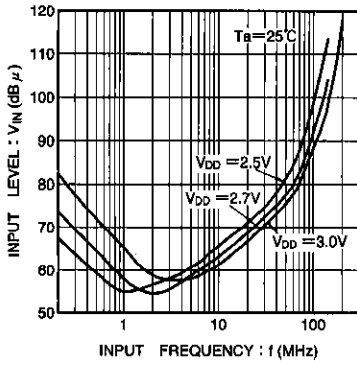


Fig. 2 Input frequency vs. input level

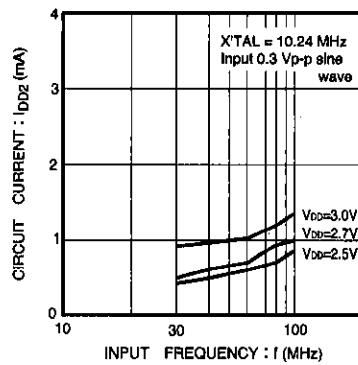


Fig. 3 Input frequency vs. circuit current (for single operation)

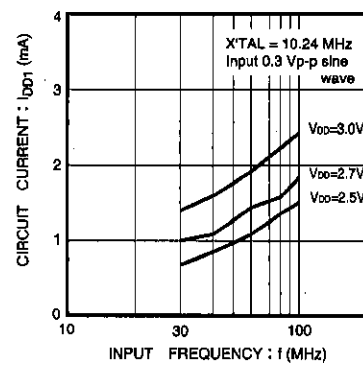
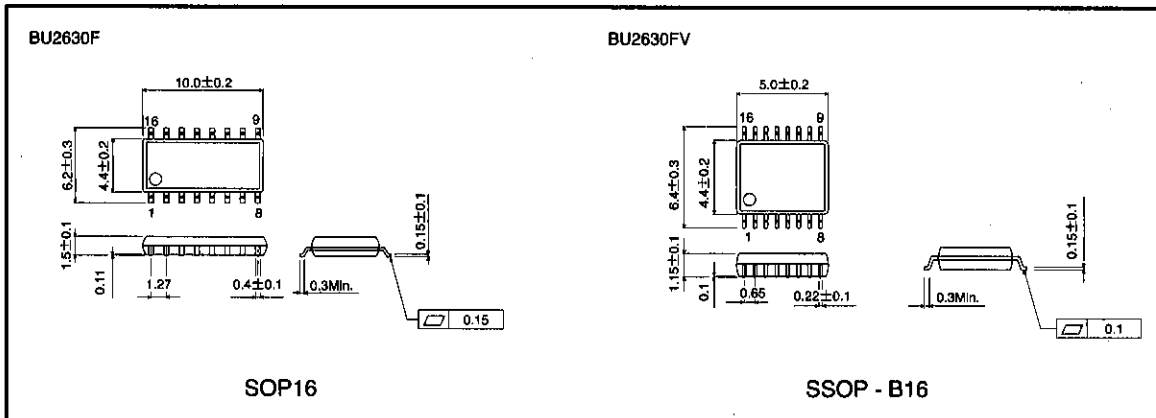


Fig. 4 Input frequency vs. circuit current (for dual operation)

● External dimensions (Units: mm)



PLL frequency synthesizers for radio communications

Cellular phones/PHS/Pagers

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