PLL frequency synthesizer for tuners

BU2615S / BU2615FS

BU2615 PLL frequency synthesizers work up through the FM band. Featuring low radiation noise, low power consumption, and highly sensitive built-in RF amps, they support an IF count function.

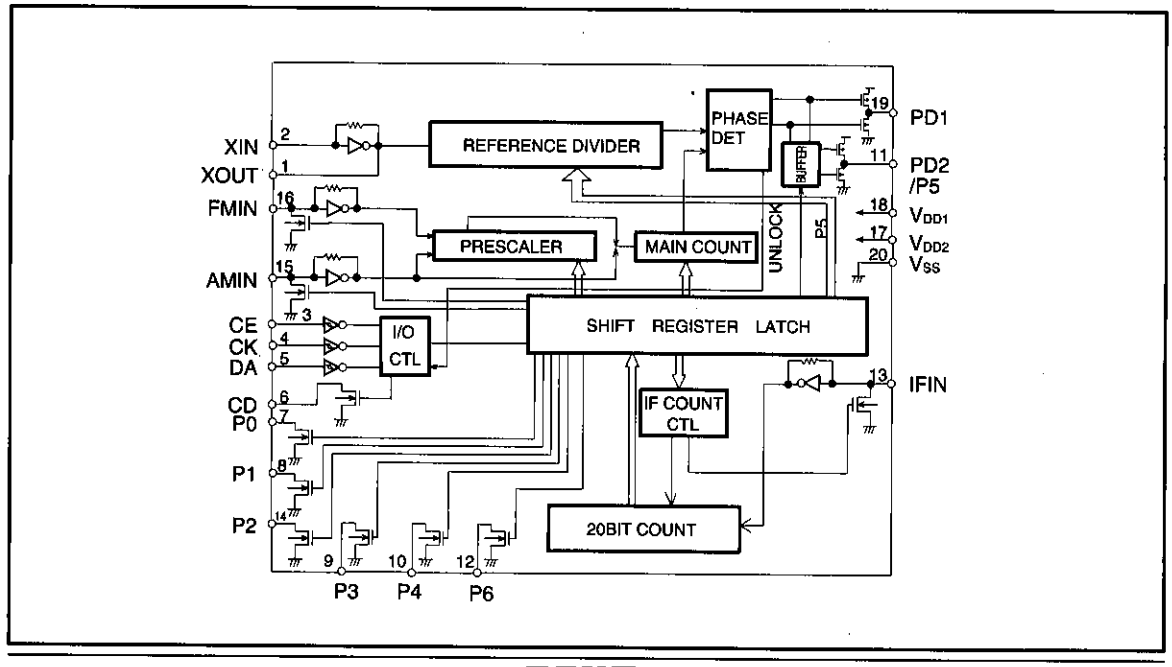
●Applications

Tuners (Mini components, radio cassette players, radio equipment, etc.)

●Features

1) Built-in high-speed prescaler can divide 130MHzVCO.
2) Basic oscillation of 75kHz keeps unnecessary radiation noise to a low level.
3) Low power-consumption (during operation : 4mA PLL OFF 100 μA)
4) In addition to the standard FM and AM, also offers the following 7 frequencies : 25kHz, 12.5kHz, 6.25kHz, 3.125kHz, 5kHz, 3kHz, and 1kHz.
5) Counter for measurement of intermediate frequencies.
6) Unlock detection
7) Seven output ports (open drain).
   The BU2614, with three output ports, is also available.
8) Serial data input (CE.CK.DA)

●Block diagram



●Pin assignments

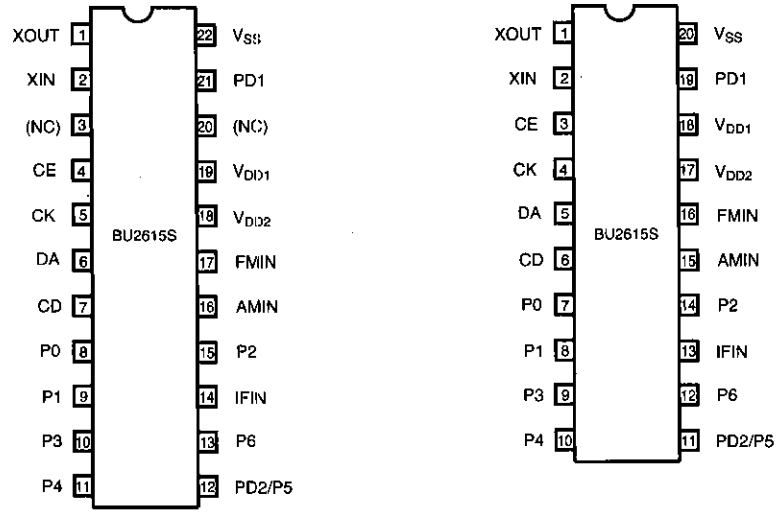


Fig.1 Pin assignments

●Pin description

Pin No. BU2615S	Pin No. BU2615FS	Symbol	Terminal name	Function	I/O
1	1	XOUT	Crystal oscillation terminal	For generation of standard frequency and internal clock. Connected to 75 kHz crystal oscillator.	OUT
2	2	XIN			IN
4	3	CE	Chip enable	When CE is H, DA is synchronous with the rise of CK and read to the internal shift register. DA is then latched at the timing of the fall of CE. Also, output data is output from the CD terminal synchronous to the rise of CK.	IN
5	4	DA	Serial data		
6	5	CK	Clock signal		
7	6	CD	Count data	Frequency data and unlock data are output.	Nch open drain
8	7	P0	Output port	Controlled on the basis of input data.	
9	8	P1			
10	9	P3			
11	10	P4			
12	11	P5/PD2		P5/PD2 can be switched between output port and phase comparison output on the basis of input data.	CMOS/3-state
13	12	P6			Nch open drain
14	13	IFIN	IF input	Input for frequency measurement.	IN
15	14	P2	Output port	Controlled on the basis of input data.	Nch open drain
16	15	AMIN	AM input	Local input for AM	IN
17	16	FMIN	FM input	Local input for FM	IN
18	17	V_{DD2}	Power supply 2	4.0V to 6.0V applied for high-speed circuit power supply.	
19	18	V_{DD1}	Power supply 1	Power supply for logic. 2.7V to 6.0V	
21	19	PD1	Phase comparison output	High level when value obtained by dividing local output is higher than standard frequency. Low level when value is lower. High impedance when value is same.	3-state
22	20	V_{SS}	GROUND		
3.20	—	NC	NC	No internal connection.	

●Absolute maximum ratings (Ta = 25℃)

Parameter		Symbol	Limits	Unit	Conditions
Power supply voltage		V_{DD}	−0.3～7.0	V	V_{DD1}, V_{DD2}
Max. input voltage 1		V_{IN1}	−0.3～7.0	V	CE, CK, DA
Max. input voltage 2		V_{IN2}	−0.3～V_{DD}0.3	V	XIN, FMIN, AMIN, IFIN
Max. output voltage 1		V_{OUT1}	−0.3～10.0	V	P_0, P_1, P_2, P_3, P_4, P_6, CD
Max. output voltage 2		V_{OUT2}	−0.3～V_{DD}0.3	V	PD_1, PD_2, P_5, XOUT
Max. output current		I_{OUT}	0～3.0	mA	P_0, P_1, P_2, P_3, P_4, P_6, CD
Allowable dissipation	BU2615	Pd	600*1	mW	
	BU2615FS		450*2		
Operating temp. range		Topr	−10～75	℃	
Storage temp. range		Tstg	−55～125	℃	

*1 Reduced by 6.0mW for each increase in Ta of 1°C over 25°C.

*2 Reduced by 4.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating power supply voltage range

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD1}	2.7～6.0	V
	V_{DD2}	4.0～6.0	V

●Electrical characteristics (unless other specified, Ta = 25℃, $V_{DD}1 = V_{DD}2 = 5.0V$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage 1	I_{DD1}	—	5.0	10.0	mA	FM_{IN}=130MHz, 100mVrms 17-pin current
Power supply voltage 2	I_{DD2}	—	100	150	μA	18-pin current
Circuit current w/o signal	I_{DD3}	—	150	300	μA	No input, PLL = OFF 17-pin current
"H" level input voltage	V_{IH}	4.0	—	—	V	CE, CK, DA terminals
"L" level input voltage	V_{IL}	—	—	1.0	V	CE, CK, DA terminals
"H" level input current 1	I_{IH1}	—	—	1.0	μA	CE, CK, DA terminals $V_{IN}=V_{DD}$
"H" level input current 2	I_{IH2}	—	0.3	—	μA	XIN terminal $V_{IN}=V_{DD}$
"H" level input current 3	I_{IH3}	—	6.0	—	μA	FMIN, AMIN, IFIN terminals $V_{IN}=V_{DD}$
"L" level input current 1	I_{IL1}	−1.0	—	—	μA	CE, CK, DA terminals $V_{IN}=V_{SS}$
"L" level input current 2	I_{IL2}	—	−0.3	—	μA	XIN terminal $V_{IN}=V_{SS}$
"L" level input current 3	I_{IL3}	—	−6.0	—	μA	FMIN, AMIN, IFIN terminals $V_{IN}=V_{SS}$
"L" level output voltage 1	V_{OL1}	—	0.2	0.5	V	P_0, P_1, P_2, P_3, P_4, P_8, CD I_O=1.0mA
"OFF" level leakage current 1	I_{OFF1}	—	—	1.0	μA	P_0, P_1, P_2, P_3, P_4, P_6, CD V_O=10V
"L" level output voltage 2	V_{OL2}	—	0.1	0.5	V	FMIN, AMIN, IFIN terminals I_{OUT}=0.1mA
"H" level output voltage	V_{OH}	V_{DD}−1.0	V_{DD}−0.3	—	V	PD1, PD2, P5 I_{OUT}=−1.0mA
"L" level output voltage	V_{OL}	—	0.2	1.0	V	PD1, PD2, P5 I_{OUT}=1.0mA
"OFF" level leakage current 2	I_{OFF2}	—	—	100	nA	PD1, PD2 $V_{OUT}=V_{DD}$
"OFF" level leakage current 3	I_{OFF3}	−100	—	—	nA	PD1, PD2 $V_{OUT}=V_{SS}$
Internal return resistance 1	R_{F1}	—	10	—	MΩ	XIN
Internal return resistance 2	R_{F2}	—	500	—	kΩ	FMIN, ANIN, IFIN terminals
Input frequency 1	F_{IN1}	10	75	160	kHz	XIN, sine wave, C coupling
Input frequency 2	F_{IN2}	10	—	130	MHz	FMIN, sine wave, C coupling V_{IN} = 50 mV_{rms}
Input frequency 3	F_{IN3}	0.4	—	30	MHz	AMIN1, sine wave, C coupling V_{IN} = 70 mV_{rms}
Input frequency 4	F_{IN4}	0.4	—	16	MHz	IFIN, sine wave, C coupling V_{IN} = 70 mV_{rms}
Max. input amplitude	F_{INMAX}	—	—	1.5	Vrms	XIN, FMIN, AMIN, IFIN, sine wave, C coupling
Min. pulse amplitude	TW	—	1.0	—	μs	CK, DA
Input rise time	TR	—	—	500	ns	CE, CK, DA
Input fall time	TF	—	—	500	ns	CE, CK, DA

●Explanation of the data

(1) Division data : For D_0 through D_{15} (When S = 1, use D_4 through D_{15}.)

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

Examples :

Divided frequency = 1100 S = 0, PS = 0 Divided value is double the set value.

0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0
Divided frequency = 1107 (D) =453 (H)				S=1、PS=1											
1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0
Divided frequency = 926(D) =39E (H)				S=1、PS=0											
×	×	×	×	0	1	1	1	1	0	0	1	1	1	0	0

(2) CT : Frequency measurement beginning data
1 : Beginning of measurement
0 : Internal counter is reset, IFIN is pulldown.

(3) Output port control data : P0, P1, P2, P3, P4, P5, P6
1 : Open drain output ON (P5 is LO)
0 : Open drain output OFF (P5 is HI)

(4) R0, R1, R2, standard frequency data

Data			
R_0	R_1	R_2	Standard frequency
0	0	0	25kHz
0	0	1	12.5kHz
0	1	0	6.25kHz
0	1	1	5kHz
1	0	0	3.125kHz
1	0	1	3kHz
1	1	0	1kHz
1	1	1	※PLL OFF

※ FMIN = pulldown, AMIN = pulldown, PD = high impedance

(5) S : switch between FMIN and AMIN
0 : FMIN 1 : AMIN

(6) PS : If this bit is set to ON while AMIN is selected, swallow counter division is possible.

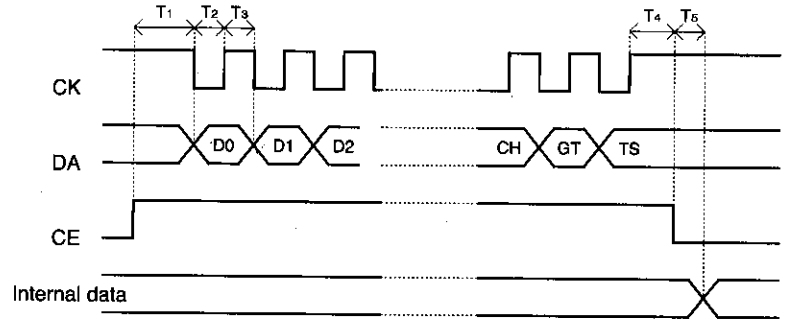
(7) CH : If this bit set to ON, output port P5 goes to phase comparison output. 0 : P5 1 : PD2

(8) GT : Frequency measurement time and unlock detection ON/OFF

CT	GT	Frequency measurement	Unlock detection	Data output
0	0	OFF	OFF	NG
0	1	OFF	ON	OK
1	0	ON gate time 16 mSEC	ON	
1	1	ON gate time 32 mSEC	ON	

(9) TS : Test data (0) is input.

●Input data format



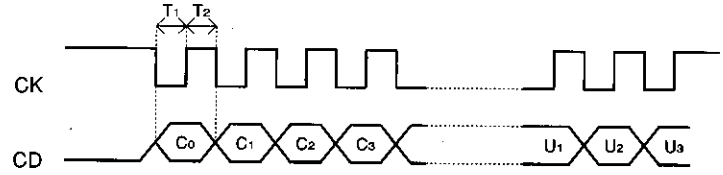
$T_1 \geqq 15\,\mu SEC$ T_2、$T_3 > 1\,\mu SEC$ $T_4 > 0\,\mu SEC$ $T_5 < 15\,\mu SEC$

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

← Input done from D_0.

P_0	P_1	P_2	P_3	P_4	P_5	P_6	CT	R_0	R_1	R_2	S	PS	CH	GT	TS

Output data format CE output is LO.



$T_1, T_2 > 1\,\mu SEC$

Output data includes pullup resistance.

Output data format

LSB

C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

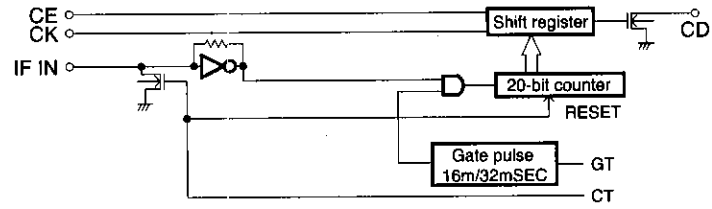
← Input done from C_0.

C_{16}	C_{17}	C_{18}	C_{19}	U_0	U_1	U_2	U_3

※ Data output only possible when CT = 1 or GT = 1.

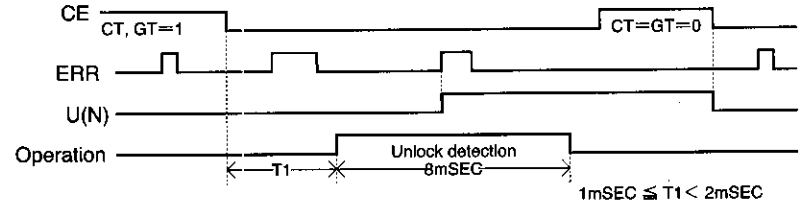
●Frequency counter

1) Structure



2) How the frequency counter operates
When control data CT equals 1, the 20-bit counter and the amp go into operation. When CT equals 0, input pulldown and the counter are reset. Measuring time (gate pulse) is selected (16mSEC/32mSEC) on the basis of control data GT. When control data CT equals 0, the counter is reset.

3) Explanation of output data
D_0 : LSB D_{19} : MSB
How the unlock detection circuit operates
When control data GT equals 1, or CT equals 1, the unlock detection circuit goes into operation for 8mSEC. When CT equals 1, the unlock detection circuits stops operating before the frequency counter gate pulse is emitted. When CT equals 0, or GT equals 0, the unlock detection circuit is reset.

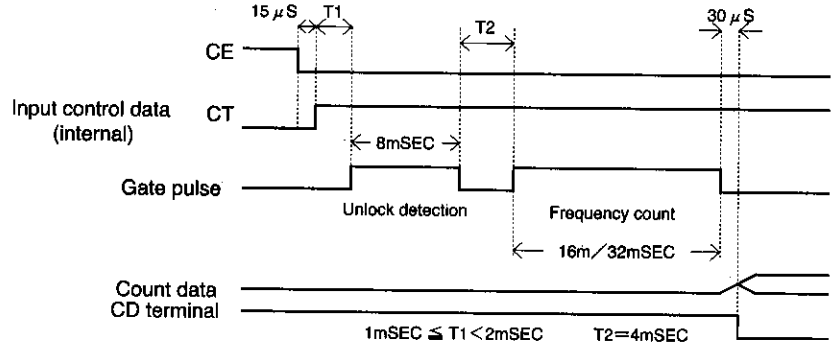


Explanation of output data

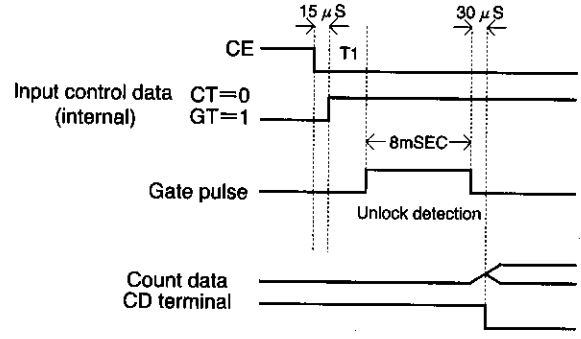
U0	U1	U2	U3					
0	0	0	0		<	ERR	<	7 μSEC
1	1	1	0	7 μSEC	<	ERR	<	13 μSEC
1	1	0	0	13 μSEC	<	ERR	<	26 μSEC
1	1	1	0	26 μSEC	<	ERR	<	54 μSEC
1	1	1	1	54 μSEC	<	ERR	<	

●How the frequency counter and unlock detection circuit operate

1) When CT = 1 : Frequency count and unlock detection are carried out.

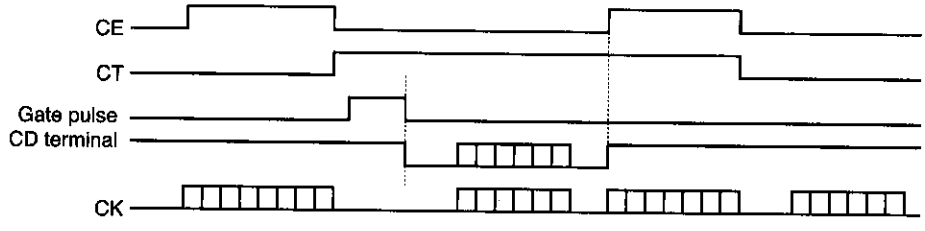


2) When CT = 0 and GT = 1 : Only unlock detection is carried out.



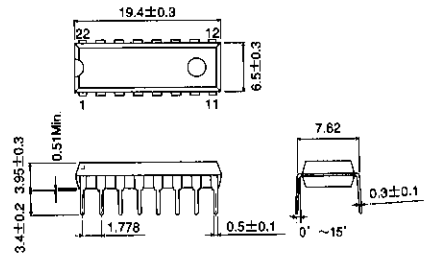
●Explanation of CD terminal

When frequency measurement or unlock detection is finished, the CD terminal goes to LO to indicate that the count and unlock detection have finished. It also synchronizes with CK to output counter data. When the next data is input, it goes to HI.



●External dimensions (Unit: mm)

BU2615S



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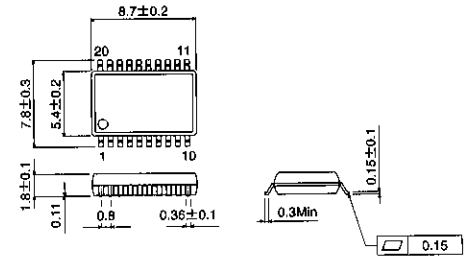

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