

# Clock Generator for Video CD Systems

## BU2173F

The BU2173F is an IC that generates the CPU clock signal, system clock signal and video clock signal used in video CD systems. A single crystal resonator can generate three different oscillation frequencies.

### ●Applications

Video CD systems

### ●Features

- 1) Three frequency clock signals can be generated with a single attached crystal resonator.
- 2) Two internal PLL channels.
- 3) Internal loop filter, eliminating the need to attach a loop.
- 4) Single 5.0V power supply.
- 5) SOP 18-pin package.

### ●Absolute maximum ratings (Ta=25°C)

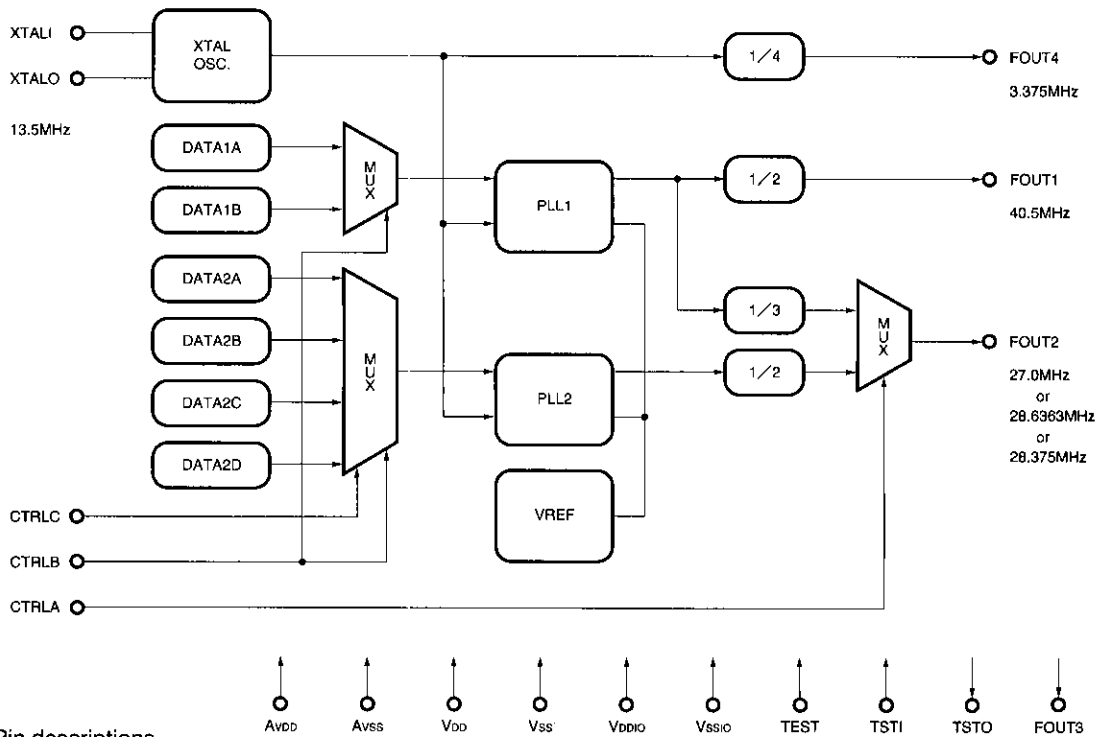
Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>DD</sub>	-0.3~7.0	V
Power dissipation	P <sub>d</sub>	450	mW
Operating temperature	T <sub>opr</sub>	-5~70	°C
Storage temperature	T <sub>stg</sub>	-25~125	°C

\* Reduced by 4.5 mW for each increase in Ta of 1°C over 25°C.

### ●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>DD</sub> , A <sub>VDD</sub> , V <sub>DDIO</sub>	4.75~5.25	V
Input voltage, high level	V <sub>IH</sub>	0.8V <sub>DD</sub> ~V <sub>DD</sub>	V
Input voltage, low level	V <sub>IL</sub>	0.0~0.2V <sub>DD</sub>	V
Operating temperature	T <sub>opr</sub>	-5~70	°C

## ● Block diagram

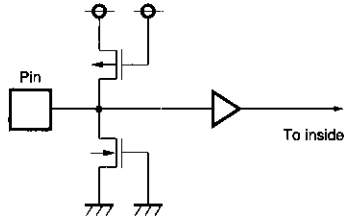


## ● Pin descriptions

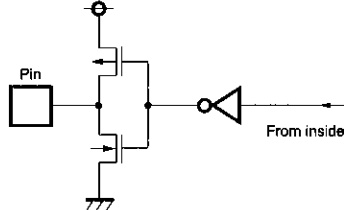
Pin No.	Pin name	Function	Type
1	V <sub>DD</sub>	Digital V <sub>DD</sub>	—
2	TSTO	Open in the normal mode (used for testing)	B
3	XTALI	Reference oscillation input	C
4	XTALO	Reference oscillation output	C
5	CTRLA	GD-G/VCD clock switching	A
6	CTRLB	Stays at the high level when the IC is in the normal mode	A
7	CTRLC	CD-G PAL/NTSC clock switching	A
8	TSTI	Connect to V <sub>SS</sub> when the IC is in the normal mode (used for testing)	A
9	V <sub>SS</sub>	Digital ground	—
10	Av <sub>SS</sub>	Analog ground	—
11	FOUT3	Not used (open when the IC is in the normal mode)	B
12	V <sub>SSIO</sub>	I/O ground	—
13	FOUT2	Clock output 2	B
14	TEST	Setting the test mode (connect to V <sub>SS</sub> when the IC is in the normal mode)	A
15	FOUT1	Clock output 1	B
16	V <sub>DDIO</sub>	I/O V <sub>DD</sub>	—
17	FOUT4	Clock output 4	B
18	Av <sub>DD</sub>	Analog V <sub>DD</sub>	—

● Input/output circuits

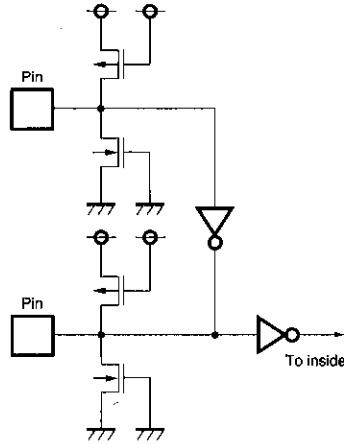
Type A



Type B



Type C



● Electrical characteristics (unless otherwise noted, Ta=25°C, V<sub>DD</sub>=5.0V, A<sub>VDD</sub>=5.0V, I<sub>O<sub>VDD</sub></sub>=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input current, low level	I <sub>IL</sub>	-300.0	0.0	300.0	μA	
Input current, high level	I <sub>IH</sub>	-300.0	0.0	300.0	μA	
Input voltage, low level	V <sub>IL</sub>	—	—	1.0	V	
Input voltage, high level	V <sub>IH</sub>	4.0	—	—	V	
Output voltage, low level	V <sub>OL</sub>	—	—	0.5	V	I <sub>OL</sub> =4.0mA
Output voltage, high level	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> =-4.0mA
Circuit current	I <sub>DD</sub>	—	30	50	mA	f <sub>XTAL</sub> = 13.5 MHz, no load
Reference frequency	f <sub>REF</sub>	—	13.5	—	MHz	Use with CTRLB at the high level
Output frequency (1)	f <sub>1</sub>	—	40.5	—	MHz	f <sub>1</sub> =f <sub>REF</sub> ×96/16/2
Output frequency (2)	f <sub>2A</sub>	—	27.000	—	MHz	f <sub>2A</sub> =f <sub>REF</sub> ×96/16/3 CTRLA=H, CTRLB=H, CTRLC=H
	f <sub>2B</sub>	—	28.375	—	MHz	f <sub>2B</sub> =f <sub>REF</sub> ×227/54/2 CTRLA=L, CTRLB=H, CTRLC=L
	f <sub>2C</sub>	—	28.636	—	MHz	f <sub>2C</sub> =f <sub>REF</sub> ×140/33/2 CTRLA=L, CTRLB=H, CTRLC=H
Output frequency (4)	f <sub>4</sub>	—	3.375	—	MHz	f <sub>4</sub> =f <sub>REF</sub> ×1/4
Jitter		—	1.0	—	nSec	Measure at f <sub>2A</sub> , f <sub>2B</sub> , f <sub>2C</sub> (reference)
Reference frequency (2)	f <sub>REF2</sub>	—	14.318	—	MHz	Use with CTRLB at the low level
Output frequency (1)	f <sub>1B</sub>	—	40.5	—	MHz	f <sub>1B</sub> =f <sub>REF2</sub> ×98/35/2
Output frequency (2)	f <sub>2D</sub>	—	27.000	—	MHz	f <sub>2D</sub> =f <sub>REF2</sub> ×98/35/3 CTRLA=H, CTRLB=L, CTRLC=H
	f <sub>2E</sub>	—	28.636	—	MHz	f <sub>2E</sub> =f <sub>REF2</sub> ×80/20/2 CTRLA=L, CTRLB=L, CTRLC=H
Output frequency (4)	f <sub>4B</sub>	—	3.579	—	MHz	f <sub>4B</sub> =f <sub>REF2</sub> ×1/4

● Measurement circuit

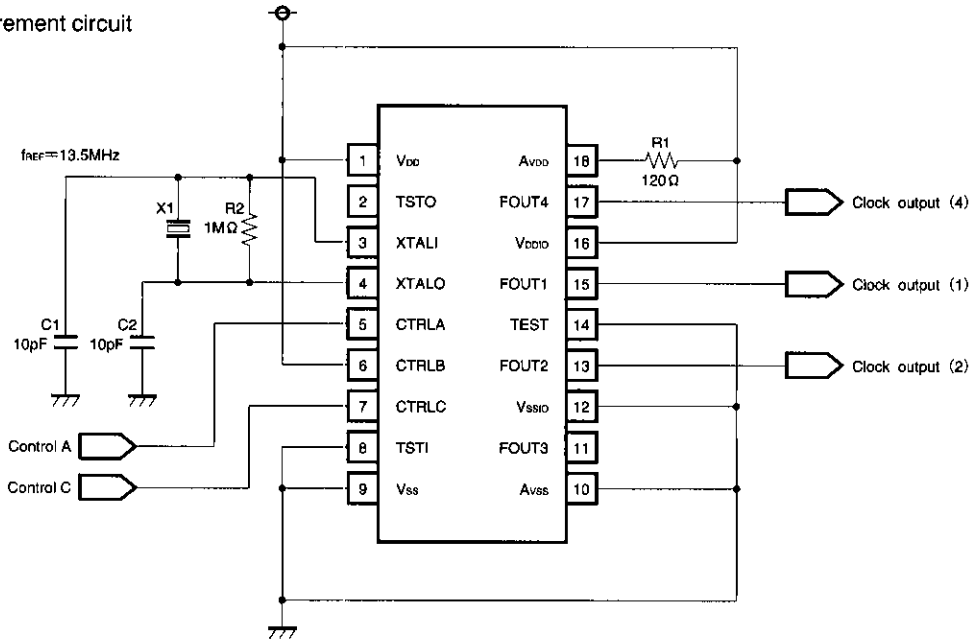


Fig. 1

Note: Certain crystal resonators may require setting XTALI and XTALO to the optimum allowable values.

● Application circuit

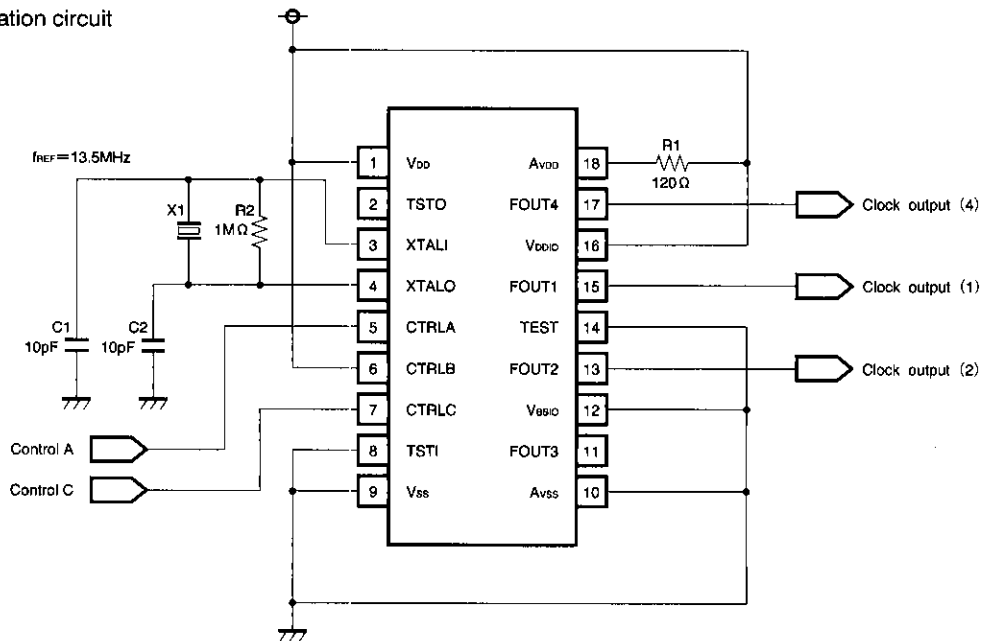


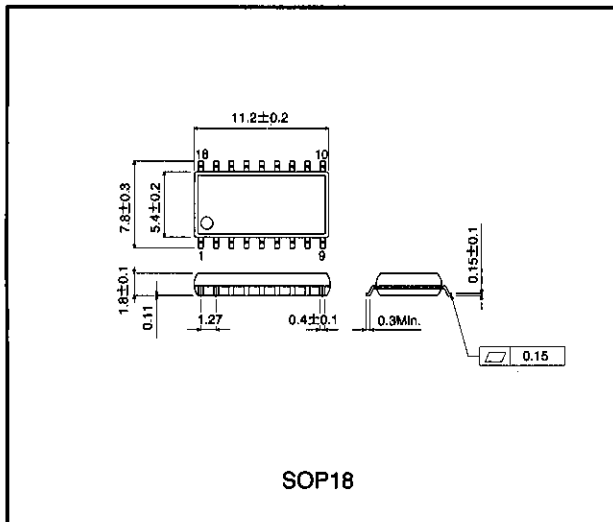
Fig. 2

Note: Certain crystal resonators may require setting XTALI and XTALO to the optimum allowable values.

●Attached components

- R1 : To keep the voltage of  $A_{VDD}$  effectively low, and to enhance signal stability by separating  $A_{VDD}$  and  $D_{VDD}$  with an impedance. Be sure to attach.
- R2 : Needed to provide a feedback resistance for the crystal resonator.
- C1/C2 : When  $f_0$  must be adjusted according to the crystal resonator used, or when the crystal resonator results in unnecessary oscillation points, attach a PF and adjust according to the value for this capacitor.
- X1 : Use a crystal resonator with an oscillation frequency of 13.5MHz or 14.318MHz.

●External dimensions (Units: mm)



Clock generator

Personal computers

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