PRELIMINARY DATA SHEET

ASI 3560A
Audio Stream Interface

MICRONAS
INTERMETALL

MICRONAS

INTERMETALL

Contents

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Audio Stream Interface

1. Introduction

The ASI 3560A audio stream interface offers the integration of digital audio data into a digital component video stream. Combined with a video decoder of the VPX 32xx family and an audio demodulator of the MSP 34xx family, the generated output stream contains video, audio, and VBI data (e.g. teletext, intercast, etc.). This configuration enables single-board plug-and-play tuner cards without extra wiring of audio signals.

Since the ASI 3560A multiplexes arbitrary serial data into a video stream, it is generally applicable and not limited to audio data.

1.1. Features

– guarantees synchronized digital video and audio

– I^2S interface for audio data (Sony and Philips format)

– transmission as horizontal or vertical ancillary data possible

– fully programmable audio window within the video stream

– sample rates up to 32 kHz with 16-bit stereo during transmission in the vertical blank interval.

– sample rates up to 48 kHz with 16-bit stereo during transmission in the horizontal blank interval.

– compliant to ITU-R 601-5 video stream format

– compliant to ITU-R 656-3 video stream format

– controlling via I^2C interface

– IEEE 1149.1 (JTAG) boundary scan interface

– low-power / stand-by mode

– 44-pin PLCC package
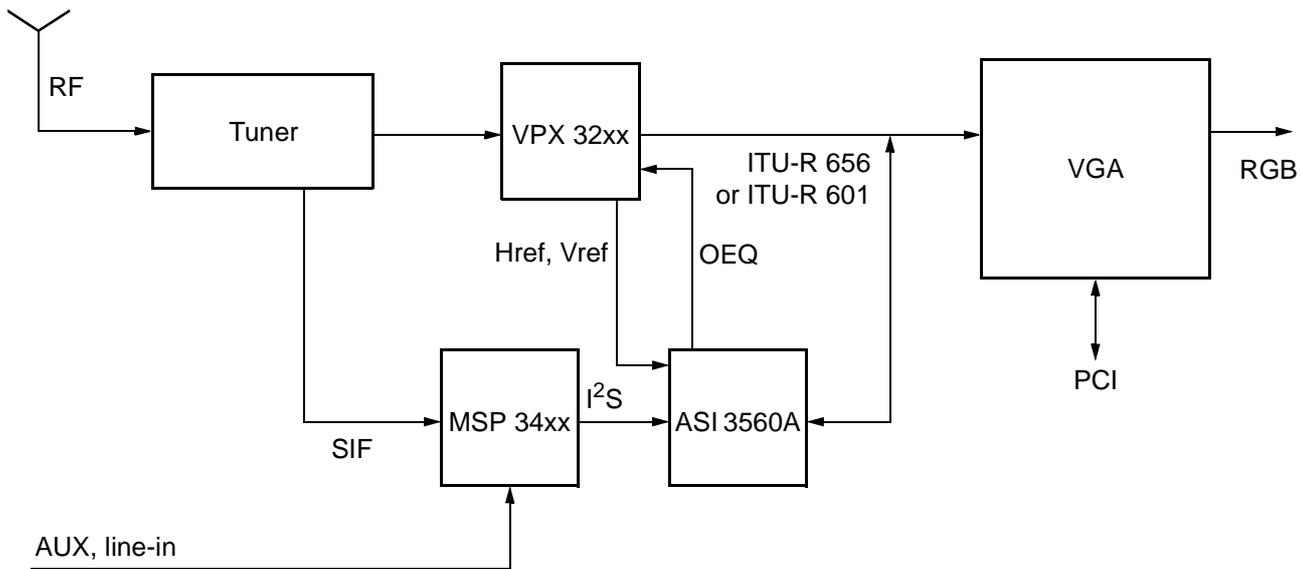
Fig. 1–1: Application example

2. Functional Description

2.1. Architecture of the ASI 3560A

The principal task of the ASI 3560A is to buffer incoming serial digital data in a FIFO and multiplex them blockwise into a digital video component stream during the vertical or horizontal blanking interval (VBI, HBI), when no video data is transmitted. Figure 2–1 shows a simplified block diagram of the IC architecture.

The Sync-Detection unit determines the actual position within the stream by evaluating the video reference signals (ITU-R 601 mode) or scanning the video bus itself for sync information (ITU-R 656 mode).

The control unit detects the reaching of the programmed audio window, disables the video decoder output, and initiates the writing of the FIFO data to the bus.

Since the data block format is compliant to the ITU-R 656 specification, every data packet is preceded with a header and followed by a checksum, which is generated by a Format Generation block.

The configuration of the interfaces, the positioning of the data window, and most parts of the transmission format face.
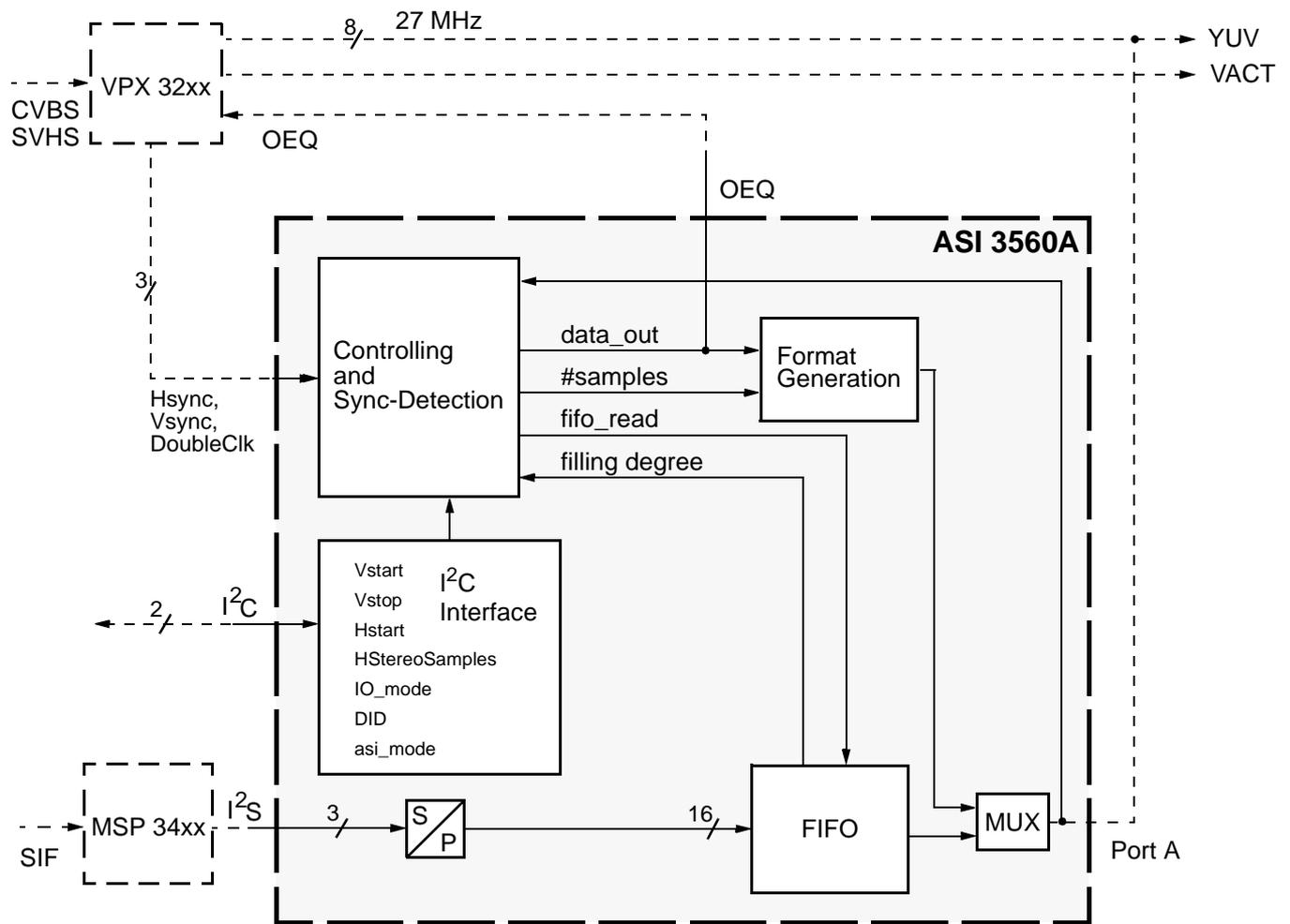
Fig. 2–1: Block diagram of the ASI 3560A

2.2. Synchronization to the Video Stream

The ASI 3560A is capable of dealing with the following video stream formats:

– YUV 4:2:2, ITU-R 601-5, 8 bit, double clock

– YUV 4:2:2, ITU-R 656-3

Although the generated data outputs are identical, the determination of the window position is completely different for both standards. While the ITU-R 601-5 specification uses additional signals to transmit the sync-information, the ITU-R 656-3 recommendation inserts sync information in the video stream itself and thus reduces the necessary number of wires.

The ASI 3560A begins with the output of an ancillary header, followed by audio data, if the internal line counter is within the values of the I^2C-registers 'VStart' and 'VStop' and the pixel counter reaches the value of the 'HStart' register.

The internal counters are reset with the related sync-information: reference signals or headers. Therefore, the absolute window position within the video stream determined by the I^2C registers ('VStart', 'VStop', HStart', and 'HStereoSamples') depends on the selected sync-mode.

2.2.1. Synchronization to Vref and Href

If bit[5] of the 'IO_mode' register (see Table 3–2 on page 18) is zero, the ASI 3560A determines the audio window position relative to the Vref and Href signals of an ITU-R 601 compliant video interface. The internal counters are reset with the first slope of the regarded reference signal. For proper detection, the polarity of the reference signals has to be specified with bits[0:1] of the 'IO_mode' register.

For video conferencing applications, a selection of the field is possible indicated by bit[8:7] of the 'IO_mode'-register. The field is identified by the relation between Vref and Href as depicted in Figure 2–2 and Figure 2–3.

2.2.2. Synchronization to the SAV/EAV Header

If bit[5] of the 'IO_mode' register (see Table 3–2 on page 18) is set to "1", the ASI 3560A determines the audio window position by evaluating the V- and H-flag of the SAV (bit[6] = 0) or the EAV (bit[6] = 1) headers of an ITU-R 656 data stream (see Table 2–1 on page 8). The internal line counter is reset to zero with every V-flag equal to "1". The pixel counter starts counting from zero if the H-flag equals bit[6] of the 'IO_mode' register. The upper left corner of the audio window is reached when these internal counters equal the registers 'VStart' and 'HStart'.

For video conferencing applications, a selection of the field is possible indicated by bit[8:7] of the 'IO_mode'-register. The field is identified by evaluating the F-Flag in the SAV and EAV header, respectively, and data packets are inserted only in the selected field.
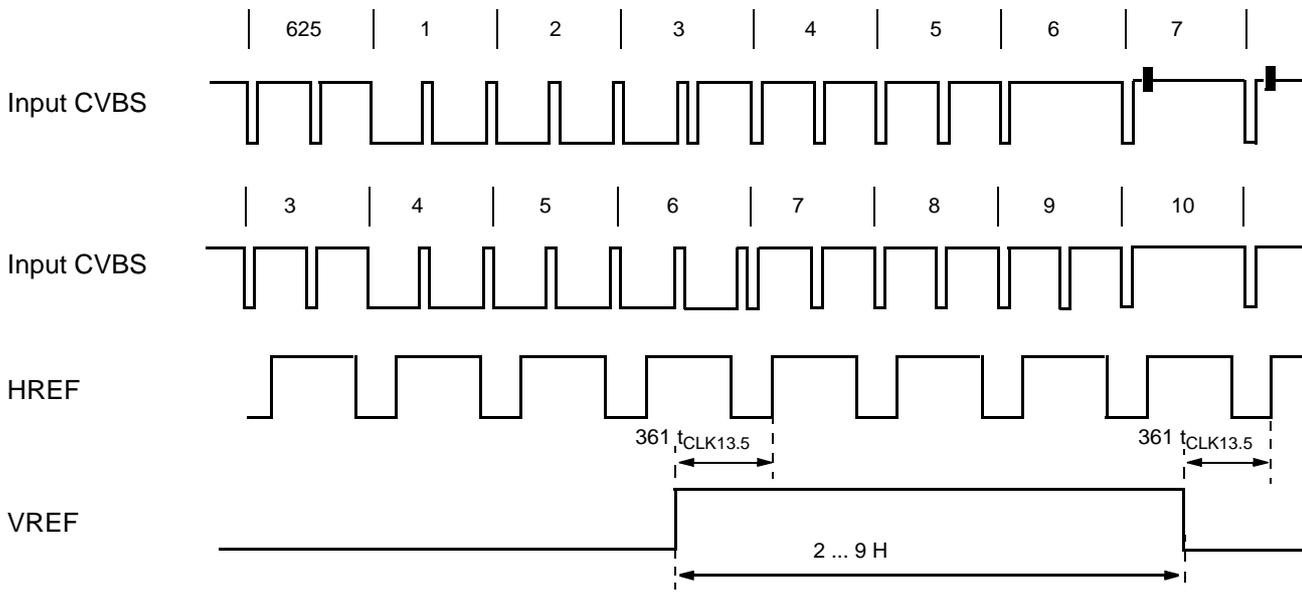
Fig. 2–2: Expected VREF timing for ODD fields

312 | 313 | 314 | 315 | 316 | 317 | 318 | 319 | 320

Input CVBS

265 | 266 | 267 | 268 | 269 | 270 | 271 | 272 | 273

Input CVBS

HREF

VREF

46 $t_{CLK13.5}$

46 $t_{CLK13.5}$

2 .. 9 H
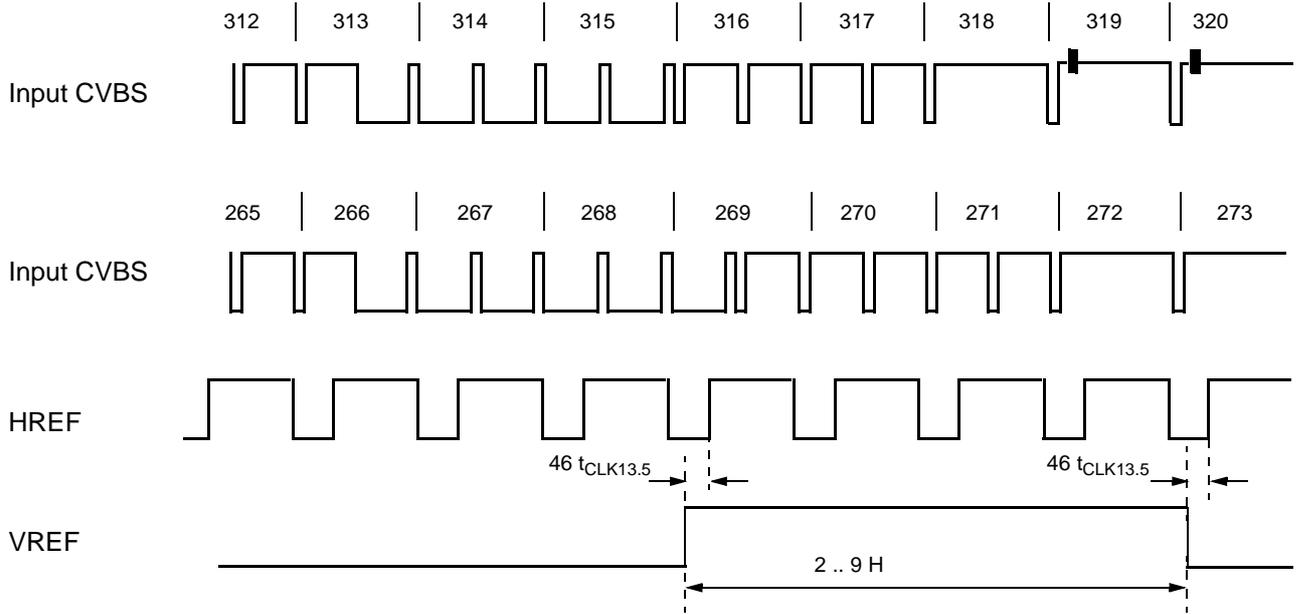
Fig. 2–3: Expected VREF timing for EVEN fields

dependent on video window size

current line-length

Digital Video

EAV

SAV

C_B Y C_R Y ...

EAV

SAV

C_B Y C_R Y ...

constant during horizontal blanking

SAV: "start of active video" header
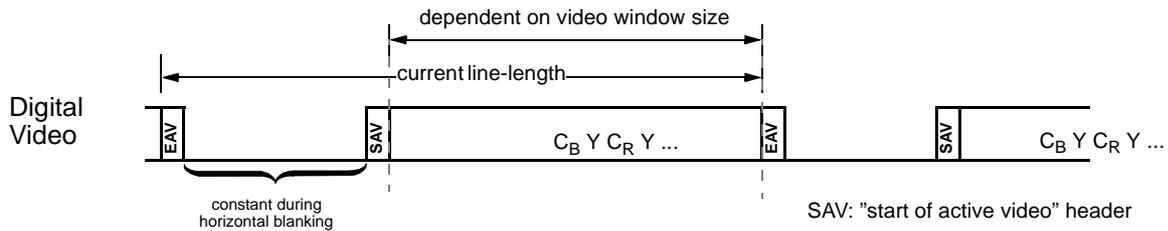
Fig. 2–4: Component video stream with embedded reference headers (according to ITU-R656)

DATA

80h | 10h | SAV_1 | SAV_2 | SAV_3 | SAV_4 | C_{B1} | Y_1 | C_{R1} | Y_2 | C_{Bn-1} | Y_{n-1} | C_{Rn-1} | Y_n | EAV_1 | EAV_2 | EAV_3 | EAV_4 | 80h | 10h

LLC
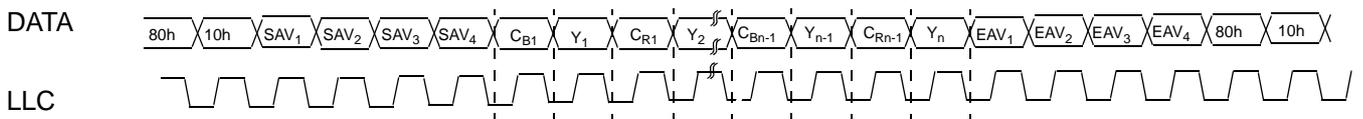
Fig. 2–5: Detailed video stream

dependent on video decoder

dependent on Audio-window size

current line-length

Digital Video

EAV

SAV

ANC

D_1 D_2 D_3 D_4 ...

Chks

EAV

SAV

C_B Y C_R Y ...

constant during horizontal blanking

ANC : Ancillary Header
Dx : User Data Words
Chks: Checksum

SAV: "start of active video" header
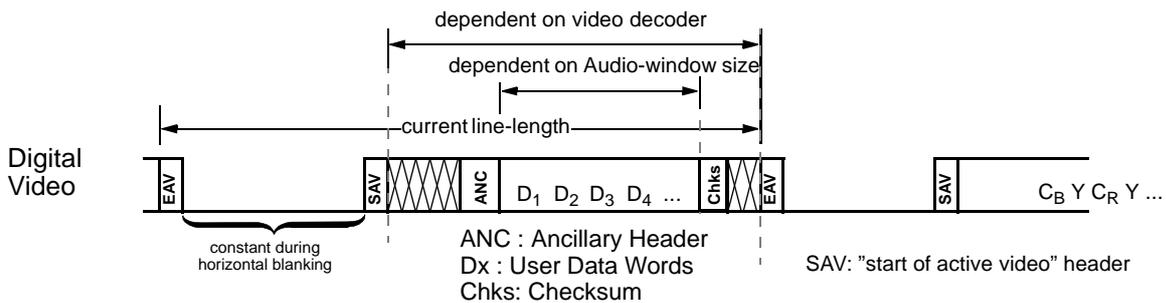
Fig. 2–6: Insertion of ancillary data in the VBI

Table 2–1: Coding of SAV/EAV-header (ITU-R 656 specification)

words	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	
First	1	1	1	1	1	1	1	1	$FF
Second	0	0	0	0	0	0	0	0	$00
Third	0	0	0	0	0	0	0	0	$00
Fourth	1	F	V	H	P5	P4	P3	P2	Sync information

F = 0 during field 1
V = 0 elsewhere
H = 0 in SAV

F = 1 during field 2
V = 1 during vertical field blanking
H = 1 in EAV

P2, P3, P4, and P5 are protection bits, which are not regarded by the ASI 3560A

Table 2–2: Coding of the ancillary header (compliant to ITU-R 656-3 recommendation)

words	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	
First	0	0	0	0	0	0	0	0	$00
Second	1	1	1	1	1	1	1	1	$FF
Third	1	1	1	1	1	1	1	1	$FF
Fourth	$\overline{\text{bit 8}}$	even parity	T7	T6	T5	T4	T3	T2	Data ID (programmable)
Fifth	$\overline{\text{bit 8}}$	even parity	N7	N6	N5	N4	N3	N2	Data Block Number (DBN)
Sixth	$\overline{\text{bit 8}}$	even parity	C7	C6	C5	C4	C3	C2	Data Count (DC)

2.3. Ancillary Data Format

Ancillary packets are transferred compliant to the draft recommendation ITU-R BT.[11-2/AD] with the following extensions:

– Ancillary data blocks may be longer than 255 bytes INTERMETALL extended mode, see Table 3–2)

– Ancillary data packets must not follow immediately after EAV or SAV.

The ASI 3560A always generates an ancillary header for each line, which is compliant to the ITU-R 656 video stream format, even in ITU-R 601 mode. The coding of the headers is depicted in Table 2–2.

If the VGA controller cannot deal with ancillary data packets, audio data can be transmitted together with video data in the active video interval. Therefore, the preamble $00 FF FF can be modified to $80 7F 7F with bit[2] of the 'IO_mode' register, which assures correct SAV/EAV-detection.

The 8-bit (incl. parities!) of the Data ID (DID) are programmable to enable the user the freedom of specifying his serial data compliant to any future recommendation.
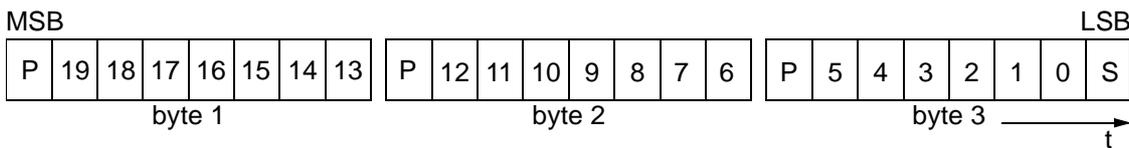
The Data Block Number (DBN) counts the ancillary data packets if its value is not forced to zero (which means $80 with parities) with bit[3] of the 'IO_mode' register (see Table 3–2 on page 18).

The Data Count (DC) word depends on the setting of bit[4] of the 'IO_mode' register. If it is set to zero, the DC determines the number of following DWords (32 bit = 4 cycles) compliant to the ITU-R 656-3 recommendation and is therefore limited to 255 User Data Words (UDW). In order to allow the usage of longer packets, a so-called INTERMETALL extended mode may be used by setting bit[4] to one. In this case, the whole 8 bit represents the number of 6 byte packets, which equals the number of stereo samples. Please note that there are no longer any parities transmitted.

A successive checksum is added behind the audio data packages, which are transmitted in a format described in section 2.4. The checksum consists of the sum of the seven LSBs of DID, DBN, DC, and all UDWs (user data words) within the modulo range of 7 bit. Since the ASI 3560A supports only an 8-bit protocol, the checksum means the modulo addition of the bits 2..8 concerning the 10-bit ITU-R656 specification.

2.4. Data Transmission Format

The audio data is transferred in 6-byte packages, each containing one stereo sample. The protocol has been designed for 20-bit audio data (see Figure 2–7). The audio samples are always MSB aligned, which means a 16-bit sample is transferred in bit 4-19. The ASI status flag allows the user to determine problems without polling the I2C register 'asi_mode'.

MSB　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　LSB

P	19	18	17	16	15	14	13	P	12	11	10	9	8	7	6	P	5	4	3	2	1	0	S

byte 1　　　　　　　　　　　　byte 2　　　　　　　　　　　byte 3 ⟶
　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　t

P: odd parity (the number of ones in the whole byte is odd),
S: ASI status flag (0: data valid, 1: error / read asi_mode register for further information)

Fig. 2–7: Transmission format of the audio data

2.5. Reset / Standby-Mode / Operation Mode

The ASI 3560A distinguishes between two kinds of reset, an external and an internal reset. The external hardware or power-on-reset leads to the stand-by mode. The internal reset is evoked by an I²C command and switches from stand-by to an operation mode.

The stand-by mode is the default mode at the startup and requires the LLC clock from the video demodulator, e.g. a VPX32xx. Without this clock, the ASI 3560A is switched off completely and is in the so-called sleep mode.

The I²C interface has its own sleep mode which is independent of the IC's stand-by mode. When a start condition is sensed, the I²C interface becomes active and performs an I²C transaction, e.g. receiving a telegram. After the stop condition has been sensed, the I²C interface automatically returns to its sleep mode. If the I²C interface has received the correct wakeup sequence for ASI3560A (setting bit[0] of the 'asi_mode' register to one), the ASI 3560A leaves its standby mode and enters the 'sync mode'.

During the 'sync mode', the line and pixel counter are adjusted accordingly to Href/Vref or SAV/EAV, respectively. Please note that still no data is output.

Setting bit[1] of the 'asi_mode' register switches the ASI 3560A into the operation mode, but the output will stay disabled until the end of the specified audio window in the component stream has been detected. At this point, the FIFO and the I²S-interface are reset, so that the first transmitted audio window contains the correct audio samples collected during one field period.

In general, there are no timing constraints concerning the reset procedure, apart from the fact that the ASI 3560A requires the LLC clock from the video decoder for functionality. Therefore, the controller must wait until the video decoder generates this clock before it may send the ASI 3560A wake-up protocol. Please consult the data sheet of the video decoder for further information about the time between reset and the generation of the LLC clock.
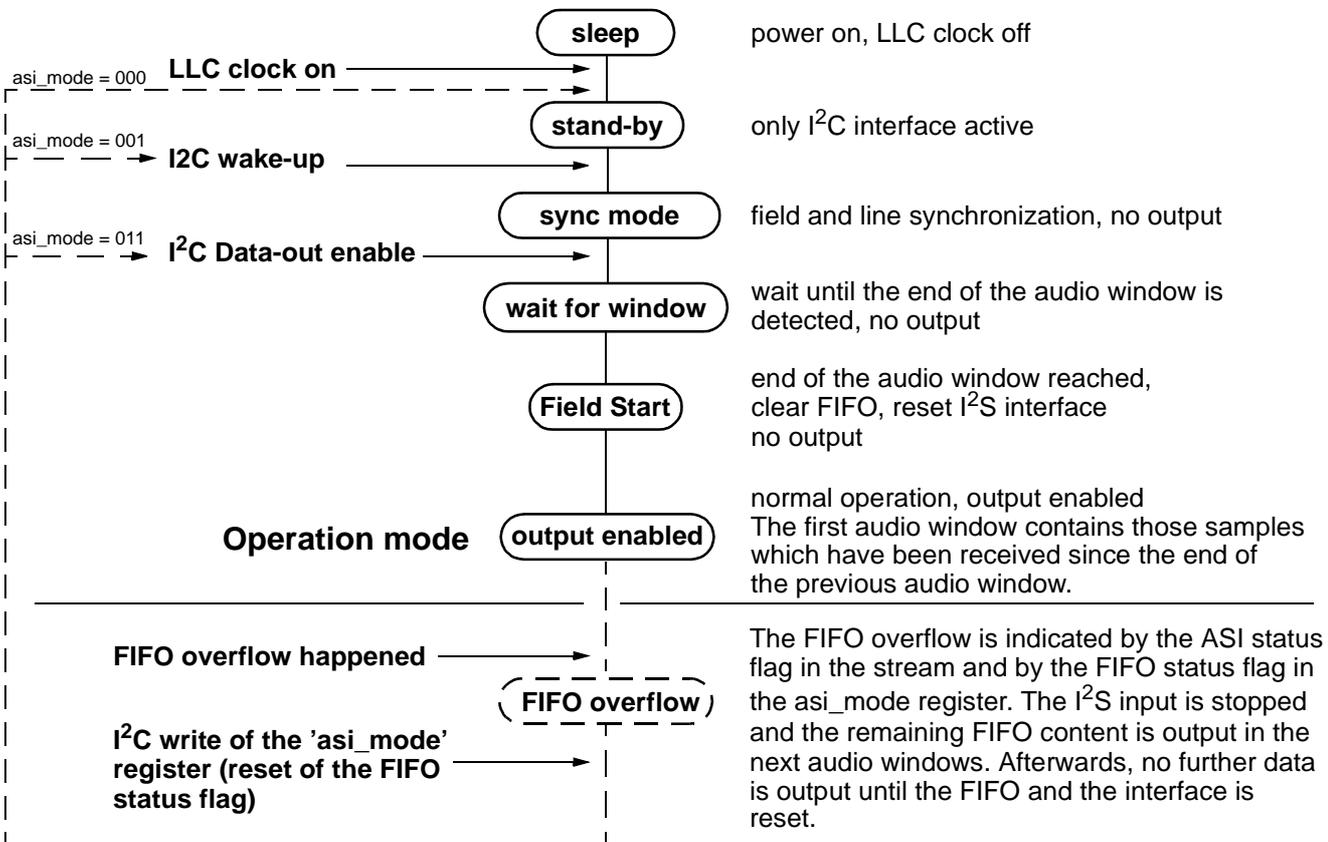

Fig. 2–8: Operation modes of the ASI 3560A

2.6. FIFO and Output Controlling

An internal state machine analyzes the incoming sync information from the video decoder (HREF,VREF, or sync headers) and derives the actual line number within the current field and the horizontal position within the line.

If the programmed audio window is detected, the state machine disables the output of the video decoder and initiates the generation of an ancillary header preceding valid audio data. After termination of the header, the reading of the assembled audio data from the internal FIFO is started.

The number of audio samples per ancillary packet is determined for each line independently. It depends on the FIFO filling level and the horizontal size of the audio window. The ASI 3560A attempts to output the data as fast as possible. If enough samples are available in the FIFO, the ancillary data packet containing audio samples will take up the maximum allowed horizontal space, otherwise an even number of samples from the available data will be output.

For clear identification of the left and right channel, data is always transmitted in packets of 6 bytes corresponding to one sample for each channel starting with the left one. For more details concerning the transmission format, see section 2.4.

The FIFO buffers the incoming continuous audio data stream. Its size of 3 kbytes is determined for the transmission of serial data with 128 kByte/s in the vertical blanking interval assuming a worst case scenario (50 Hz TV standard, 5% line frequency deviation, minimum number of lines used for the audio window).

In case of a FIFO overflow, the FIFO status bit in the 'asi_mode' register is set and the FIFO input is stopped. This means that the FIFO contains valid data which will be output in the following audio windows. Since the ASI status flag in the output data is set, the user can detect the overflow in time and can react with muting or even fading.

In order to restart the FIFO, the user has to reset the FIFO status flag in the 'asi_mode' control register. Please note that every write access to the 'asi_mode' register leads to a FIFO and I^2S interface reset if bit[2] is set to zero.

2.7. Video Stream Interface

The video interface of the ASI 3560A is bidirectional, because it works as an input interface during the sync-detection in the ITU-R 656 mode. Its output driver strength can be adjusted with the bits[11:13] of the 'IO_mode' register.

2.8. I^2S Interface

Audio data is received via an I^2S slave interface which accepts MSB first serial audio data with a resolution of 16 or more bits. However, the internal storage is limited to 16 bits per sample. The interface supports both the Philips and the Sony format. The required format can be selected with bit[9] of the 'IO_mode' register (see Table 3–2 on page 18). Additionally, the valid data bits can be left or right aligned - but still MSB first - within the data word (bit[10]).

Figure 2–9 shows the supported I^2S bus formats. The serial data is transmitted in two's complement with MSB first. The data is synchronized with the falling edge of the clock and latched at the rising edge.

A detailed description of the timing constraints can be found in section 4.6.3. on page 26 and section 4.8.7. on page 35.

The interface can handle data rates up to 4.1 Mbit/s, which means sample rates up to 130 kHz with 32 bit frames per sample and channel are possible.
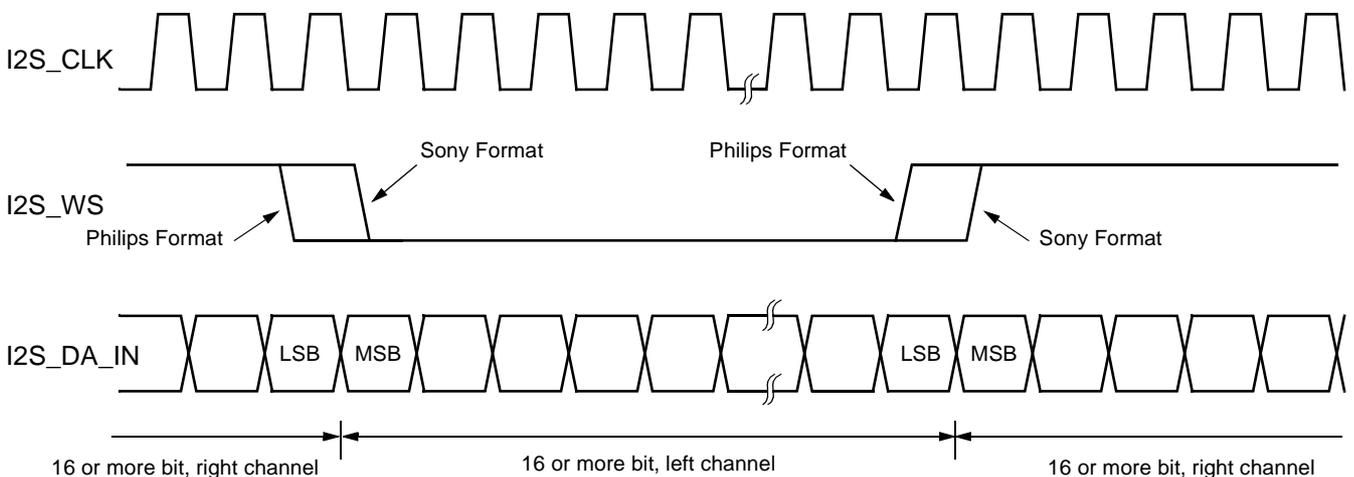

Fig. 2–9: I^2S bus transmission formats

2.9. JTAG Boundary-Scan, Test Access Port (TAP)

The design of the Test Access Port, which is used for Boundary-Scan Test, conforms to standard IEEE 1149.1-1990. Also included is a list of the mandatory instructions supported, as well as the optional instructions. The following comprises a brief overview of some of the basics, as well as any optional features which are incorporated. The IEEE 1149.1 document may be necessary for a more concise description. Finally, an adherence section goes through a checklist of topics and describes how the design conforms to the standard.

The implementation of the instructions HIGHZ and CLAMP conforms to the supplement P1149.1/D11 (October 1992) to the standard 1149.1-1990.

2.9.1. General Description

The TAP in the ASI 3560A is incorporated using the four signal interface. The interface includes TCK, TMS, TDI, and TDO. The optional TRESET signal is not used. This is not needed because the chip has an internal power-on-reset which will automatically steer the chip into the TEST-LOGIC-RESET state. The goal of the interface is to provide a means to test the boundary of the chip. There is no support for internal or BIST(built-in self test).

2.9.2. TAP Architecture

The TAP function consists of the following blocks: TAP-controller, instruction register, boundary-scan register, bypass register, optional device identification register, and master mode register.

2.9.2.1. TAP Controller

The TAP controller is responsible for responding to the TCK and TMS signals. It controls the transition between states of this device. These states control selection of the data or instruction registers and the actions which occur in these registers. These include capture, shifting, and update. See Fig. 5-1 of IEEE 1149.1 for TAP state diagram.

2.9.2.2. Instruction Register

The instruction register chooses which one of the data registers is placed between the TDI and TDO pins when the select data register state is entered in the TAP controller. When the select instruction register state is active, the instruction register is placed between the TDI and TDO.

Instructions

The following instructions are incorporated:

– bypass

– sample/preload

– extest

– master mode

– ID code

– HIGHZ

– CLAMP

2.9.2.3. Boundary Scan Register

The boundary scan register (BSR) consists of boundary scan cells (BSCs) which are distributed throughout the chip. These cells are located at or near the I/O pad. It allows sampling of inputs, controlling of outputs, and shifting between each cell in a serial fashion to form the BSR. This register is used to verify board interconnect.

Input Cell

The input cell is constructed to achieve capture only. This is the minimal cell necessary since Internal Test (INTEST) is not supported. The cell captures either the system input in the CAPTURE-DR state or the previous cells output in the SHIFT-DR state. The captured data is then available to the next cell. No action is taken in the UPDATE-DR state. See Figure 10-11 of IEEE 1149.1 for reference.

Output Cell

The output cell will allow both capture and update. The capture flop will obtain system information in the CAPTURE-DR state or previous cells information in the SHIFT-DR state. The captured data is available to the next cell. The captured or shifted data is downloaded to the update flop during the UPDATE-DR state. The data from the update flop is then multiplexed to the system output pin when the EXTEST instruction is active. Otherwise, the normal system path exists where the signal from the system logic flows to the system output pin. See Fig. 10-12 of IEEE 1149.1 for reference.

Tristate Cell

Each group of output signals, which are tristatable, is controlled by a boundary scan cell (output cell type). This allows either the normal system signal or the scanned signal to control the tristate control. In the ASI 3560A, there is only one such tristate control cell for the OEQ (see section "Output Driver Tristate Control" for further information).

Bidirect Cell

The bidirect cell is comprised of an input cell and a tristate cell as described in the IEEE standard. The port A is a bidirectional tristatable port, while the SDA port is purely bidirectional.

2.9.2.4. Bypass Register

This register provides a minimal path between TDI and TDO. This is required for complicated boards where many chips may be connected in serial.

2.9.2.5. Device Identification Register

This is an optional 32-bit register which contains the MICRONAS INTERMETALL identification code (JEDEC controlled), part and revision number. This is useful in providing the tester with assurance that the correct part and revision are inserted into a PCB.

2.9.2.6. Master Mode Data Register

This is an optional register used to control an 8-bit test register in the chip. This register supports shift and update. No capture is supported. This was done so that the last word can be shifted out for verification.

2.9.3. IEEE 1149.1-1990 Spec Adherence

This section defines the details of the IEEE1149.1 design for the ASI 3560A. It describes the function as outlined by IEEE1149.1, section 12.3.1. The section of that document is referenced in the description of each function.

2.9.3.1. Instruction Register

(Section 12.3.1.b.i of IEEE 1149.1-1990)

The instruction register is three bits long. No parity bit is included. The pattern loaded in the instruction register during CAPTURE-IR is binary "101" (MSB to LSB). The two LSBs are defined by the spec to be "01" (bit 1 and bit 0) while the MSB (bit 2) is set to "1".

2.9.3.2. Public Instructions

(Section 12.3.1.b.ii of IEEE 1149.1-1990)

A list of the public instructions can be found in Table 2–3.

Table 2–3: Public instructions

Instruction	Code (MSB to LSB)
EXTEST	000
SAMPLE/PRELOAD	001
ID CODE	010
MASTER MODE	011
HIGHZ	100
CLAMP	110
BYPASS	100 - 111

The EXTEST and SAMPLE/PRELOAD instructions both apply the boundary scan chain to the serial path. The ID CODE instruction applies the ID register to the serial chain. The BYPASS, the HIGHZ, and the CLAMP instructions apply the bypass register to the serial chain.

The MASTER MODE instruction is a test data instruction for public use. It provides the ability to control an 8-bit test register in the chip.

2.9.3.3. Self-Test Operation

(Section 12.3.1.b.iii of IEEE 1149.1-1990).

There is no self-test operation included in the ASI 3560A design which is accessible via the TAP.

2.9.3.4. Test Data Registers

(Section 12.3.1.b.iv of IEEE 1149.1-1990).

The ASI 3560A includes the use of four test data registers. They are the required bypass and boundary scan registers, the optional ID code register, and the master mode register.

The bypass register is, as defined, a 1-bit register accessed by codes 100 through 111, inclusive. Since the design includes the ID code register, the bypass register is not placed in the serial path upon power-up or Test-Logic-Reset.

The master mode is an 8-bit test register which is used to force the ASI 3560A into special test modes. This is reset upon power-on-reset. This register supports shift and update only. It is not recommended to access this register. The loading of that register can drive the IC into an undefined state.

2.9.3.5. Boundary Scan Register

(Section 12.3.1.b.v of IEEE 1149.1-1990)

The boundary scan chain has a length of 29 shift registers. The scan chain order is specified in Table 2–4

2.9.3.6. Device Identification Register

(Section 12.3.1.b.vi of IEEE 1149.1-1990)

The manufacturer's identification code for MICRONAS INTERMETALL is "6C"$_{(hex)}$. The general implementation scheme uses only the 7 LSBs and excludes the MSB, which is the parity bit. The part number is 3010$_{hex}$ in case of ASI 3560A. The version code starts from "1"$_{(hex)}$ and changes with every revision. The version number relates to changes of the chip interface only.

Version	Part Number	7F	Manufacturer ID
0 0 0 1	0 0 1 1 0 0 0 0 0 0 0 1 0 0 0 0	0 0 0 0	1 1 0 1 1 0 0 1

31   28 27   12 11   8 7   1 0

   1   3   0   1   0   0   d   9
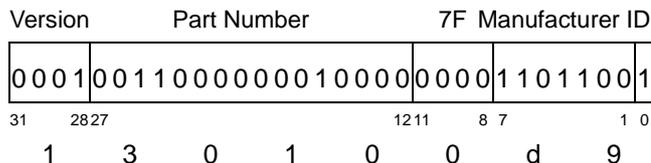
Fig. 2–10: Device identification register

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Table 2–4: Scan chain order

No.	Pin	Mode
1	VREF	input
2	HREF	input
3	I^{2}S_WS	input
4	I^{2}S_CLK	input
5	I^{2}S_DA_IN	input
6	RESQ	input
7	SCL	input
8	SDA	output
9	SDA	input
10	LLC	input
11	OEQ	tristate
12	OEQ	output
13	A[7:0]	tristate
14	A[0]	output
15	A[0]	input
16	A[1]	output
17	A[1]	input
18	A[2]	output
19	A[2]	input
20	A[3]	output
21	A[3]	input
22	A[4]	output
23	A[4]	input
24	A[5]	output
25	A[5]	input
26	A[6]	output
27	A[6]	input
28	A[7]	output
29	A[7]	input

TAP State Transitions

TDO could be used as programmable output pin or LLC2 clock signal (see Pin Description).

State transitions are dependent on the value of TMS, synchronized by TCK.
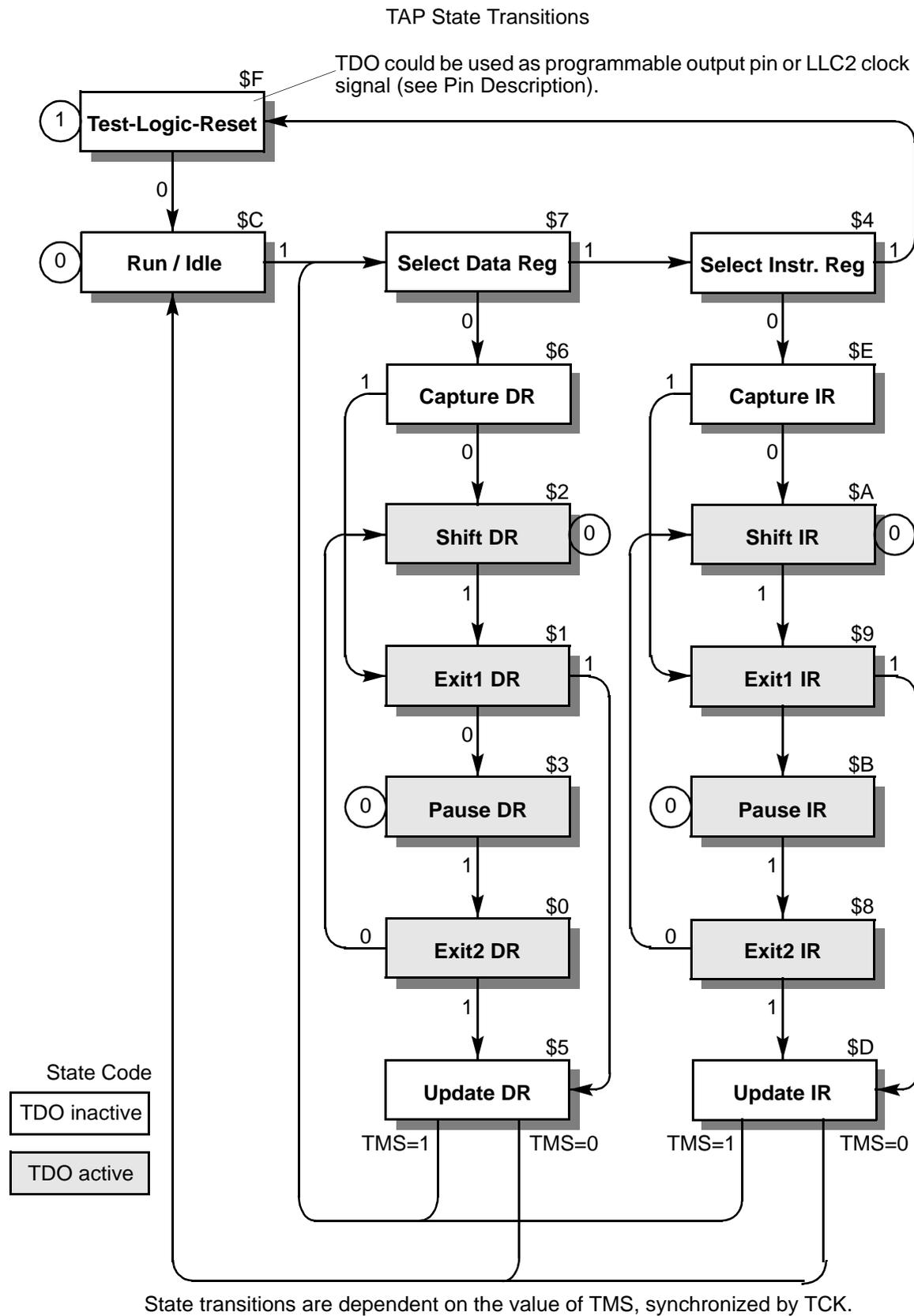
Fig. 2–11: TAP state transitions

2.9.3.7. Performance

(Section 12.3.1.b.vii of IEEE 1149.1-1990)

See section "Specification" for further information.

2.10. Enable/Disable of Output Signals

In order to enable the output pins of the ASI 3560A to achieve the high impedance/tristate mode, various controls have been implemented. The following paragraphs give an overview of the different tristate modes of the output signals.

BS (Boundary Scan) Mode:

The tristate control by the test access port TAP for boundary scan has the highest priority. Even if the TAP-controller is in the EXTEST or CLAMP mode, the tristate behavior is only defined by the state of the different boundary scan registers for enable control. If the TAP controller is in HIGHZ mode, then all output pins are in tristate mode independent of the state of the different boundary scan registers for enable control.

RESET State:

If the TAP-controller is not in the EXTEST mode, then the RESET-state defines the state of all digital outputs. The only exception is made for the data output of the boundary scan interface TDO. If the circuit is in reset condition ($\overline{RES} = 0$), then all output interfaces are in tristate mode.

3. I²C Bus Interface

The ASI 3560A configurations are programmable via an I²C bus slave control interface. Only one level of subaddressing is used, which means the first bus address selects the device; the second, the internal register. The device address is given in Table 3–1, a list of the available I²C registers in Table 3–2.

The I²C interface of the ASI 3560A conforms to the specification for the I²C-fast-mode. If the power supply of the ASI 3560A is switched off, both pins SCL and SDA float. external pull-up devices must be adapted to fulfill the required rise time for the fast-mode. For bus loads up to 200 pF, the pull-up device could be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit.

Please note, that the I²C control interface requires the LLC clock to work, which means that the chip cannot be addressed, if the VPX is in sleep mode
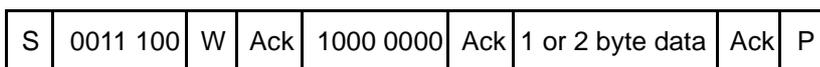
Table 3–1: I²C Device Address

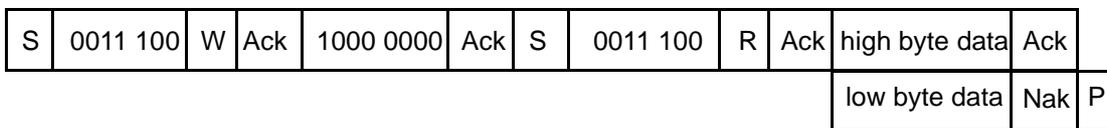| Mode	Write	Read
ASI 3560A device address	38_{hex}	39_{hex}

3.1. Protocol Description

Once the reset is complete, the IC is selected by asserting the device address in the address part of a I²C transmission. A device address pair is defined as a write address (38_{hex}) and a read address (39_{hex}). Writing is done by sending the device write address first, followed by the subaddress byte and one or two data bytes. For reading, the read subaddress has to be transmitted, first, by sending the device write address (38_{hex}) followed by the subaddress, a second start condition with the device read address (39_{hex}), and reading one or two bytes of data. It is not allowed to send a stop condition in between. This will result in reading erratic data.

The registers of the ASI 3560A have 8 or 16- bit data size; 16-bit registers are accessed by reading/writing two 8-bit data bytes with the high byte first. The order of the bits in a data/address/subaddress byte is always MSB first.

Figure 3–1 shows the I²C bus protocols for read and write operations; the read operation requires an extra start condition after the subaddress and repetition of the read chip address, followed by the read data bytes.

Example:

I²C write access subaddress 80_{hex}

| S | 0011 100 | W | Ack | 1000 0000 | Ack | 1 or 2 byte data | Ack | P |

I²C read access subaddress 80_{hex}

| S | 0011 100 | W | Ack | 1000 0000 | Ack | S | 0011 100 | R | Ack | high byte data | Ack |
| | | | | | | | | | | low byte data | Nak | P |
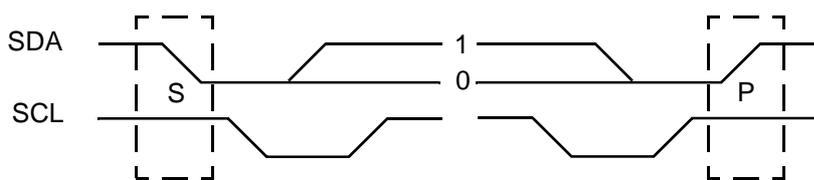
W = 0
R = 1
Ack = 0
Nak = 1
S = Start
P = Stop

Fig. 3–1: I²C bus protocol (MSB first)

3.2. Control Registers

Table 3–2 contains a list of the available registers. The start initialization for all registers apart from I2C_IDx and Ver_NR is zero. For the asi_mode register this means that the chip is in stand-by mode after a reset.

Table 3–2: I^2C Register Table

| I^2C Reg. Address	Number of bits	Mode[1]	Function	Name
00_{hex}	8 / 8	r	Manufacture ID in accordance with JEDEC Solid State Products Engineering Council, Washington DC MICRONAS INTERMETALL Code EC_{hex}	I2C_ID0
$01 / 02_{hex}$	8 / 8	r	16-bit part number: 3010_{hex} (01: LSBs, 02: MSBs)	I2C_ID1, I2C_ID2
03	8 / 8	r	Version number: 01_{hex}	Ver_NR
80_{hex}	9 / 16	w / r	start line of the audio data window within a field	VStart
81_{hex}	9 / 16	w / r	end line of the audio data window within a field	VStop
82_{hex}	10 / 16	w / r	horizontal start position relative to the trailing edge of Href (2 bytes packets), minimum allowed value is 3 (means 6bytes).	HStart
$7F_{hex}$	8 / 8	w / r	number of stereo samples (6 byte) per line	HStereoSamples
84_{hex}	11 / 16	w / r	interface mode register	IO_mode

			bit[0] : Href polarity
			     0 : active high
			     1 : active low
				hpol

			bit[1] : Vref polarity
			     0 : active high
			     1 : active low
				vpol

			bit[2] : ANC preamble modification
			     0 : standard header (00_h FF_h FF_h)
			     1 : modified header (80_h $7F_h$ $7F_h$)
				preamod

			bit[3] : Data block number (DBN) mode
			     0 : every ancillary data packet is counted with 6-bit counter
			     1 : DBN is always set to $80
				dbn_mod

			bit[4] : data count (DC) mode
			     0 : Standard mode (counting DWords)
			     1 : INTERMETALL extended mode (8-bit counting 6 byte packages, no parities !)
				dc_mode

Table 3–2: I^{2}C Register Table, continued

I^{2}C Reg. Address	Number of bits	Mode[1]	Function	Name

84$_{hex}$	11 / 16	w / r	bit[6:5] : ITU-R656 header detection enable
			    0 0 : use Vref and Href
			    0 1 : scan video component stream and synchronize to SAVs
			    1 1 : scan video stream and synchronize to EAVs
				scanstream

			bit[8:7] : Field usage
			    0 0 : every field
			    0 1 : every odd field
			    1 1 : every even field
				field_select

			bit[9] : I^{2}S mode
			    0 : Japanese
			    1 : Philips
				I2S_mode

			bit[10] : I^{2}S alignment
			    0 : left aligned within data word, MSB first
			    1 : right aligned within data, MSB first
				I2S_align

			bit[13:11] : driver strength of port A[7:0]	stra1
10$_{hex}$	8 / 8	w / r	Data ID in ANC-header	DID
08$_{hex}$	3 / 8	w / r	Stand-by, control	asi_mode

			bit[1:0] : operation mode control
			    0 0 : stand-by mode (default)
			    0 1 : sync mode, output disabled
			    1 1 : data out enable
				asi_state

			bit[2] : FIFO control flag
			    read : FIFO status flag (1 : overflow)
			    write : 0 - reset FIFO and synchronize
				status

1) w: writable, r: readable

4. Specifications

4.1. Outline Dimensions
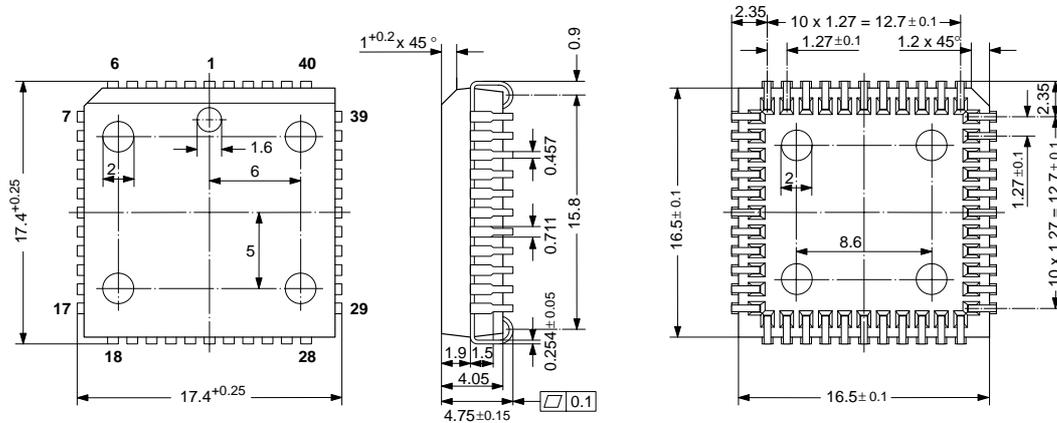
SPGS7003-2/2E

Fig. 4–1:
44-Pin PLCC Plastic Leaded Chip Carrier Package
(PLCC44)
Weight approximately 2.5 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
LV = if not used, leave vacant

S.T.B. = shorted to BAGNDI if not used
DVSS = if not used, connect to DVSS
X = obligatory; connect as described in circuit diagram
AHVSS = connect to AHVSS

Pin No. PLCC 44-pin	Pin Name	Type	Connection (If not used)	Short Description
1	TDO	OUT	NC	Boundary-Scan-Test Data Output
2	TMS	IN	NC	Boundary-Scan-Test Mode Select
3	NC		LV	not connected
4	TDI	IN	NC	Boundary-Scan-Test Data Input
5	NC		LV	not connected
6	VREF	IN		vertical reference
7	HREF	IN		horizontal reference
8	NC		LV	not connected
9	I2S_WS	IN		I^2S word select
10	NC		LV	not connected
11	I2S_CLK	IN		I^2S clock
12	VDD	SUPPLY	X	supply voltage for digital circuitry
13	VSS	SUPPLY	X	supply voltage for digital circuitry

Pin No. PLCC 44-pin	Pin Name	Type	Connection (If not used)	Short Description
14	NC		LV	not connected
15	I2S_DA_IN	IN		I^{2}S data input
16	NC		LV	not connected
17	RESQ	IN		reset input
18	SCL	IN/OUT		I^{2}C clock
19	NC		LV	not connected
20	SDA	IN/OUT		I^{2}C data
21	NC		LV	not connected
22	LLC	IN		double clock (27 MHz)
23	NC		LV	not connected
24	OEQ	OUT		disable video output
25	NC		LV	not connected
26	A0	IN/OUT		video data port
27	NC		LV	not connected
28	A1	IN/OUT		video data port
29	A2	IN/OUT		video data port
30	NC		LV	not connected
31	A3	IN/OUT		video data port
32	NC		LV	not connected
33	PVSS	SUPPLY	X	supply voltage pad circuits
34	NC		LV	not connected
35	PVDD	SUPPLY	X	supply voltage pad circuits
36	NC		LV	not connected
37	A4	IN/OUT		video data port
38	NC		LV	not connected
39	A5	IN/OUT		video data port
40	A6	IN/OUT		video data port
41	NC		LV	not connected
42	A7	IN/OUT		video data port
43	NC		LV	not connected
44	TCK	IN	NC	Boundary-Scan-Test Clock Input

4.3. Pin Descriptions

Pins 2, 4 - JTAG Input Pins TMS, TDI (Fig. 4–4)
Test Mode Select and Test Data Input signals of the JTAG Test Access Port (TAP). Both signals are inputs with a TTL compatible input specification. To comply with JTAG specification, they use pull-ups at their input stage. The input stage of the TMS and TDI uses a TTL Schmitt Trigger.

Pin 44 - JTAG Input Pin TCK (Fig. 4–3)
Clock signal of the Test-Access Port. It is used to synchronize all JTAG functions. When JTAG operations are not being performed, this pin should be driven to VSS. The input stage of the TCK uses a TTL Schmitt Trigger.

Pin 1 - JTAG Output Pin TDO (Fig. 4–7)
Data output for JTAG Test Access Port (TAP).

Pins 9 - I^2S Wordstrobe I2S_WS (Fig. 4–3)
This pin connects to the I^2S bus wordstrobe line.

Pins 11 - I^2S Clock I2S_CLK (Fig. 4–3)
This pin connects to the I^2S bus clock line.

Pins 15 - I^2S Data I2S_DA_IN (Fig. 4–3)
This pin connects to the I^2S bus data line.

Pins 6,7 - Reference Signals VREF, HREF (Fig. 4–3)
These signals are sync signals generated by the video decoder (e.g. VPX).

Pins 26,28,29,31,37,39,40,42 - Video Port A[7:0] (Fig. 4–8)

Pin 35 - Supply Voltage, Pad Circuitry PVDD

Pins 22 - LLC (Fig. 4–3)
LLC is the reference clock signal for the video bus connected to port A[7:0].

Pin 33- Ground, Pad Circuitry PVSS

Pin 24 - Output Enable Output Signal OEQ (Fig. 4–6)
The output enable output signal has TTL output characteristic. It controls the tri-state condition of the video ports of the video demodulator (e.g. VPX. Please note that the state during the positive edge of RESQ selects the I^2C device address of a VPX).

Pin 20 - I^2C Data SDA (Fig. 4–5)
This pin connects to the I^2C bus data line.

Pin 18 - I^2C Clock SCL (Fig. 4–5)
This pin connects to the I^2C bus clock line.

Pin 17 - Reset Input RESQ (Fig. 4–3)
A low level on this pin resets the circuit.

Pin 13 - Ground, Digital Circuitry VSS

Pin 12 - Supply Voltage, Digital Circuitry VDD
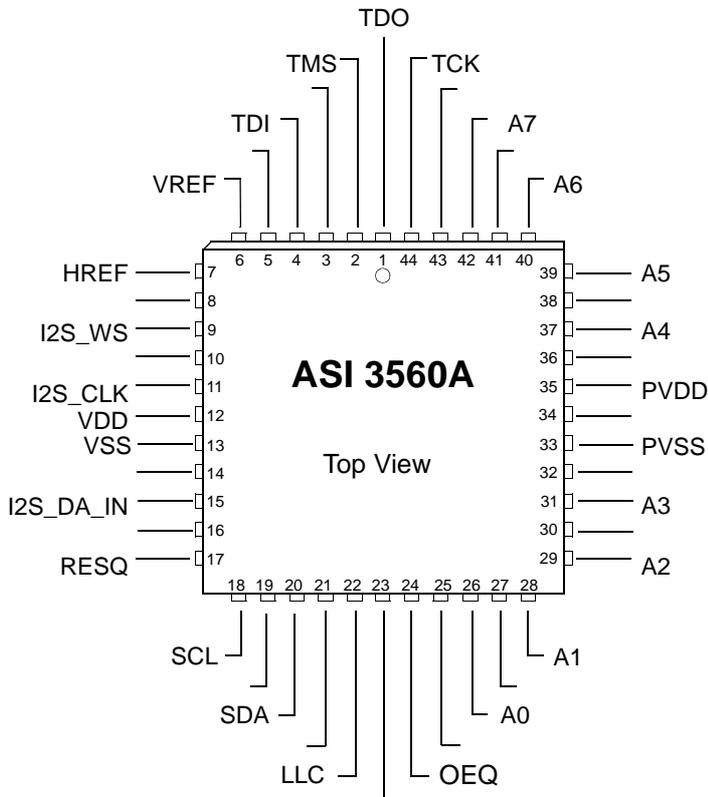
4.4. Pin Configuration
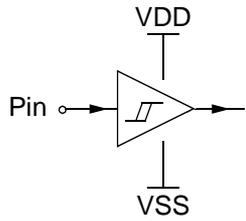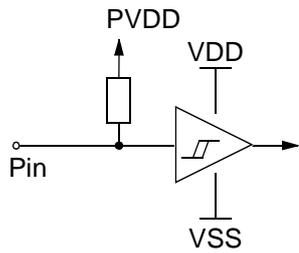

Fig. 4–2: 44-pin PLCC package

4.5. Pin Circuits

Fig. 4–3: TCK, HREF, VREF, RESQ, LLC, I^{2}S_xxx

Fig. 4–6: OEQ

The characteristics of the Schmitt-Triggers are dependent on the supply of VDD/VSS

Fig. 4–4: TMS, TDI

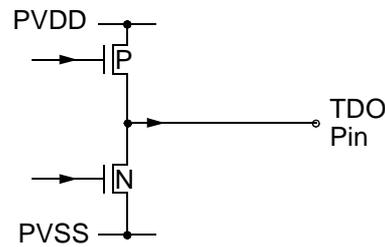**Fig. 4–7:** Output port TDO
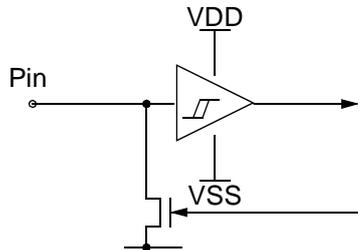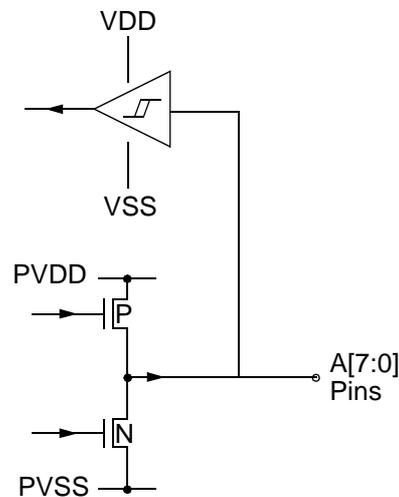

Fig. 4–5: I^{2}C Interface SDA, SCL

Fig. 4–8: Bidirectional video port A[7:0]

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Temperature		0	65	°C
T_S	Storage Temperature		-40	125	°C
T_J	Junction Temperature		0	125	°C
V_{SUB}	Supply Voltage, all Supply Inputs		-0.3	6	V
$P_{TOT\,MAX}$	Power Dissipation due to package characteristics	VDD, PVDD,		1089	mW
	Input Voltage of TMS, TDI		PVSS - 0.5	PVDD + 0.5[1]	V
	Input Voltage	TCK	PVSS - 0.5	6	V
	Input Voltage	SDA, SCL	VSS - 0.5	6	V
	Signal Swing	A[7:0], TDO	PVSS - 0.5	PVDD + 0.5[1]	V
	Signal Swing	OEQ	VSS - 0.5	VDD + 0.5 [1]	
	Maximum D | VSS - PVSS |			0	V

[1] External voltage exceeding PVDD+0.5 V should not be applied to these pins even when they are tri-stated.

Stresses beyond those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions/Characteristics" of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	-	0	-	65	°C
V_{SUPD}	Digital Supply Voltage	VDD	4.75	5.0	5.25	V
V_{SUPP}	Pad Supply Voltage	PVDD	3.15		3.6[1]	V
f_{XTAL}	Clock Frequency	LLC		27.0		MHz

[1] could also be connected to the 5 V supply net; but for best performance, it is recommended to connect it to 3.3 V supply.

4.6.3. Recommended I²S Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
t_{I2SCL_low}	I²S Clock low time	I²S_CLK	120	490		ns
t_{I2SCL_high}	I²S Clock high time	I²S_CLK	120	490		ns
t_{I2SWS_SU}	I²S word strobe setup time	I²S_WS	40			ns
t_{I2SWS_H}	I²S word strobe hold time	I²S_WS	40			ns
t_{I2SDA_SU}	I²S data in setup time	I²S_DA_IN	40			ns
t_{I2SDA_H}	I²S data in hold time	I²S_DA_IN	40			ns

4.6.4. Recommended I²C Conditions

(Timing diagram see Fig. 4–11 on page 33)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{IMIL}	I²C-BUS Input Low Voltage	SCL, SDA			0.3	VDD
V_{IMIH}	I²C-BUS Input High Voltage		0.6			VDD
f_{SCL}	I²C-BUS Frequency	SCL			400	kHz
t_{I2C1}	I²C START Condition Setup Time	SCL, SDA	1250			ns
t_{I2C2}	I²C STOP Condition Setup Time		1250			ns
t_{I2C3}	I²C-Clock Low Pulse Time	SCL	1250			ns
t_{I2C4}	I²C-Clock High Pulse Time		1250			ns
t_{I2C5}	I²C-Data Setup Time Before Rising Edge of Clock	SCL, SDA	250			ns
t_{I2C6}	I²C-Data Hold Time after Falling Edge of Clock		250			ns

4.6.5. Recommended Digital Inputs Levels of HREF, VREF, A[7:0], LLC, I²S_xxx, RESQ, TCK, TMS, TDI

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{IL}	Input Voltage LOW	HREF, VREF, A[7:0], LLC, I²S_xxx, RESQ, TCK, TMS, TDI	-0.5	0	0.8	V
V_{IH}	Input Voltage HIGH	HREF, VREF, LLC, I²S_xxx, RESQ, TCK	2.0	5	6	V
V_{IH}	Input Voltage HIGH	TDI, TMS, A[7:0]	2.0	PVDD	PVDD + 0.3	V

4.7. Characteristics

at T_A = 0 to 65 °C, $V_{SUPD/A}$ = 4.75 to 5.25 V, V_{SUPP} = 3.15 to 3.5 V, f = 27.0 MHz for min./max. values
at T_C = 60 °C, $V_{SUPD/A}$ = 5 V, V_{SUPP} = 3.3 V, f = 27.0 MHz for typical values

4.7.1. Current Consumption

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
I_{VSUPD}	Current Consumption	VDD		t.b.d.		mA
I_{VSUPP}	Current Consumption	PVDD	application dependent			mA
			-		45@3.3V 75@5V	
P_{TOT}	Total Power Dissipation, normal operation condition	VDD, PVDD		t.b.d.		W
P_{TOT}	Total Power Dissipation low power mode	VDD, PVDD		t.b.d.		W

4.7.2. Characteristics, Reset

(Timing diagram see Fig. 4–10 on page 33)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{startup}$	RESQ inactive to active LLC		3.2		us	Reset and LLC from video decoder (e.g. VPX32xx)

4.7.3. Characteristics, Control Bus Interface

(Timing diagram see Fig. 4–11 on page 33)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IMOL}	Output Low Voltage	SDA	- -	-	0.4 0.6	V V	I_I = 3 mA I_I = 6 mA
t_{IMOL1}	I²C-Data Output Hold Time after Falling Edge of Clock SCL	SDA	15			ns	
t_{IMOL2}	I²C-Data Output Setup Time before Rising Edge of Clock SCL	SDA	100			ns	f_{SCL} = 1 MHz, VDD = 5 V
t_F	Signal Fall Time	SDA	-	-	300	ns	C_L = 400 pF, R_{PU} = 4,7 k
f_{SCL}	Clock Frequency[1]	SCL	0	-	400	kHz	low power mode
[1] The maximum clock frequency of the I2C interface is limited to 400 kHz while the IC is working in the low power mode.							

4.7.4. Characteristics, JTAG Interface (Test Access Port TAP)

(Timing diagram see Fig. 4–13 on page 34)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$F_{CYCL-TAP}$	JTAG Cycle Time	100			ns	
F_{H-TAP}	TCK High Time	50			ns	
F_{L-TAP}	TCK Low Time	50			ns	
$V_{RES-TAP}$	Minimum supply voltage to initiate an internal reset of the JTAG-TAP generated by a voltage supply supervision circuit	3.5			V	VDD pin
Test Access Port (TAP), see timing diagram Fig. 4–13 on page 34						
t_{S-TAP}	TMS, TDI Setup Time	10			ns	
t_{H-TAP}	TMS, TDI Hold Time	10			ns	
t_{D-TAP}	TCK to TDO Propagation Delay for Valid Data			50	ns	
t_{ON-TAP}	TDO Turn-on Delay			45	ns	
$t_{OFF-TAP}$	TDO Turn-off Delay			45	ns	
Boundary-Scan Test, Characteristics of all IO pins which are connected to the boundary scan register chain						
t_{S-PINS}	Input Signals Setup Time at CAPTURE-DR	10			ns	
t_{H-PINS}	Input Signals Hold Time at CAPTURE-DR	10			ns	
t_{D-PINS}	TCK to Output Signals, Delay for Valid Data			50	ns	
$t_{ON-PINS}$	Turn-on Delay			20	ns	
$t_{OFF-PINS}$	Turn-off Delay			20	ns	

4.7.5. Characteristics, Digital Inputs/Outputs

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Digital Input Pins TMS, TDI, TCK, HREF, VREF, LLC, A[7:0], I²S_CLK, I²S_WS, I²S_DA_IN, $\overline{RES}$,SCL, SDA						
C_{IN}	Input Capacitance		5	8	pF	
I_I	Input Leakage Current Input Pins TCK, HREF, VREF, LLC, A[7:0], I²S_CLK, I²S_WS, I²S_DA_IN, $\overline{RES}$, SCL, SDA			-1 +1	mA	$V_I = V_{SS}$ $V_I \leq V_{DD}$
I_I	Input Leakage Current Input Pins with Pull-ups: TDI and TMS		-25	-55 +1	mA	$V_I = V_{SS}$ $V_I \leq V_{DD}$
Digital Output pin OEQ						
C_O	High-Impedance Output Capacitance					
V_{OL}	Output Voltage LOW					
V_{OH}	Output Voltage HIGH					
I_O	Output Leakage Current					
Digital Output pins A[7:0], TDO						
C_O	High-Impedance Output Capacitance		5	8	pF	
V_{OL}	Output Voltage LOW			0.4 0.6	V V	$I_I = 3$ mA $I_I = 6$ mA
V_{OH}	Output Voltage HIGH	2.4	-	PVDD	V	
I_O	Output Leakage Current			-1 +1	mA mA	while IC remains in low power mode $V_I = V_{SS}$ $V_I \leq V_{DD}$
A special VDD, VSS supply is used only to support the digital output pins. This means, inherently, that in case of tri-state conditions, external sources should not drive these signals above the voltage PVDD which supplies the output pins.						

4.7.6. Clock Signal LLC

The following timing specifications refer to Fig. 4–10 on page 33.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
LLC:						
t_{LLC}	Cycle Time		37		ns	
F_H	Duty Cycle $F_H / (F_L + F_H)$		50		%	

4.7.7. Digital Video Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Data and Control Pins (LLC to A[7:0], HREF, VREF: The following timing specifications refer to the timing diagrams of section 4.8.6. on page 35						
t_{OH}	Output Hold Time	8			ns	
t_{PDI}	Input Propagation Delay			23	ns	
t_{PDO}	Output Propagation Delay			21	ns	
Output Enable by OEQ (see Fig. 4–12)						
t_{ON}	Output Enable OEQ			15	ns	
t_{OFF}	Output Disable OEQ			15	ns	

4.7.8. Characteristics, TTL Output Driver

4.7.8.1. TTL Output Driver Type A

Output Pins A[7:0], TDO

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
T_A		65	RT	0	°C	Ambient Temperature
VDD		4.75	5.0	5.25	V	Supply
PVDD		3.0	3.3	3.6	V	Pad Supply
t_{RA}	Rise Time	2	5	10	ns	$C_I = 30\,pF$, strength = 4
t_{FA}	Fall Time	2	5	10	ns	$C_I = 30\,pF$, strength = 4
$I_{OH}(0)$	Output High Current (strength = 0)	-1.37	-2.25	-2.87	mA	$V_{OH} = 0.6\,V$
$I_{OL}(0)$	Output Low Current (strength = 0)	1.75	3.5	4.5	mA	$V_{OH} = 2.4\,V$
$I_{OH}(7)$	Output High Current (strength = 7)	-11	-18	-25	mA	$V_{OH} = 0.6\,V$
$I_{OL}(7)$	Output Low Current (strength = 7)	14	28	36	mA	$V_{OH} = 2.4\,V$
$I_{OH}(7)$	Output High Current (strength = 7) **ATE Condition EM**	-14.2	-17.8	-23.5	mA	$V_{OH} = 0.6\,V$, T = RT VDD= 5.0 V; PVDD= 3.3 V
$I_{OL}(7)$	Output Low Current (strength = 7) **ATE Condition EM**	21.9	27.4	32.9	mA	$V_{OH} = 0.6\,V$, T = RT VDD= 5.0 V; PVDD= 3.3 V
$I_{OH}(7)$	Output High Current (strength = 7) **ATE Condition Probe**	-11.5	-14.4	-19	mA	$V_{OH} = 0.6\,V$, T = 90 °C VDD= 5.0 V; PVDD= 3.3 V
$I_{OL}(7)$	Output Low Current (strength = 7) **ATE Condition Probe**	17.7	22.2	26.6	mA	$V_{OH} = 0.6\,V$, T = 90 °C VDD= 5.0 V; PVDD= 3.3 V

4.7.8.2. TTL Output Driver OEQ

Output Pins OEQ

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
T_A		65	RT	0	°C	Ambient Temperature
VDD		4.75	5.0	5.25	V	Supply
t_{RA}	Rise Time				ns	C_I = 30 pF, strength = 4
t_{FA}	Fall Time				ns	C_I = 30 pF, strength = 4
$I_{OH}(0)$	Output High Current (strength = 0)				mA	V_{OH} = 0.6 V
$I_{OL}(0)$	Output Low Current (strength = 0)				mA	V_{OH} = 4.0 V
$I_{OH}(7)$	Output High Current (strength = 7)				mA	V_{OH} = 0.6 V
$I_{OL}(7)$	Output Low Current (strength = 7)				mA	V_{OH} = 4.0 V
$I_{OH}(7)$	Output High Current (strength = 7) **ATE Condition EM**				mA	V_{OH} = 0.6 V, T = RT VDD= 5.0 V;
$I_{OL}(7)$	Output Low Current (strength = 7) **ATE Condition EM**				mA	V_{OH} = 0.6 V, T = RT VDD= 5.0 V;
$I_{OH}(7)$	Output High Current (strength = 7) **ATE Condition Probe**				mA	V_{OH} = 0.6 V, T = 90 °C VDD= 5.0 V;
$I_{OL}(7)$	Output Low Current (strength = 7) **ATE Condition Probe**				mA	V_{OH} = 0.6 V, T = 90 °C VDD= 5.0 V;

The driving capability/strength is controlled by the state of the I^2C register 84_{hex} [13:11].

A special PVDD, PVSS supply is used only to support the digital output pins. This means, inherently, that in case of tri-state conditions, external sources should not drive these signals above the voltage PVDD which supplies the output pins.

All timing specifications are based on the following assumptions:

– the load capacitance is $C_A = 30\,pF$,

– no static currents are assumed,

– the driving capability of the pads is STR = 4, which means that 5 of 8 output drivers are enabled.

The typical case specification relates to:

– the ambient temperature is $T_A = 25\,°C$, which relates to a junction temperature of $T_J = 70\,°C$;

– the power supply of the pad circuits is PVDD = 3.3 V, and the power supply of the digital parts is VDD = 5.0 V.

The best case specification relates to:

– a junction temperature of $T_J = 0\,°C$,

– the power supply of the pad circuits is PVDD = 3.6 V, and the power supply of the digital parts is VDD = 5.25 V.

The worst case specification relates to:

– a junction temperature of $T_J = 125\,°C$,

– the power supply of the pad circuits is PVDD = 3.0 V, and the power supply of the digital parts is VDD = 4.75 V.

Rise times are specified as a transition between 0.6 V to 2.4 V. Fall times are defined as a transition between 2.4 V to 0.6 V.

strength = 7

strength >= 6

strength >= 5

strength >= 4

strength >= 3

strength >= 2

strength >= 1
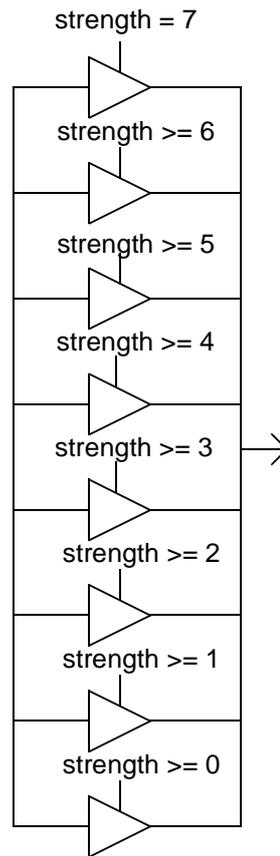
strength >= 0

Fig. 4–9: Block diagram of the output stages

Note: The drivers of the output pads are implemented as a parallel connection of 8 tri-state buffers of the same size. The buffers are enabled depending on the desired driver strength. This opportunity offers the advantage of adapting the driver strength to on-chip and off-chip constraints, e.g. to minimize the noise resulting from steep signal transitions.

4.8. Timing Diagrams

4.8.1. Power-Up Sequence

The reset may go high before LLC starts. The IC remains in low-power mode after reset and must be started by an I^2C wakeup telegram.
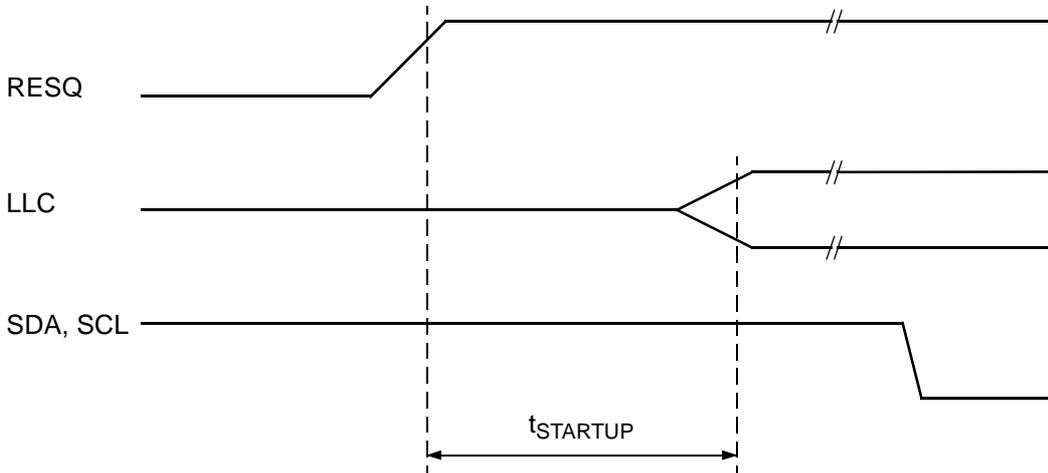
Fig. 4–10: Power-up sequence

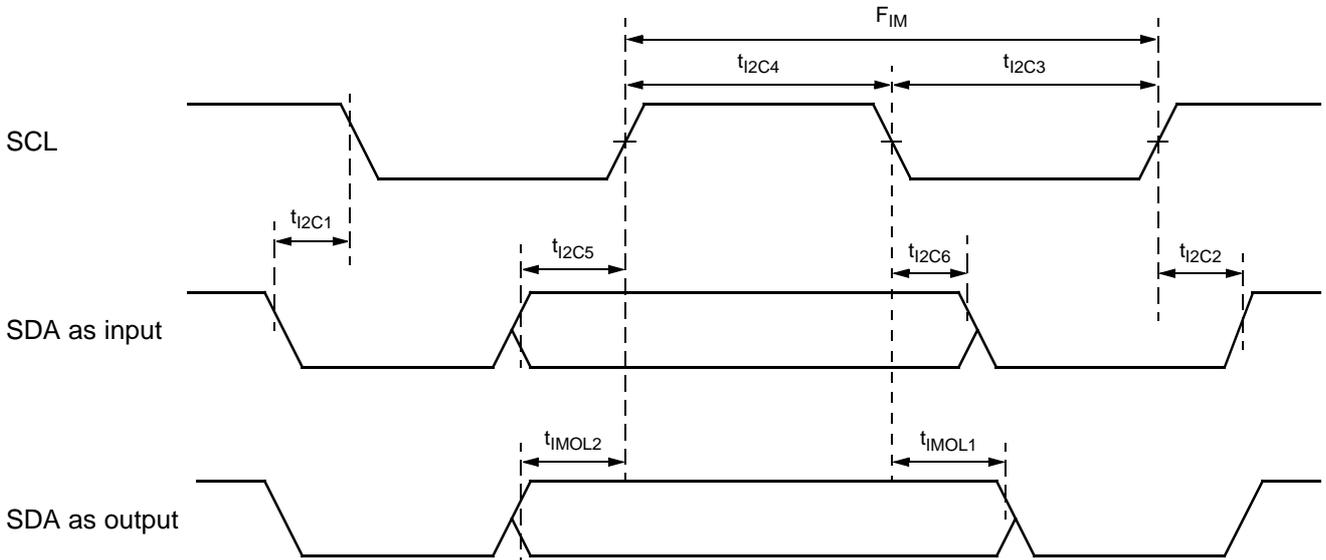#### 4.8.2. Control Bus Timing Diagram

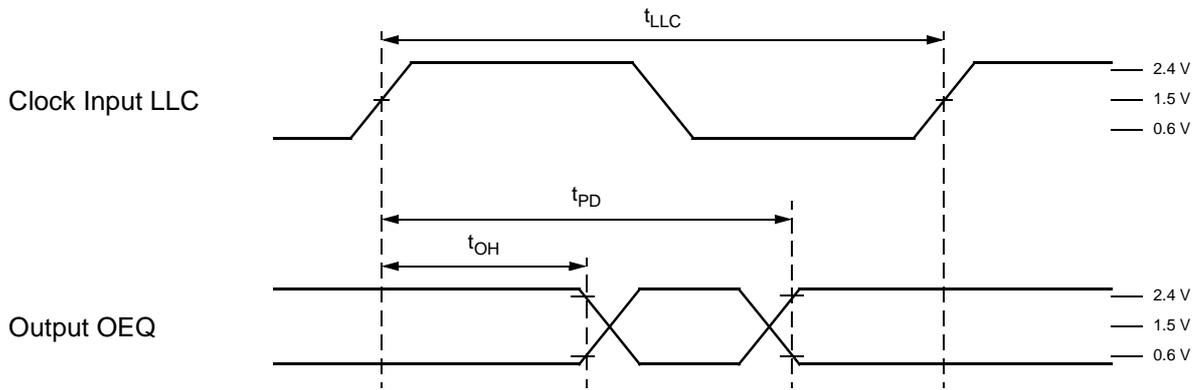**Fig. 4–11:** I^2C bus timing diagram

4.8.3. Output Enable by Pin OEQ

Fig. 4–12: Expected Drive Control by OEQ output
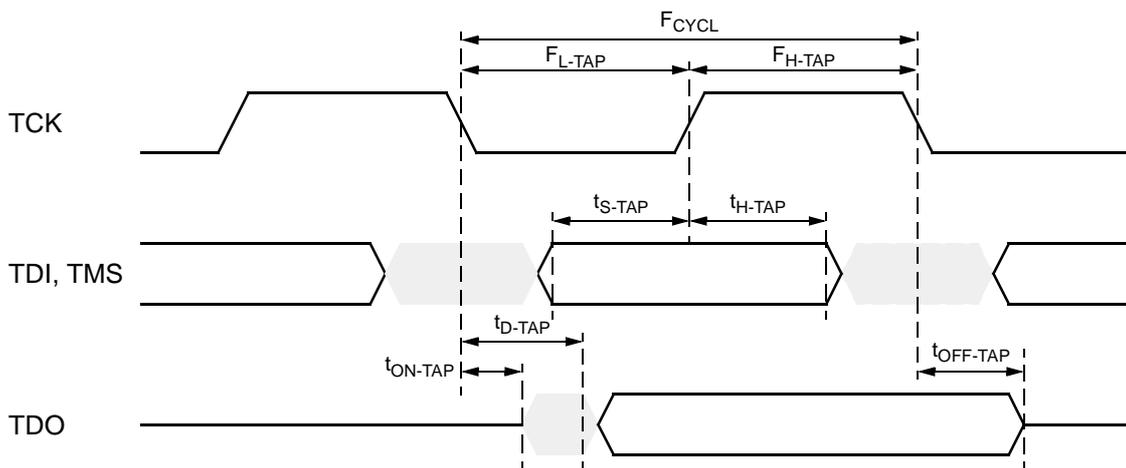
4.8.4. Timing of the Test Access Port TAP

Fig. 4–13: Timing of Test Access Port TAP

4.8.5. IO-Timing of all Pins connected to the Boundary-Scan-Register-Chain
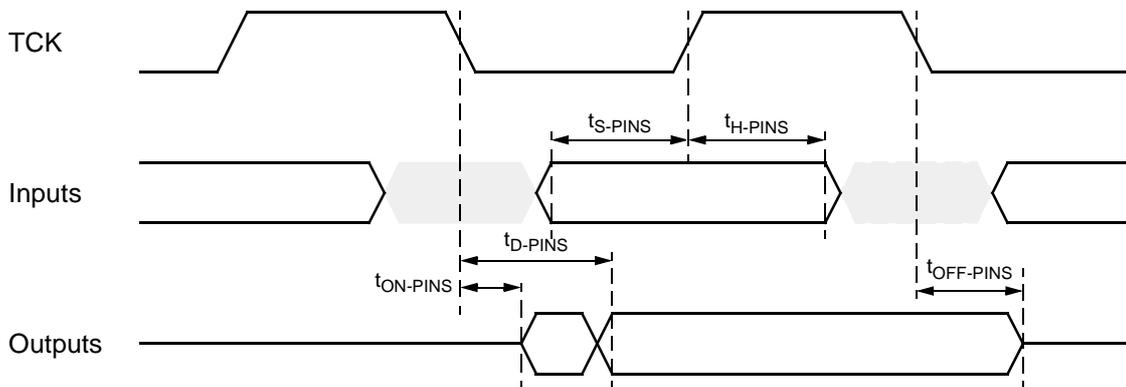
Fig. 4–14: Timing with respect to input and output signals

4.8.6. Timing Diagram of the Digital Video Interface
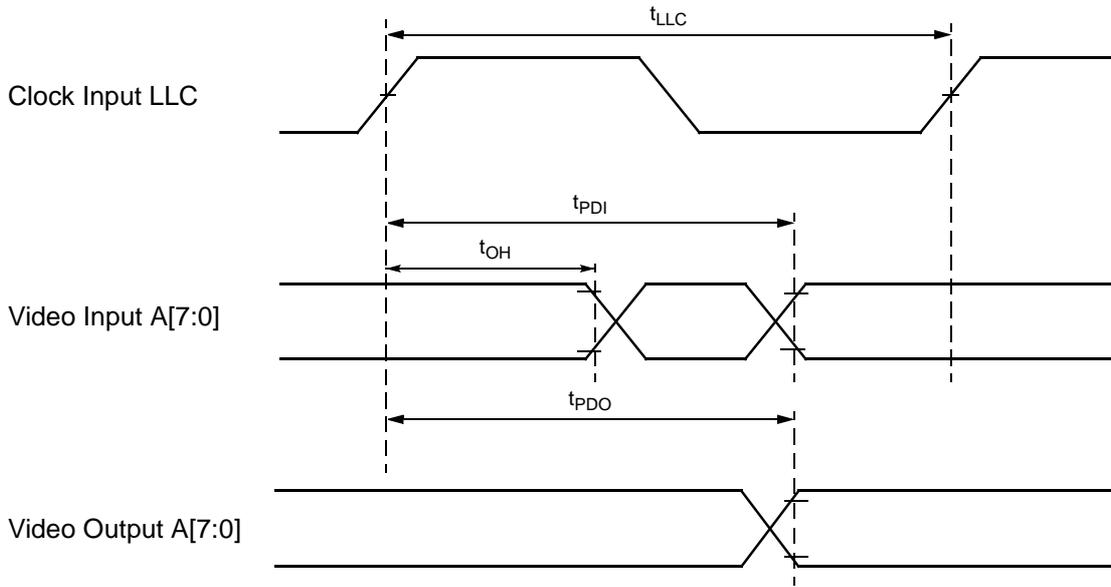
Fig. 4–15: Video Output Interface: detailed timing

4.8.7. Timing Diagram of the I^{2}S Interface
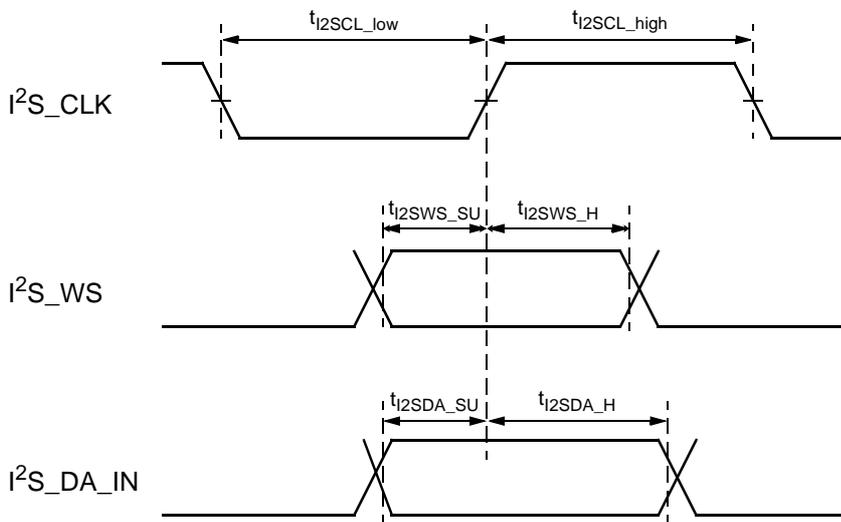
Fig. 4–16: Detailed timing of the I^{2}S interface

5. Data Sheet History

1. Preliminary data sheet: "ASI 3560A Audio Stream Interface, Jan. 23, 1998, 6251-458-1PD. First release of the preliminary data sheet.