Application report for the UMA1014T frequency synthesizer

SCO/AN91004

1. INTRODUCTION

This application note is intended as a guide to designing a phase locked loop based on the Philips UMA1014T frequency synthesizer integrated circuit. The UMA1014T is a low power single chip solution to frequency synthesis in the range 100 MHz to 1100 MHz and is primarily intended for use in analogue cellular radio applications.

The device comprises of the following functional blocks:

- RF dual-modulus prescaler.
- RF programmable divider.
- Reference oscillator.
- Reference programmable divider.
- Digital phase comparator.
- In-lock detection circuitry.
- I^2C serial programming interface.

In addition, the device features a power down mode for battery conservation and a XTAL/8 output for use with the Philips cellular radio chipset. The only major external component required is a voltage controlled oscillator (VCO).

This application report presents a design for a frequency synthesizer based on the UMA1014T suitable for the local oscillator for analogue cellular radio applications in the 900 MHz band. A PCB layout is suggested. For detailed device specifications of the UMA1014T refer to the data sheet (Reference 1).

2. FUNCTIONAL DESCRIPTION OF THE UMA1014T

The main functions are illustrated in a Phase Lock Loop (PLL) block diagram (Fig 1). A temperature controlled crystal oscillator (TCXO) provides a reference frequency to the PLL. A phase comparator uses a charge pump to send correction current pulses to a low pass filter. The filter integrates the pulses giving a voltage which controls a VCO. VCO and TCXO o/ps are divided down to a common comparison frequency to control the phase comparator. When the VCO o/p is on frequency, the current pulses need only be large enough to cancel leakage currents, thus maintaining the required voltage on the VCO.

2.1 Main Divider Chain

The UMA1014T contains a fully programmable main divider chain with an on-chip RF prescaler. The range of the main divider is from 2,048 to 262,143, thus permitting all useful phase detector comparison frequencies over the full range of input frequencies.

2.2 Reference Divider Chain

Since current analogue systems have only a few different channel spacings, and in any system there is a restricted choice of reference crystal frequencies, the UMA1014T implements a reference divider with limited programmability. A total of 16 different division ratios can be selected which enables all the required phase detector comparison frequencies to be generated. These ratios are 128, 160, 192, 240, 256, 320, 384, 480, 512, 640, 768, 960, 1024, 1280, 1536 and 1920.

In addition, there is one eighth of the crystal frequency available on an output for use with the Philips cellular radio chipset. This chipset uses a 1.2 MHz clock for the analogue and digital baseband circuits which is provided by the frequency synthesizer; the synthesizer thus requires the use of a 9.6 MHz crystal in this application.

2.3 Phase Detector

There are three requirements for the phase detector; firstly it should cover the full 360 degree phase range, secondly it should have good noise performance, and thirdly it should have good comparison frequency suppression. In order to meet these requirements, the use of a high gain digital phase comparator is beneficial. The comparator covers the complete phase range while introducing little noise owing to the high proportion of time that is spent in a high impedance state. Good reference rejection is achieved due to low leakage currents.

2 .3 .1 Digital Phase Comparator

The Digital Phase Comparator (PCD) has three states, sinking current, sourcing current and a high impedance tristate. The design is based on D type flip-flops and responds to the full 360 degree range of phase inputs. The D type flip-flops control two current sources arranged in a push pull configuration. PCD delivers a constant current while the main and reference dividers are out of phase, either sinking or sourcing (Fig 2). The current IPCD is programmed via the I^2C interface to be either 1 mA or 0.5 mA. The phase comparator gain is hence:

$$\text{PCD gain} = \frac{\text{IPCD}}{2 \times \pi} \text{ A / rad} \qquad (1.)$$

The phase comparator circuit incorporates a delay which eliminates a dead band that would otherwise be present in digital phase comparators. Dead bands are due to the finite time the current sources take to switch on. The design of the UMA1014T takes this into account by introducing the delay into the D type reset line. This gives the current sources enough time to respond. Both current sources are switched on for the duration of the delay thus cancelling each other at PCD.

3. INTERFACING TO THE UMA1014T

The UMA1014T provides two way communication to a controller, power down facility, programmable o/p ports, oscillator circuitry and PLL control. The UMA1014T is designed to have the minimum of external components to enable low cost, compact and reliable circuits.

3.1 Programming the UMA1014T

The UMA1014T is programmed via the Philips Standard I^2C bus. To program information into the device registers, it is necessary to transmit first the device address, then the sub-address, and finally the data bytes for the register(s) (Reference 2). To read the status register, it is only necessary to transmit the address before reading back the value of the status register. When writing to the UMA1014T, the sub-address allows writing to any single register, or a burst mode where all registers can be written in one I^2C transfer. The formats are thus:

Write to one register:
START - address - sub-address - data - STOP
- contains register number to be accessed
- R/WN (read/write not) bit set to 0 (write)

Write to several registers:
START - address - sub-address - data 1 - ... - data n - STOP
- contains first register number to be accessed in the sequence and auto-increment enabled
- R/WN bit set to 0 (write)

Read from status register:
START - address - status - STOP
- R/WN bit set to 1 (read)

The address byte, in addition to containing the R/WN bit as shown above, has one bit that reflects the inverse of the SAA pin logic level. This allows the addressing of up to two synthesizer circuits on the same I^2C bus.

The format for the address bus is as follows:

1 1 0 0 0 1 SAA R/WN
- 0 (write, 1 (read)
- opposite logic level to that of SAA pin
- MSB of device address, transmitted first after START condition

The sub-address has the following format: (X means not used)

X X X DI AVI X SB1 SB0
- register pointer
- auto-increment – 0 (disable), 1 (enable)
- SYA interrupt – 1(disable), 0 (enable)

Data is formatted as a series of registers as follows:

Reg	SB 1/0	Bit Allocation								Preset
		7	6	5	4	3	2	1	0	
A	00	PD	0	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10101001
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

Register map bit polarities:

	0	1
PD	Normal operation	Power down
IPCD	Current in PCD = 0.5mA	PCD = 1mA
RD3..0	Reference divider ratio MSB = RD3	
PHI	Passive loop (no inversion)	Active loop (Phase inversion)
VCOA	Set Pin 7 low	Set Pin 7 high
VCOB	Set Pin 13 low	Set Pin 13 high
MD17..0	Main divider ratio MSB = MD17	

RD3..RD0 reference divider programming:

RD3	RD2	RD1	RD0	Reference Division Ratio
0	0	0	0	128
0	0	0	1	160
0	0	1	0	192
0	0	1	1	240
0	1	0	0	256
0	1	0	1	320
0	1	1	0	384
0	1	1	1	480
1	0	0	0	512
1	0	0	1	640
1	0	1	0	768
1	0	1	1	960
1	1	0	0	1024
1	1	0	1	1280
1	1	1	0	1536
1	1	1	1	1920

MD17..MD0 main divider value 2048 to 262,143 (hex $800 to $3ffff).

3.2 Hardware Control Inputs and Outputs

There are a number of status and control signals generated by the UMA1014T and also a hardware control input.

3.2.1 HPD Input

This input is used to disable the divider chains in order to save power when the synthesizer is not required to be operational. The power down state can be activated either by taking this pin low or by setting the power down bit in the I^2C register to a '1'. The input has an internal pull-up resistor so that normal operation will be obtained if the pin is left open circuit.

The power down state does not have any effect on the I^2C circuitry, so that the device may still be addressed, and new information programmed into the registers even in the power down mode.

3.2.2 FX8 Output

This is an open collector output of one eighth of the crystal or TCXO input frequency. It is required for use with the Philips cellular radio chipset for AMPS and TACS systems; in this application the synthesizer should be used with a 9.6 MHz TCXO. The recommended pull-up load is 27 kΩ.

3.2.3 SYA (Synthesizer Alarm) Output

This is an open collector output which is normally held high by an external 27 kΩ load. Under error conditions, the synthesizer latches SYA low. The error conditions that set SYA low are a power dip or an out-of-lock condition. A power dip occurs when V_{CC} supply falls below about 3.5 V. SYA is reset again by reading the status register, which contains the relevant alarm information. The SYA output can also be enabled and disabled via I^2C as required.

The typical use of SYA would be to interrupt a microcontroller to warn of the error condition. As the output is open collector, it is possible to connect more than one device together directly; in this case the microcontroller would poll the relevant devices to locate the source of the error condition.

3.2.4 VCO0 and VCO1 Outputs

These are open collector outputs and are intended for enabling the power supply to VCOs or buffer stages so that these parts of the set can be powered down when not required to be operational. The outputs are controlled via I^2C. In addition, the VCO0 output is forced low during an out-of-lock condition; this output could, therefore, be used to disable the transmitter when this condition occurs to prevent causing interference. In this case, there may well be other parts of the circuitry also controlling the transmitter in the same way; as the VCO0 and VCO1 lines are open collector, they may be directly connected to other such controlling signals.

The VCO1 output is not affected by the hardware power down input or power down via I^2C. The VCO0 output will of course be forced low due to the out-of-lock condition resulting from a power down.

3.3 Crystal Oscillator

For analogue cellular radio applications, the UMA1014T will almost certainly be used with an external oscillator in order to provide the stability necessary to ensure operation within the specification. However, in case some other applications do not require such accuracy, provision has been made to form a crystal oscillator using the OSC_{IN} and OSC_{OUT} inputs (Pins 1 and 2, respectively). The oscillator circuit should be of the Colpitts type and requires the addition of four capacitors to function. This is shown in Fig 3, with capacitor values suitable for operation at 9.6 MHz.

The internal biasing provides possible operation over the range 3 MHz to 16 MHz with the addition of a suitable crystal. It may be necessary to adjust the values of the capacitors slightly to guarantee oscillation under all conditions for frequencies significantly different at 9.6 MHz.

The crystal used in this circuit is parallel resonant, fundamental mode, with a load capacitance of 30 pF which is approximately the series combination of the three fixed capacitors in parallel with the trimmer capacitor.

3.4 External Oscillator

When using an external oscillator such as a TCXO module, the output from the oscillator should be connected directly to the OSC_{IN} pin (Pin 1). The OSC_{OUT} pin (Pin 2) should either be left open circuit, or could be used as a buffered version of the signal applied to OSC_{IN}.

3.5 RF Connection to Main Divider

The output from the VCO needs to be split between the synthesizer RF o/p and the UMA1014T main divider input. A matched splitter is used as shown in Fig 4. Ideally, the splitter should provide maximum isolation to the VCO to prevent pulling or modulation due to changes in the load impedance at the RF o/p and main divider input. The amount of isolation is limited by the required RF output power and the main divider input sensitivity. Emphasis is placed on the importance of providing sufficient isolation between the VCO and the main divider to keep spurious modulations at a minimum level.

3.6 Loop Filter Design

The correct design of the loop filter is of considerable importance to the optimum performance of the synthesizer. The filter should be designed so as to achieve the required compromise between noise performance and switching time. The actual circuit will, therefore, depend on the particular application. A procedure has been established to ensure quick and simple loop filter design. The method, based on first-order approximations, provides a working solution without a need for computer simulation and modelling.

Design Procedure

For typical applications a passive loop is used, thus removing the need for an operational amplifier. The following design is based on a second-order low-pass filter (Reference 3). Then, for applications requiring further reference breakthrough rejection, a third-order is incorporated. The third-order loop filter is used for circuits and measurements in this report.

Loop parameters are first chosen, these are:

- Radio frequency RF
- Comparison frequency CF
- Switching time St
- Minimum modulating frequency MF
- VCO gain rad/Volt Ko
- Phase comparator gain Amps/rad Kd
- Phase margin Φ

Determine the loop bandwidth Fn from

$$\frac{3}{\text{switching time}} = \text{fn} \quad (2.)$$

Determine main divider ratio from

$$N = \frac{RF}{CF} \quad (3.)$$

Determine angular velocity wn rads / s from $wn = 2 \times \pi \times Fn$

The loop filter circuit (Fig 5) has three time constants, these are:

$$T1 = C3 \cdot R2 \quad (4.)$$

$$T2 = R2 \cdot C1 \cdot C3 \; / \; (C3 + C4) \quad (5.)$$

$$T3 = C2 \cdot R1 \quad (6.)$$

The second-order loop is designed by omitting R1 and C2 (T3) and uses the equations below:

$$T2 = \frac{\frac{1}{\Phi} - \text{Tan } \Phi}{wn} \quad (7.)$$

$$T1 = \frac{1}{wn^2 \cdot T2} \quad (8.)$$

$$C3 + C1 = K \sqrt{\frac{1 + (wn \cdot T1)^2}{1 + (wn \cdot T2)^2}} \quad (9.)$$

where,

$$K = \frac{Kd \cdot Ko}{N \cdot wn^2} \quad (10.)$$

$$C1 = \frac{T2 \cdot (C3 + C1)}{T1} \quad (11.)$$

$$C3 = (C3 + C1) - C1 \quad (12.)$$

$$R2 = \frac{T1}{C3} \quad (13.)$$

Measuring the reference spurs and comparing with a particular specification establishes if a third-order is necessary.

If a further 'A' dB of breakthrough suppression is needed to meet specification, then T3 is included to make a third-order filter. Note 'A' should not be so large that T3 x 10 > T1. A good starting value for 'A' is 20 dB.

$$T3 = \sqrt{\left(\frac{10^{(A/20)} - 1}{(2 \cdot \pi \cdot Fc)^2}\right)} \quad (14.)$$

T2 determines the loop stability and remains the same as for 2nd-order loop.

A calculated value of closed loop bandwidth wnc is used. This is usually slightly less than wn so the switching time will be slightly longer than originally specified.

$$wnc = \frac{(T2 + T3)}{T2^2} \cdot \tan\,\Phi \cdot \sqrt{1 + \frac{4 \cdot T2^2}{(2 \cdot \tan\Phi \cdot (T2 + T3))^2}} - 1 \quad (15.)$$

$$T1 = \frac{1}{wnc^2 \cdot (T2 + T3)} \quad (16.)$$

$$C3 + C1 = K \sqrt{\frac{1 + (wnc \cdot T1)^2}{(1 - wnc^2 \cdot T2 \cdot T3)^2 + \frac{T3 + T2}{T1}}} \quad (17.)$$

where,

$$K = \frac{Ko \cdot Kd}{N \cdot wnc^2} \quad (18.)$$

$$C1 = \frac{(C3 + C1) \cdot T2}{T1} \quad (19.)$$

$$C2 = C(C3 + C1) - C1 \quad (20.)$$

$$C2 = \frac{C1}{16} \quad (21.)$$

$$R2 = \frac{T1}{C3} \quad (22.)$$

$$R1 = \frac{T3}{C2} \quad (23.)$$

For a successful filter it is important that C3 > > C1 and C1 > > C2.

3.6.1 Worked Example

As an example the design of the third-order loop filter for the UMA1014T under the following conditions is shown below. This design on the PCAL1143-I board suitable for ETACS transmit application. Switching time is set slightly shorter than expected to compensate for the reduction in the final loop bandwidth Fnc.

VCO frequency		=	888MHz
VCO gain	Ko	=	13MHz/V
Channel spacing		=	25kHz (with half channel offset)
Reference oscillator		=	9.6MHz
Switching time		=	12ms (for a requirement < 14ms)
Min mod frequency		=	300Hz
Phase margin (degrees)		=	45
Additional reference Rejection	A	=	20dB

In this example the phase comparator gain Kd chosen is 1 mA / cycle as opposed to 0.5 mA / cycle. In open environment a loop based on this is less susceptible to interference as capacitor values are higher. A comparison frequency of 12.5 kHz is chosen to allow for the half channel offset specified in ETACS.

The first-order loop bandwidth Fn:

$$\frac{3}{12 \cdot 10^3} = 250Hz \quad wn = 2 \cdot \pi \cdot Fn = 1570 rads/s \quad \text{Use (2.)}$$

The main divider ratio N:

$$\frac{888 \cdot 10^6}{12.5 \cdot 10^3} = 71,040 \quad \text{Use (3.)}$$

$$T2 = \frac{\frac{1}{\cos 45} - \tan 45}{1570} = 2.64 \cdot 10^{-4} \quad \text{Use (7.)}$$

$$T3 = \sqrt{\frac{10^{(20/20)} - 1}{(2 \cdot \pi \cdot 12,500)^2}} = 3.82 \cdot 10^{-5} \quad \text{Use (14.)}$$

$$wnc = \frac{4 \cdot (2.64 \cdot 10^{-4})^2}{(2.64 \cdot 10^{-4})^2} x \quad \text{Use (15.)}$$

$$\left(\sqrt{\frac{4 \cdot (2.64 \cdot 10^{-4})^2}{(2 \cdot \tan 45 \cdot (2.64 \cdot 10^{-4} + 3.82 \cdot 10^{-5}))^2}} - 1\right) = 1421$$

$$T1 \cdot \frac{1}{1421^2 \cdot (2.64 \cdot 10^{-4} + 3.82 \cdot 10^{-5})} = 1.64 \cdot 10^{-3} \quad \text{Use (16.)}$$

$$K = \frac{13 \cdot 10^6 \cdot 10^{-3}}{71,040 \cdot 1421^2} = 9.04 \cdot 10^{-8} \quad \text{Use (18.)}$$

$$C1 + C3 = \quad \text{Use (17.)}$$

$$k \sqrt{\frac{1 + (1421 \cdot 1.64 \cdot 10^{-3})^2}{(1–1421^2 \cdot 2.64 \cdot 10^{-4} \cdot 3.82^{-5})^2 + \frac{3.82 \cdot 10^{-5} + 2.64^{-4}}{1.64 \cdot 10^{-3}}}}$$

$$= 2.14 \cdot 10^{-7}$$

$$C1 = \frac{2.14 \cdot^{-7} \cdot 2.64 \cdot 10^{-4}}{1.64 \cdot 10^{-3}} = 3.45 \cdot 10^{-8} \quad \text{Use (19.)}$$

$$C3 = 2.14 \cdot 10^{-7} - 3.45 \cdot 10^{-8} = 1.8 \cdot 10^{-7} \quad \text{Use (20.)}$$

$$C2 = \frac{3.45 \cdot 10^{-8}}{16} = 2.15 \cdot 10^{-9} \quad \text{Use (21.)}$$

$$R2 = \frac{1.64 \cdot 10^{-3}}{1.8 \cdot 10^{-7}} = 9111 \quad \text{Use (22.)}$$

$$R1 = \frac{3.82 \cdot 10^{-5}}{2.15 \cdot 10^{-9}} = 17,767 \quad \text{Use (23.)}$$

Values chosen for filter components are:

C1 = 33nF	R1 = 18kΩ
C2 = 2.2nF	R2 = 10kΩ
C3 = 180nF	

3.7 PCB Layout Considerations

The circuit of the UMA1014T demonstration board (PCAL1143-1) is shown in Fig 6, with the layout shown in Fig 7. This PCB has a solid ground plane on one side (apart from isolated pads for non-grounded connections to leaded components). In addition, there are areas of ground plane on the surface mount side of the board to ensure satisfactory grounding of important components. There are a good number of plated-through holes connecting the

two layers of ground plane. Normal RF design practices should of course be taken into account when laying out the circuit.

There are a number of particular points that should be borne in mind when considering the circuit and layout.

- The non-surface mount side of the board (if a 2 sided board is used) should be virtually solid ground plane to give good RF performance.
- The 5 V digital supply (V_{CC}) should be well decoupled as close to the pin as possible, preferably with a large value capacitor (e.g., 47 μF) and in series with a small value resistor (e.g., 12 Ω) from the 5 V line.
- The 5 V charge pump supply (V_{CP}) should be decoupled separately from V_{CC} but in a similar manner. Routing the 5 V supply under the IC is to be avoided.
- Incorporating a ground plane on the surface mount side of the PCB underneath the synthesizer helps isolate digital noise from the charge pump parts. This ground plane should be well connected with vias to the full ground plane.

4. TYPICAL PERFORMANCE

This section describes the typical performance obtainable with the UMA1014T with the circuit shown in Fig 6 and parameters listed in 3.6.1. The relevant performance criteria for a synthesizer are usually:

Close-in phase noise (i.e., noise within the loop bandwidth).
Noise floor at an offset from the carrier.
Comparison breakthrough components.
Switching time.

It should be noted of course that these criteria can be traded off against each other to some extent to tailor the overall performance, and that the performance described here is only one compromise between the various criteria. In general, the choice of a low loop bandwidth will improve the comparison frequency breakthrough and will filter out more of the close-in phase noise, but will result in a longer switching time. The use of a higher order filter can improve comparison frequency breakthrough with little effect on the noise or switching time. The noise floor at offsets significantly higher than the loop bandwidth are determined completely by the VCO itself.

Plots of the close-in spectrum (span of 2 kHz) and also a span of 50 kHz are shown in Figs 8 and 9, respectively, for a carrier frequency of 888 MHz and a comparison frequency of 12.5 kHz. From Fig 8 we can see from the noise plateau that the loop bandwidth is around 270 Hz, and Fig 9 shows the spectrum analyzer noise floor at offsets greater than about 15 kHz from the carrier with the first and second comparison frequency breakthrough component being visible at 12.5 kHz and 25 kHz from the carrier, respectively.

Figure 10 shows switching waveforms for a frequency jump of 10 MHz. The top trace (labelled CH1) is the I^2C transfer to the UMA1014T; the second (CH2) is the VCO control line. The third trace (CH3) is the VCOA output showing the out-of-lock condition. The fourth trace (CH4) is the RF output of the VCO mixed down to 0 Hz with a signal generator at the destination frequency. The VCO output is coupled to the mixer via an amplifier with 17 dB gain followed by a 10 dB attenuator. This is to provide isolation to the VCO from the mixer.

The mixer output trace shows that the switching time is 13 ms, which is a little longer than the VCO control line trace appears to show. This is because observation of the VCO control line is not accurate due to the very high VCO gain (13 MHz / V).

From Fig 10, we can see that the VCO control line has a single overshoot during switching; this shows that the loop is properly damped, so the phase margin is correct.

To summarize the performance of the circuit in Fig 6:

loop bandwidth	270 Hz
close-in noise	- 55 dBc / Hz at 200 Hz from carrier
VCO noise floor	- 113 dBc / Hz at 25 kHz from carrier
residual fm	< 18 Hz rms, CCITT weighted
comparison frequency breakthrough	- 65 dBc at 12.5 kHz - 82 dBc at 25 kHz
typical switching time	< 13 ms for 10 MHz jump to within 1 kHz of the destination frequency

5. CONCLUSIONS

Information regarding the use of the UMA1014T in a frequency synthesizer application has been presented. A methodology for determining the loop filter components has been described since the switching and noise performance of the complete circuit depends on a good filter design. The layout of the PCAL1143-1 demonstration board has been shown as an example PCB layout.

6. REFERENCES

1. UMA1014T, Initial Specification Data Sheet, September 1990.
2. N. M. W. Oatley; Application Information for the UMA1010T/UMA1012T, Philips Components Application Report MC090001.
3. Ulriche, L. Rhode; Digital PLL Frequency Synthesizers Theory and Design. 28/3/91.

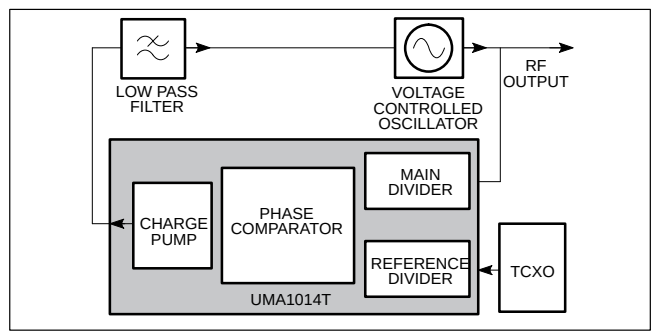


Figure 1. PLL Circuit Block Diagram

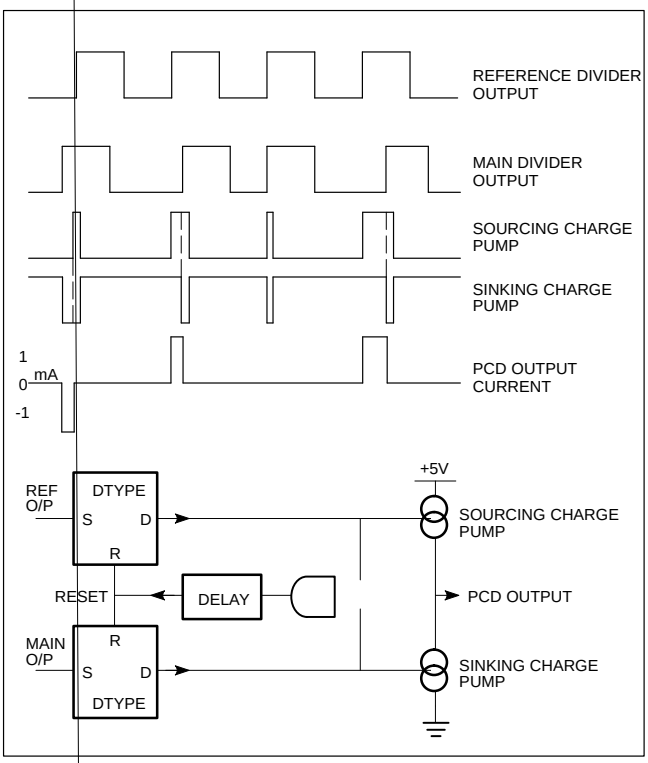


Figure 2. Digital Phase Comparator Operation

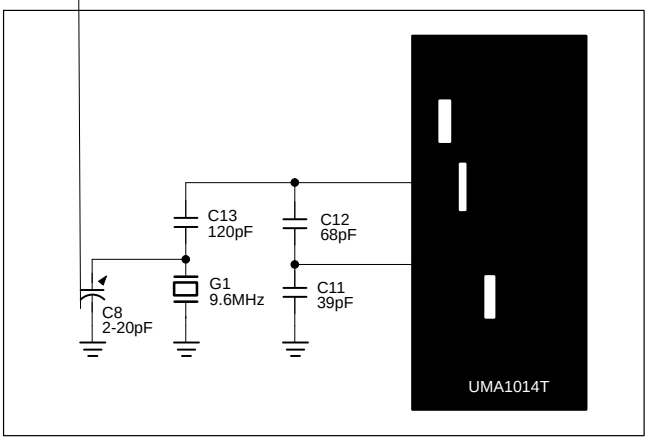


Figure 3. Crystal Oscillator Circuit Diagram

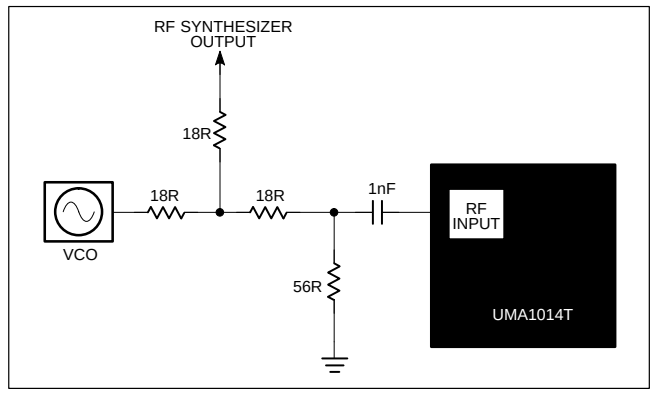


Figure 4. RF Power Splitter Circuit Diagram

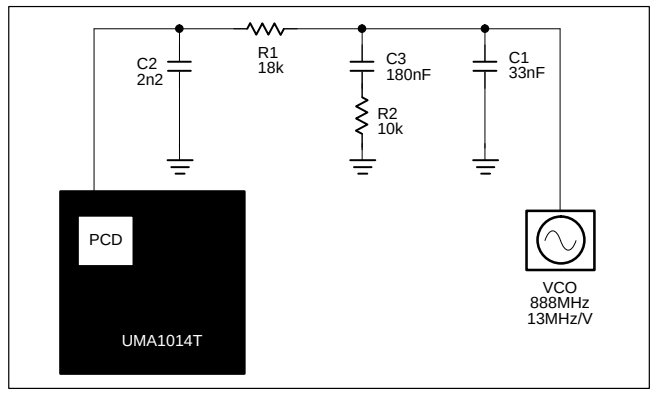


Figure 5. Loop Filter Circuit Diagram

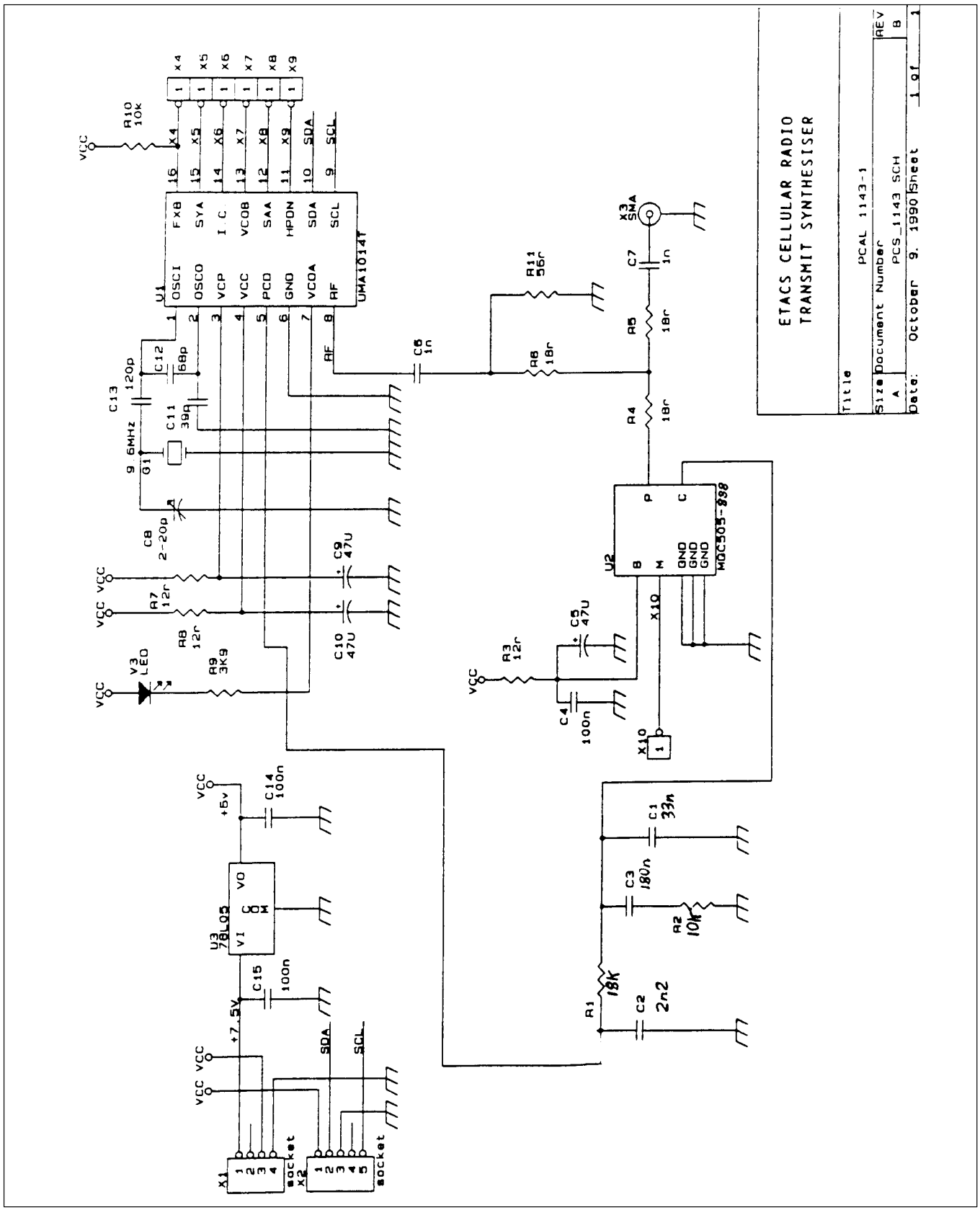
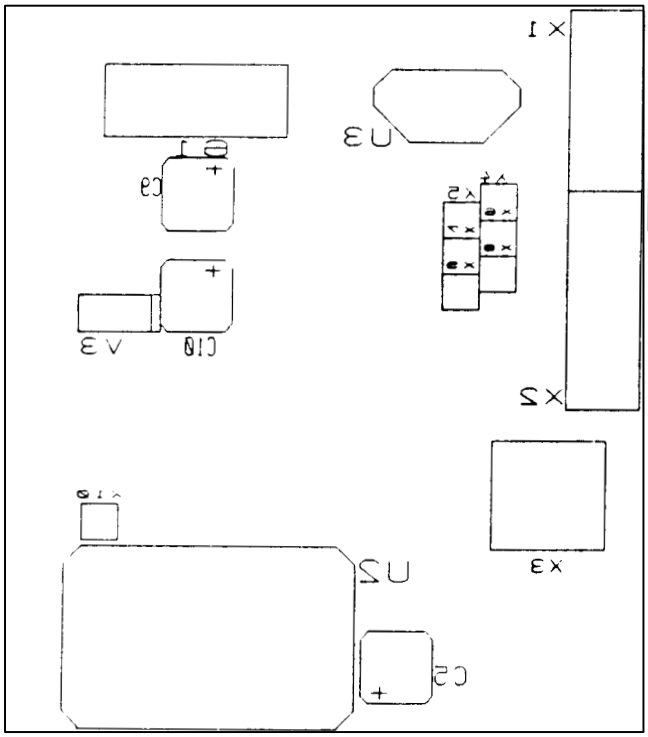
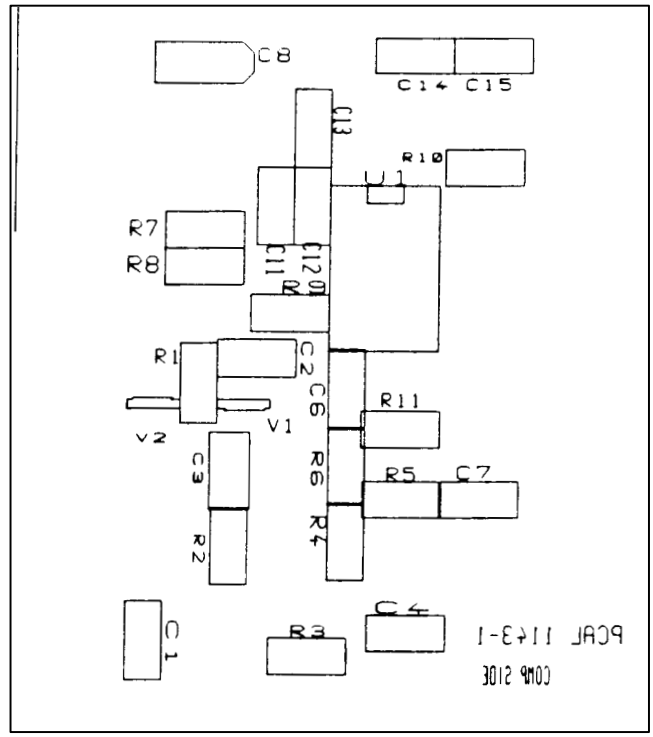


Figure 6. Frequency Synthesizer Circuit Using the UMA1014T





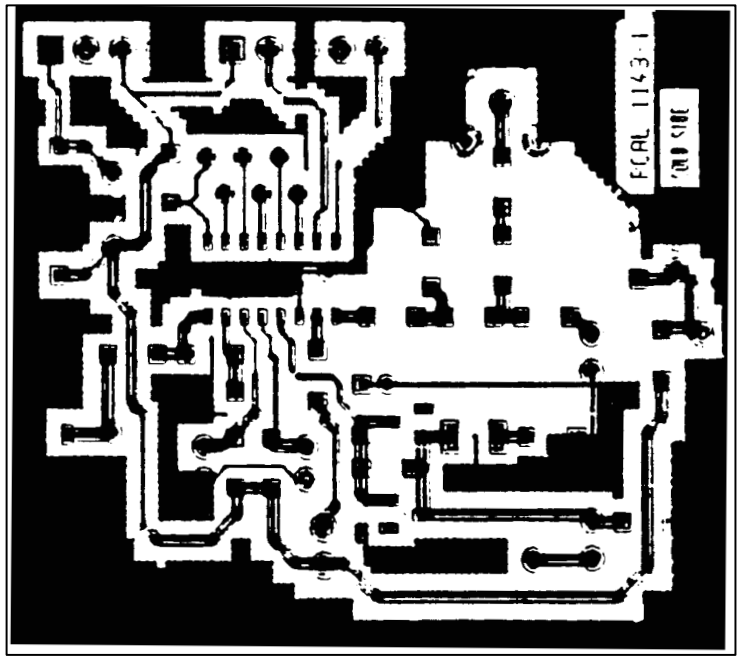


Figure 7. Board Layout for UMA1014T Frequency Synthesizer

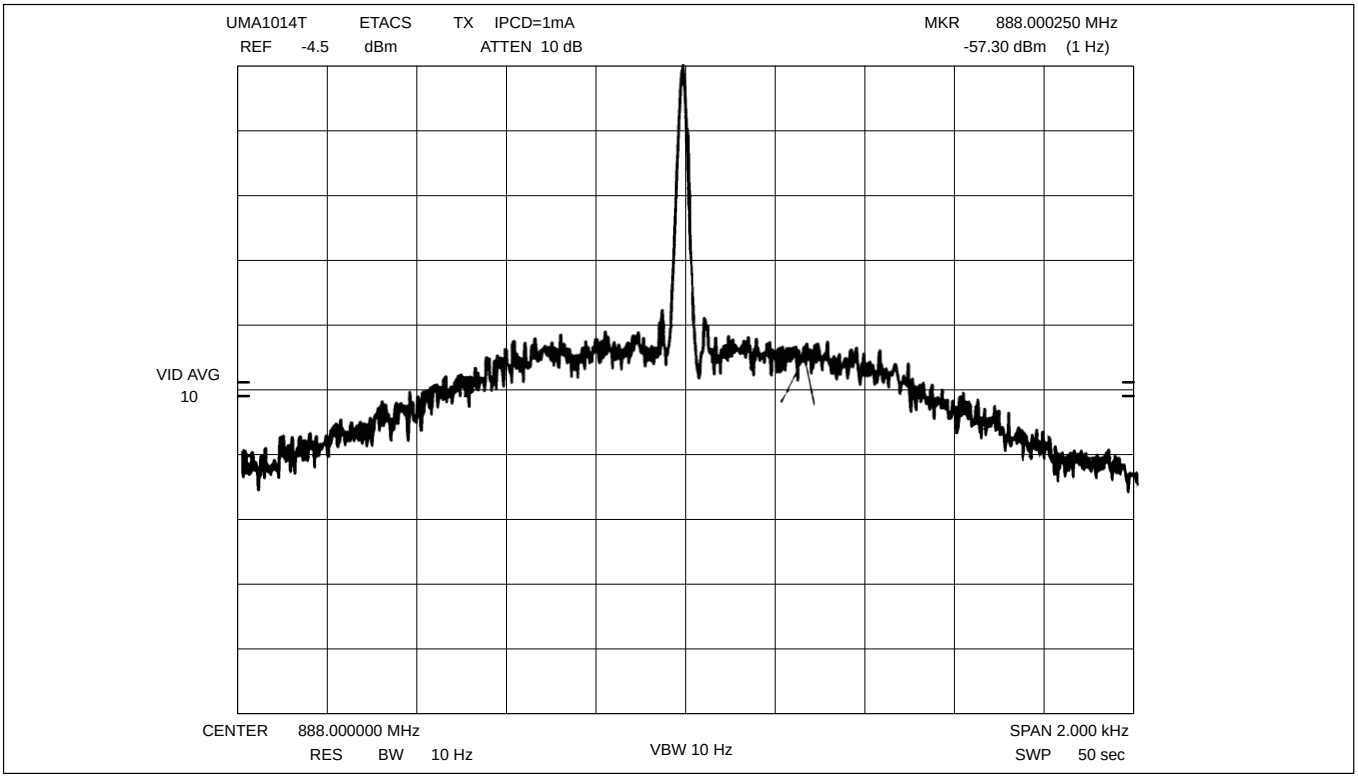


Figure 8. Typical Carrier Spectrum – 2kHz Span

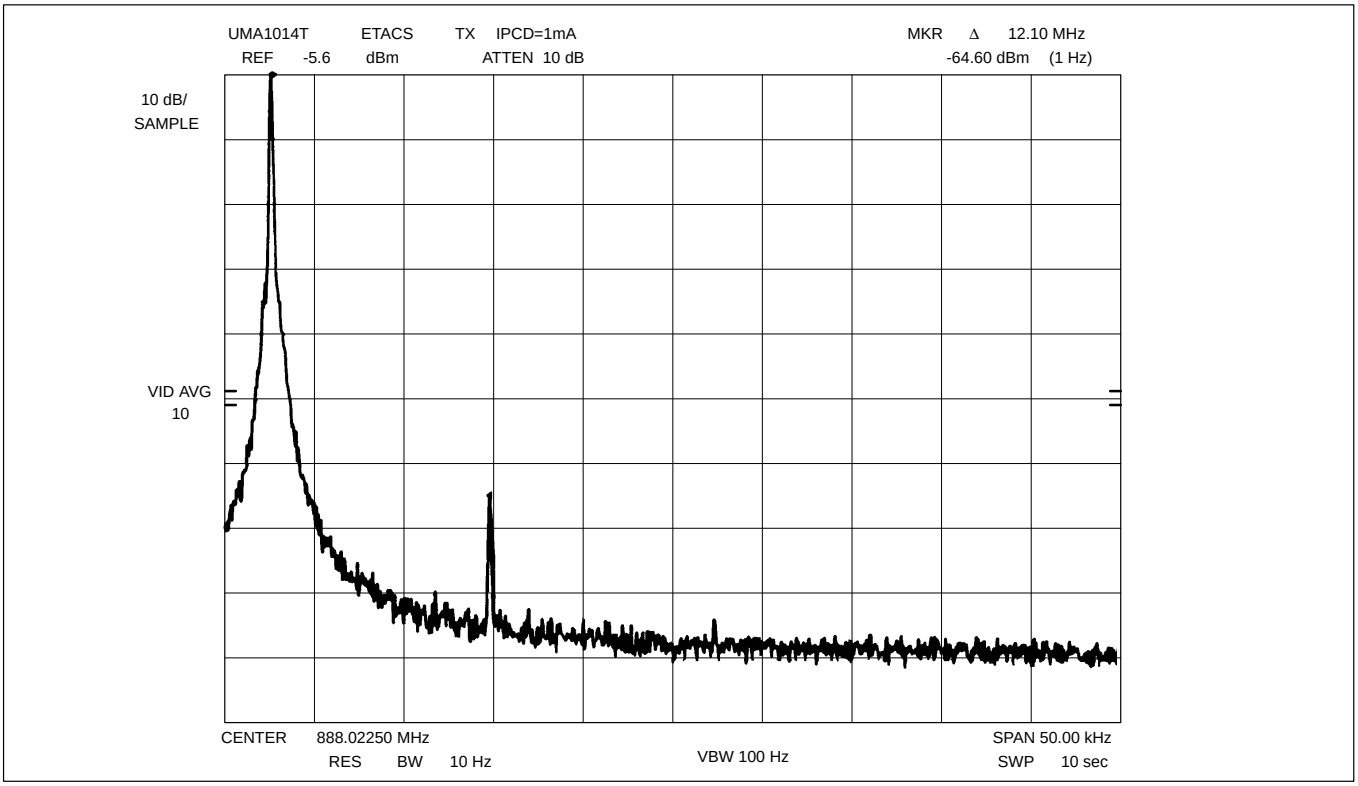


Figure 9. Typical Carrier Spectrum – 50kHz Span

Application report for the UMA1014T frequency synthesizer

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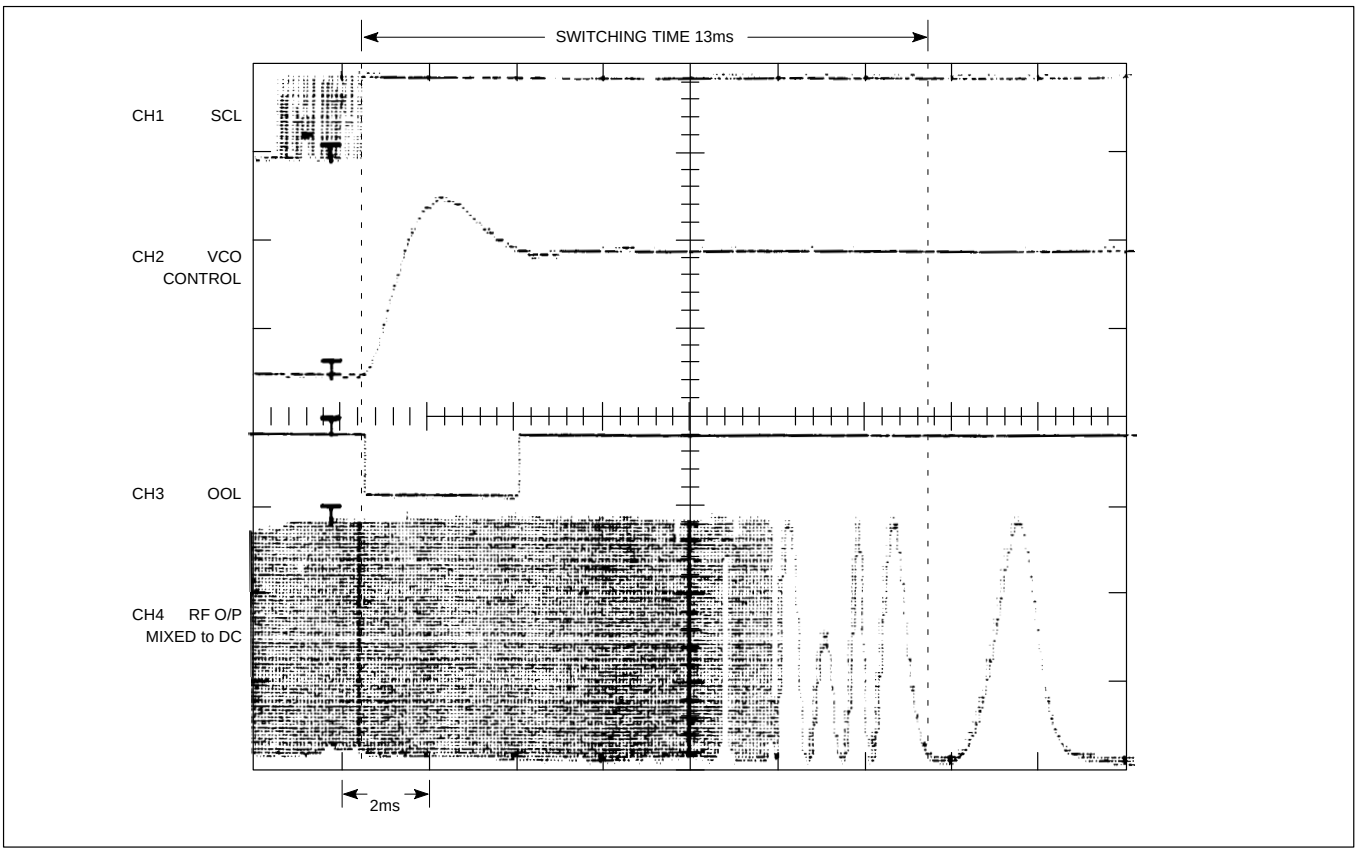

Figure 10. Typical Switching Waveforms