

# AN5491K

Synchronous signal and deflection distortion correction processing IC supporting I<sup>2</sup>C bus for HD, wide television

## ■ Overview

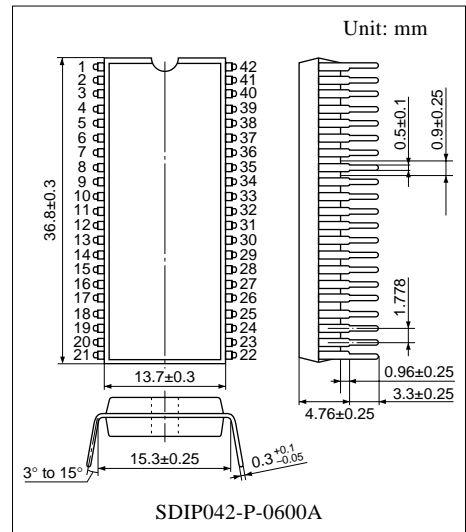
The AN5491K is a deflection processor IC for synchronous signal processing and screen distortion correction. It synchronizes with the input signal of High-vision, wide television, NTSC, PAL and VGA by the external binary input signal of them so that a multimedia television can be realized easily.

## ■ Features

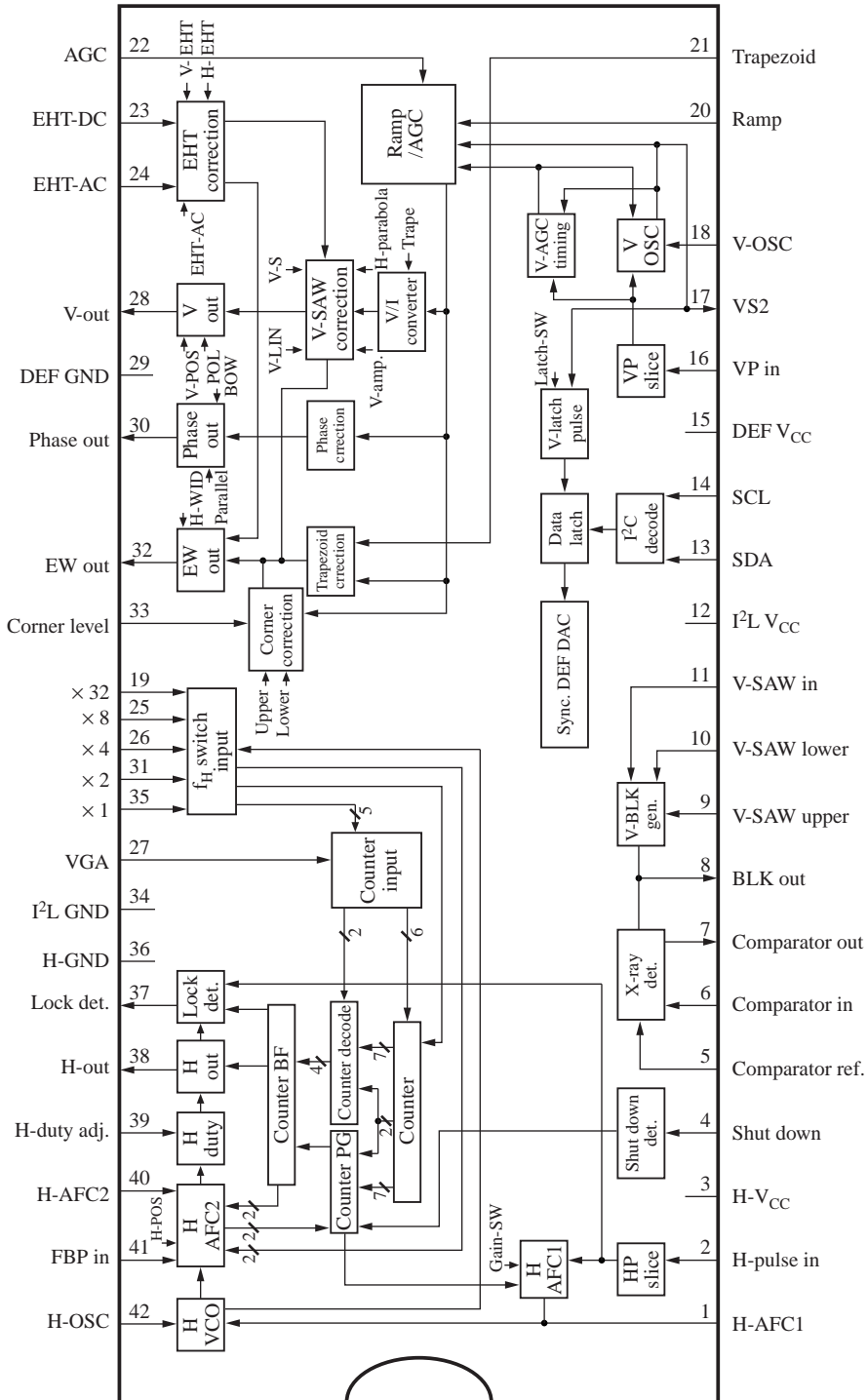
- Supports the multiple-point horizontal frequency (15.7 kHz to 62.7 kHz)
- Horizontal duty is controllable by external voltage.
- Built-in full functions for correction (Horizontal and vertical: 16 items)
- Over-current detection, shut-down and hold-down

## ■ Applications

- High-vision televisions, Wide screen televisions and Projection televisions



■ Block Diagram



### ■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	H-AFC1	22	V-AGC
2	H-pulse input	23	EHT-DC input
3	H-V <sub>CC</sub> (6.2 V)	24	EHT-AC input
4	Shut down SW	25	× 8
5	Comparator ref. (6.5 V)	26	× 4
6	Comparator	27	VGA
7	Comparator output	28	V-output
8	BLK output	29	DEF GND
9	V-SAW slice voltage (High)	30	Phase output
10	V-SAW slice voltage (Low)	31	× 2
11	V-SAW input	32	EW output
12	I <sup>2</sup> L V <sub>CC</sub> (5 V)	33	Corner slice voltage
13	I <sup>2</sup> C SDA input	34	I <sup>2</sup> L GND
14	I <sup>2</sup> C SCL input	35	× 1
15	DEF V <sub>CC</sub> (9 V)	36	H-GND
16	V-pulse input	37	Lock det.
17	V-pulse output	38	H-output
18	V-OSC	39	H-duty
19	× 32	40	H-AFC2
20	V-ramp	41	FBP input
21	Trapezoid correction voltage	42	H-OSC

### ■ Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
Supply voltage	V <sub>CC</sub>	V <sub>CC1</sub>	5.6	V
		V <sub>CC2</sub>	10	
Supply current	I <sub>CC</sub>	I <sub>CC1</sub>	24	mA
		I <sub>CC2</sub>	29	
		I <sub>3</sub>	14	
Power dissipation *2	P <sub>D</sub>	600		mW
Operating ambient temperature *1	T <sub>opr</sub>	-20 to +70		°C
Storage temperature *1	T <sub>stg</sub>	-55 to +150		°C

Note) \*1: Except for the operating ambient temperature and storage temperature, all ratings are for T<sub>a</sub> = 25°C.

\*2: The power dissipation shown is for the independent IC without a heat sink in free air at T<sub>a</sub> = 70°C.

### ■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	$V_{CC1}$	4.5 to 5.0 to 5.5	V
	$V_{CC2}$	8.1 to 9.0 to 9.9	

### ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC characteristics						
Circuit current $I_{CC1}$	$I_{12}$	$V_{CC1} = 5\text{ V}$ , $V_{CC2} = 9\text{ V}$	13.6	17.0	20.4	mA
Circuit current $I_{CC2}$	$I_{15}$	$V_{CC1} = 5\text{ V}$ , $V_{CC2} = 9\text{ V}$	16.8	21.0	25.2	mA
Circuit current $I_{CC3}$	$I_3$	$V_{CC1} = 5\text{ V}$ , $V_{CC2} = 9\text{ V}$ , $V_{CC3} = 6.5\text{ V}$	6.0	7.5	9.0	mA
Synchronizing signal processing						
Horizontal free-running oscillation frequency 1 [Divide-by-8]	$f_{HO8}$	Pin 2: Without input, Pin 25: High Pins 19, 26, 31, 35: Low	61.5	62.7	63.9	kHz
Horizontal free-running oscillation frequency 2 [Divide-by-16]	$f_{HO16}$	Pin 2: Without input Pins 19, 25, 26, 31, 35: Low	30.8	31.4	32.0	kHz
Horizontal free-running oscillation frequency 3 [Divide-by-32]	$f_{HO32}$	Pin 2: Without input Pin 19: High	15.4	15.7	16.0	kHz
Horizontal output pulse duty cycle 1 [Divide-by-32]	$\tau_{HO1}$	Pin 2: Without input, Pin 39: 2 V Pin 19: High	11.7	14.0	16.6	$\mu\text{s}$
Horizontal output pulse duty cycle 2 [Divide-by-32]	$\tau_{HO2}$	Pin 2: Without input, Pin 39: 5 V Pin 19: High	23.9	28.5	33.7	$\mu\text{s}$
Horizontal high-level output voltage	$V_{FHH}$	DC voltage for pin 38 high-level	2.8	3.5	4.2	V
Horizontal low-level output voltage	$V_{FHL}$	DC voltage for pin 38 low-level	0	—	0.3	V
Horizontal output start voltage	$V_{FHS}$	Minimum voltage of pin 3 to become $f > 10\text{ kHz}$ when horizontal oscillation output is 1 V[p-p] or more in divide-by-32 mode.	—	4.2	5.0	V
Screen center variable range 1 [Divide-by-16]	$t_{DH16}$	Pin 25: Low, Pins 19, 26, 31, 35: High Change amount of phase difference between $H_p$ and H-out of Data 08: [00] to [1F]	2.16	2.70	3.24	$\mu\text{s}$
Screen center variable range 2 [Divide-by-32]	$t_{DH32}$	Pin 19: Low, Change amount of phase difference between $H_p$ and H out of Data 08: [00] to [1F]	3.8	4.8	5.8	$\mu\text{s}$
Horizontal input pulse threshold voltage	$V_{T2}$	Slice level of pin 2	0.9	1.5	2.1	V
Over-voltage protective operation voltage	$V_4$	Pin 4 voltage at $I_4 = 50\text{ }\mu\text{A}$	0.60	0.75	0.90	V

**■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Deflection correction processing</b>						
$V_P$ pulse for OSD low-level	$V_{\text{LOSD}}$	$V_{\text{CC1}} = 5\text{ V}$ , $V_{\text{CC2}} = 9\text{ V}$	0	—	0.4	V
$V_P$ pulse for OSD high-level	$V_{\text{HOSD}}$	$V_{\text{CC1}} = 5\text{ V}$ , $V_{\text{CC2}} = 9\text{ V}$	2.2	2.75	3.3	V
EHT-AC input pin voltage	$V_{24}$	Pin 24: Open	2.00	2.45	2.90	V
Vertical input signal threshold voltage	$V_{\text{TFV}}$	Pin 16: Input	0.9	1.5	2.1	V
Vertical free-running oscillation frequency	$f_{\text{VO}}$	Pin 16: Without input external $R = 10\text{ k}\Omega$ , $C = 3.3\text{ }\mu\text{F}$	35	44	53	Hz
Typical vertical output amplitude	$V_V$	V amplitude DAC: Typ.	0.88	1.10	1.32	V[p-p]
Typical EW output amplitude	$V_{\text{EW}}$	EW output amplitude for typical vertical output amplitude = 1.25 V[p-p]	0.8	1.0	1.2	V[p-p]
Phase out amplitude	$V_{\text{PHASE}}$	Side pin parallel, DAC: Typ.	-0.1	0	0.1	V[p-p]
Ramp waveform amplitude	$V_{\text{RAMP}}$	$f_v = 50\text{ Hz}$ to $120\text{ Hz}$	2.15	2.45	2.75	V[p-p]
AGC input and output current	$I_{\text{AGC}}$		1.6	2.0	2.4	mA
Service SW: ON time	$V_{28\text{SW}}$		3.1	3.5	3.9	V
Vertical output DC						
BLK pulse high-level	$V_{\text{HBLK}}$		4.5	5.0	5.5	V
BLK pulse low-level	$V_{\text{LBLK}}$		0	—	0.4	V
Vertical output amplitude variable ratio (max.)	$\Delta V_{\text{AMPmax}}$	V amplitude ratio between typ. $\rightarrow$ max.	+40	+50	+60	%
Vertical output amplitude variable ratio (min.)	$\Delta V_{\text{AMPmin}}$	V amplitude ratio between typ. $\rightarrow$ max.	-40	-50	-60	%
Vertical output DC variable amount (min.)	$\Delta V_{\text{SHIFTmin}}$	Vertical DC: Typ. $\rightarrow$ min.	-0.28	-0.38	-0.48	V
Vertical output DC variable amount (max.)	$\Delta V_{\text{SHIFTmax}}$	Vertical DC: Typ. $\rightarrow$ max.	+0.28	+0.38	+0.48	V
Vertical output trapezoidal waveform correction variable amount (min.)	$\Delta V_{\text{TRAPmin}}$	Trapezoidal waveform correction: Typ. $\rightarrow$ min.	-0.28	-0.38	-0.48	V
Vertical output trapezoidal waveform correction variable amount (max.)	$\Delta V_{\text{TRAPmax}}$	Trapezoidal waveform correction: Typ. $\rightarrow$ max.	+0.28	+0.38	+0.48	V
External trapezoidal waveform center voltage	$V_{21}$		2.4	3.0	3.6	V
Vertical output center DC level	$V_{28}$		2.8	3.5	4.2	V
EW output (min.) to parabolic amplitude change	$V_{\text{EWmin}}$	Parabolic amplitude: Min.	-0.1	0	0.1	V[p-p]
EW output (max.) to parabolic amplitude change	$V_{\text{EWmax}}$	Parabolic amplitude: Max.	1.4	1.8	2.2	V[p-p]
EW output (min.) (DC) to horizontal amplitude change	$\Delta V_{\text{EWmin}}$	Horizontal amplitude: Min.	-0.95	-1.15	-1.35	V
EW output (max.) (DC) to horizontal amplitude change	$\Delta V_{\text{EWmax}}$	Horizontal amplitude: Max.	+0.95	+1.15	+1.35	V
EW output (bottom voltage) 1 to EHT-DC change	$\Delta V_{\text{EDC1}}$	EHT-DC: 5.0 V $\rightarrow$ 3.8 V Horizontal EHT: Max. EHT-AC gain: Min.	+1.04	+1.30	+1.56	V

### ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Deflection correction processing (continued)						
EW output (bottom voltage) 2 to EHT-DC change	$\Delta V_{\text{EDC}2}$	EHT-DC: 5.0 V $\rightarrow$ 6.2 V Horizontal EHT: Max. EHT-AC gain: Min.	-1.04	-1.30	-1.56	V
EW output (bottom voltage) 1 to EHT-AC change	$\Delta V_{\text{EAC}1}$	EHT-AC: 2.35 V $\rightarrow$ 1.35 V Horizontal EHT: Max. EHT-AC gain: Max.	+0.25	+0.35	+0.45	V
EW output (bottom voltage) 2 to EHT-AC change	$\Delta V_{\text{EAC}2}$	EHT-AC: 2.35 V $\rightarrow$ 3.35 V Horizontal EHT: Max. EHT-AC gain: Max.	-0.25	-0.35	-0.45	V
EW output parabolic DC level	$V_{32}$	Typ.	2.2	2.7	3.4	V
Parallelogram correction fluctuation 1 (upper side)	$\Delta V_{\text{UPH}1}$	Parallelogram correction: Typ. $\rightarrow$ min.	+0.16	+0.26	+0.36	V
Parallelogram correction fluctuation 2 (upper side)	$\Delta V_{\text{UPH}2}$	Parallelogram correction: Typ. $\rightarrow$ max.	-0.16	-0.26	-0.36	V
Parallelogram correction fluctuation 3 (lower side)	$\Delta V_{\text{BPH}1}$	Parallelogram correction: Typ. $\rightarrow$ min.	-0.25	-0.35	-0.45	V
Parallelogram correction fluctuation 4 (lower side)	$\Delta V_{\text{BPH}2}$	Parallelogram correction: Typ. $\rightarrow$ max.	+0.16	+0.26	+0.36	V
Bow shape correction fluctuation 1 (upper side)	$\Delta V_{\text{USD}1}$	Bow shape correction: Typ. $\rightarrow$ min.	-0.24	-0.34	-0.44	V
Bow shape correction fluctuation 2 (upper side)	$\Delta V_{\text{USD}2}$	Bow shape correction: Typ. $\rightarrow$ max.	+0.12	+0.22	+0.32	V
Bow shape correction fluctuation 3 (lower side)	$\Delta V_{\text{BSD}1}$	Bow shape correction: Typ. $\rightarrow$ min.	-0.17	-0.27	-0.37	V
Bow shape correction fluctuation 4 (lower side)	$\Delta V_{\text{BSD}2}$	Bow shape correction: Typ. $\rightarrow$ max.	+0.12	+0.22	+0.32	V
I <sup>2</sup> C interface						
SCL, SDA input threshold voltage	$V_{\text{TH}}$	$V_{\text{CC}1} = 5\text{ V}$	1.5	—	3.0	dB
Sink capacity at ACK	$V_{\text{ACK}}$	$I = 3\text{ mA}$ in case of pull-up resistor 1.6 $\Omega$	—	—	0.4	V
Maximum clock frequency	$f_{\text{SCL}}$		100	—	—	kHz

#### • Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC characteristics						
AGC pulse width	$\tau_{\text{AGC}}$		—	95	—	$\mu\text{s}$
Ramp discharge current	$I_{\text{RAMP}1}$		3.6	—	—	mA
Ramp charge current 1	$I_{\text{RAMP}2}$	$f = 120\text{ Hz}$ , Pin 4: 5.7 V	—	138	—	$\mu\text{A}$
Ramp charge current 2	$I_{\text{RAMP}3}$	$f = 30\text{ Hz}$ , Pin 4: 7.5 V	—	32.9	—	$\mu\text{A}$

### ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

#### • Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC characteristics (continued)						
BLK output amplitude	$V_{\text{BLK}}$		4	5	6	V
Vertical output drive current	$I_{28}$		-2	—	—	mA
Vertical output amplitude fluctuation with supply voltage	$\frac{V_V}{\Delta V_{\text{CC}}}$	Difference of $V_{\text{CCmax}} - V_{\text{CCmin}}$	—	0.1	—	V
Vertical output DC fluctuation with supply voltage	$\frac{V_{28}}{\Delta V_{\text{CC}}}$	Difference of $V_{\text{CCmax}} - V_{\text{CCmin}}$	—	1.0	—	V
EW output amplitude fluctuation with supply voltage	$\frac{V_{\text{EW}}}{\Delta V_{\text{CC}}}$	Difference of $V_{\text{CCmax}} - V_{\text{CCmin}}$	—	0.1	—	V
EW output DC fluctuation with supply voltage	$\frac{V_{32}}{\Delta V_{\text{CC}}}$	Difference of $V_{\text{CCmax}} - V_{\text{CCmin}}$	—	1.0	—	V
Synchronizing signal processing						
Horizontal free-running oscillation frequency [Divide-by-15]	$f_{\text{HO15}}$	Pin 2: Without input, Pin 19: Low Pins 25, 26, 31, 35: High	32.9	33.5	34.1	kHz
Horizontal output pull-in range [Divide-by-8]	$f_{\text{HP8}}$	Pin 2: Without input, Pin 25: High Pins 19, 26, 31, 35: Low	$\pm 2\ 000$	$\pm 2\ 600$	—	Hz
Comparator detection operation voltage	$V_6$	Pin 6: Minimum voltage to become high, Pin 5: 6.2 V	5.7	6.3	6.9	V
Lock detection output voltage	$V_{37}$	$V_{37}$ in horizontal AFC lock mode	5.7	6.3	6.9	V
Lock detection charge and discharge current	$I_{\text{LOCK}}$	DC measurement in divide-by-32	—	$\pm 0.8$	—	mA
FBP (AFC2) slice level	$V_{\text{TFBP}}$	Minimum voltage of pin 41 at which AFC operates.	1.5	1.9	2.3	V
Horizontal AFC $\mu$	$\mu$	DC measurement in divide-by-32	—	37	—	$\mu\text{A}/\mu\text{s}$
Horizontal VCO $\beta$	$\beta$	Slant of $\beta$ curve near $f = 15.7$ kHz	—	1.9	—	Hz/mV
FBP allowable range 1 [Divide-by-8]	$t_{\text{FBP8}}$	Time from H-out rise to FBP center	3	—	9	$\mu\text{s}$
FBP allowable range 2 [Divide-by-16]	$t_{\text{FBP16}}$	Time from H-out rise to FBP center	4	—	13	$\mu\text{s}$
FBP allowable range 3 [Divide-by-32]	$t_{\text{FBP32}}$	Time from H-out rise to FBP center	6	—	20	$\mu\text{s}$
AFC1 reference current 1	$I_{\text{AFC1}}$	Data 0C = "11" (D1, D0)	—	0.82	—	mA
AFC1 reference current 2	$I_{\text{AFC2}}$	Data 0C = "01" (D1, D0)	—	1.1	—	mA
AFC1 reference current 3	$I_{\text{AFC3}}$	Data 0C = "10" (D1, D0)	—	1.5	—	mA
AFC1 reference current 4	$I_{\text{AFC4}}$	Data 0C = "00" (D1, D0)	—	2.0	—	mA
Horizontal output pull-in range 1 [Divide-by-16]	$f_{\text{HP16}}$	Pin 2: Without input Pins 19, 25, 26, 31, 35: Low	$\pm 1\ 000$	$\pm 1\ 300$	—	Hz
Horizontal output pull-in range 2 [Divide-by-32]	$f_{\text{HP32}}$	Pin 2: Without input Pin 19: High	$\pm 500$	$\pm 650$	—	Hz

### ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

#### • Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Deflection correction processing						
Vertical output S-shape variable ratio 1	$\Delta V_{SC1}$	Vertical S-shape: Ratio of min. $\rightarrow$ max.	—	-28	—	%
Vertical output S-shape variable ratio 2	$\Delta V_{SC2}$	Vertical S-shape: Ratio of min. $\rightarrow$ max. (Change of V-out 40% to 60% point)	—	1.5	—	%
Vertical output (upper side) linearity variable ratio 1	$\Delta V_{ULIN1}$	Vertical linearity (upper side): Typ. $\rightarrow$ max.	—	+12	—	%
Vertical output (upper side) linearity variable ratio 2	$\Delta V_{ULIN2}$	Vertical linearity (upper side): Typ. $\rightarrow$ min.	—	-10	—	%
Vertical output (lower side) linearity variable ratio 1	$\Delta V_{BLIN1}$	Vertical linearity (lower side): Typ. $\rightarrow$ max.	—	+9	—	%
Vertical output (lower side) linearity variable ratio 2	$\Delta V_{BLIN2}$	Vertical linearity (lower side): Typ. $\rightarrow$ min.	—	-11	—	%
Vertical output EHT-DC change 1	$\Delta V_{EDC1}$	EHT-DC = 5.0 V $\rightarrow$ 3.8 V Vertical EHT: Max., EHT gain: Max.	—	-30	—	%
Vertical output EHT-DC change 2	$\Delta V_{EDC2}$	EHT-DC = 5.0 V $\rightarrow$ 6.2 V Vertical EHT: Max., EHT gain: Max.	—	+25	—	%
Vertical output EHT-AC change 1	$\Delta V_{EAC1}$	EHT-AC = 2.35 V $\rightarrow$ 1.35 V EHT: Max., EHT gain: Max.	—	-12	—	%
Vertical output EHT-AC change 2	$\Delta V_{EAC2}$	EHT-AC = 2.35 V $\rightarrow$ 3.35 V EHT: Max., EHT gain: Max.	—	+12	—	%
EW output (min.) to trapezoidal waveform change	$\Delta V_{TRAPmin}$	Trapezoidal SW: On, Trapezoidal: Typ. $\rightarrow$ min.	—	-40	—	%
EW output (max.) to trapezoidal waveform change	$\Delta V_{TRAPmax}$	Trapezoidal SW: On, Trapezoidal: Typ. $\rightarrow$ max.	—	+40	—	%
EW output (min.) to upper corner trapezoidal waveform change	$\Delta V_{UCmin}$	Upper corner: Typ. $\rightarrow$ min. Corner slice voltage: 1 V	—	-45	—	%
EW output (max.) to upper corner trapezoidal waveform change	$\Delta V_{UCmax}$	Upper corner: Typ. $\rightarrow$ max. Corner slice voltage: 1 V	—	+45	—	%
EW output (min.) to lower corner trapezoidal waveform change	$\Delta V_{BCmin}$	Lower corner: Typ. $\rightarrow$ min. Corner slice voltage: 1 V	—	-45	—	%
EW output (max.) to lower corner trapezoidal waveform change	$\Delta V_{BCmax}$	Lower corner: Typ. $\rightarrow$ max. Corner slice voltage: 1 V	—	+45	—	%
External trapezoidal waveform correction fluctuation 1 (Parabolic amplitude)	$\Delta V_{ETR1}$	External trapezoidal correction: 3 V $\rightarrow$ 2 V	—	-40	—	%
External trapezoidal waveform correction fluctuation 2 (Parabolic amplitude)	$\Delta V_{ETR2}$	External trapezoidal correction: 3 V $\rightarrow$ 4 V	—	+40	—	%



■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>I<sup>2</sup>C interface</b>						
3, 4, 5, 6-bit DAC DNLE	L1	1LSB = $\{\text{Data(max.)} - \text{Data(00)}\}/7,15,31,63$	0.1	1.0	1.9	LSB/step
7-bit DAC DNLE (Except for 40)	L2	1LSB = $\{\text{Data(max.)} - \text{Data(00)}\}/127$	0.1	1.0	1.9	LSB/step
7-bit DAC DNLE (40 only)	L3	1LSB = $\{\text{Data(max.)} - \text{Data(00)}\}/127$	-1.0	1.0	2.0	LSB/step

■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	Voltage
1		<p>AFC1: Horizontal frequency detection pin</p> <ul style="list-style-type: none"> <li>Pin for adjusting the frequency of horizontal input pulse and the internal reference pulse.</li> <li>Connect a lag lead filter.</li> </ul>	<p>DC approx. 4.3 V</p>
2		<p>H-pulse in: Horizontal synchronizing signal input pin</p> <ul style="list-style-type: none"> <li>Polarity is as shown in the right figure (Negative).</li> <li>Slice level is 1.5 V.</li> <li>Input polarity is one polarity only (not corresponding to both polarities).</li> </ul>	<p>AC</p> <p>H rate</p>
3		<p>V<sub>CC</sub>: Horizontal system power supply (6.5 V) pin</p> <ul style="list-style-type: none"> <li>Connect an external zener</li> </ul>	<p>DC 6.5 V</p>
4		<p>Shut down: Control pin for shut-down</p> <ul style="list-style-type: none"> <li>Horizontal output stops (GND) if a voltage <math>1 V_{BE}</math> and over (more than approx. 0.75 V) is applied to the pin.</li> </ul>	<p>DC Normal: GND</p>

### ■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
5		Comparator ref.: Reference voltage input pin for comparator <ul style="list-style-type: none"> <li>• Attach zener diode externally (approx. 6.2 V)</li> <li>(Usable as reference voltage for hold-down)</li> </ul>	DC
6		Comparator: Input pin for comparator detection <ul style="list-style-type: none"> <li>• (Usable as pin for hold-down detection)</li> </ul>	DC
7		Comparator out: Comparator detection output pin <ul style="list-style-type: none"> <li>• Connect pull-up resistors outside the IC.</li> <li>(usable as hold-down control pin)</li> <li>Note) Use under 400 μA or less.</li> </ul>	DC Normally: High
8		BLK out: Blanking pulse output pin <ul style="list-style-type: none"> <li>• Normally: Low</li> <li>At BLK: High (5 V)</li> </ul>	DC At BLK: High
9		Upper side slice: Upper side slice voltage input pin for BLK pulse generation <div style="text-align: right;"> </div>	DC

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
10		<p>Lower side slice: Lower side slice voltage input pin for BLK Pulse generation</p>	DC
11		<p>V-SAW in: V-SAW input pin for BLK pulse generation</p>	AC
12	—	<p><math>V_{CC}</math>: Power supply (5 V) pin for DAC/I<sup>2</sup>L • Connect a pass capacitor (0.01 μF) between pin 12 and GND (pin 19).</p>	DC 5 V
13		<p>SDA: I<sup>2</sup>C data input pin</p>	DC 5 V
14		<p>SCL: I<sup>2</sup>C clock input pin</p>	DC 5 V
15	—	<p><math>V_{CC}</math>: Pin for deflection system power supply (9 V) • Connect a pass capacitor between the pin and GND.</p>	DC 9 V

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
16		<p>V-pulse in: Vertical sync. signal input pin</p> <ul style="list-style-type: none"> <li>• Polarity is as shown in the right figure (Negative)</li> <li>• Slice level is 1.5 V.</li> <li>• Input polarity is only one polarity (Not correspond to both polarities)</li> </ul>	<p>AC (Pulse)</p>
17		<p>V-pulse out: Vertical sync. signal output pin</p> <ul style="list-style-type: none"> <li>• If vertical sync. signal input is present: Outputs the pulse synchronized with input V.</li> <li>Not present: Outputs free-running V pulse. (Usable for microcomputer OSD control)</li> </ul>	<p>AC (Pulse)</p>
18		<p>V-OSC: Vertical oscillation pin</p> <ul style="list-style-type: none"> <li>• Connect CR.</li> <li>• Free-running oscillation when there is no input.</li> </ul>	<p>AC</p>
19		<p>× 32: Horizontal free-running oscillation frequency control pin</p> <ul style="list-style-type: none"> <li>• To be used by high/low control.</li> <li>• Input is controlled by open collector output.</li> </ul>	<p>DC</p>
20		<p>V-ramp pin:</p> <ul style="list-style-type: none"> <li>• The pin for generating reference V sawtooth waveform for IC inside.</li> <li>• Connect an 0.22 μF mylar capacitor.</li> </ul>	<p>AC</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
21		<p>External trapezoidal waveform: The pin for controlling trapezoidal waveform compensation from outside.</p> <ul style="list-style-type: none"> <li>Used by linking to V-position shift (at AC coupling), typ. 3.0 V</li> </ul>	<p>DC 2 V to 4 V</p>
22		<p>V-AGC: Vertical AGC pin</p> <ul style="list-style-type: none"> <li>AGC pin to make a vertical output amplitude constant.</li> <li>Connect 3.3 μF tantalum capacitor.</li> </ul>	<p>DC</p>
23		<p>EHT-DC: Pin for extremely high-tension compensation (EHT)</p> <ul style="list-style-type: none"> <li>DC-coupled to pin.</li> </ul>	<p>DC Operating range: 3.8 V to 6.2 V</p>
24		<p>EHT-AC Pin for extremely high-tension compensation</p> <ul style="list-style-type: none"> <li>AC-coupled to pin.</li> </ul>	<p>AC 2.35 V in an open mode Operating range: 1.35 V to 3.35 V</p>
25		<p>× 8: Horizontal free-running oscillation frequency control pin</p> <ul style="list-style-type: none"> <li>To be used by high/low control.</li> <li>Input is controlled by open collector output.</li> </ul>	<p>DC</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
26		<p>× 4: Horizontal free-running oscillation frequency control pin</p> <ul style="list-style-type: none"> <li>To be used by high/low control.</li> <li>Input is controlled by open collector output.</li> </ul>	DC
27		<p>V-FB: Forced progressive mode pin</p> <ul style="list-style-type: none"> <li>To be used by high/low control.</li> <li>At high: Multi-point mode</li> <li>At low: Progressive mode</li> </ul>	DC
28		<p>V-out: V sawtooth waveform output pin</p> <ul style="list-style-type: none"> <li>Typ. 1.25 V[p-p]</li> </ul>	<p>AC</p>
29	—	<p>GND: GND pin for deflection-system circuit (9 V)</p>	<p>DC GND</p>
30		<p>Phase out: Pin for side pin (Bow shape) correction, parallelogram correction and control pulse output.</p> <ul style="list-style-type: none"> <li>Connect to H-AFC2 pin via 1 μF (non-polarity) capacitor.</li> </ul>	<p>AC</p> <p>DC approx. 3.7 V</p>

■ Terminal Equivalent Circuits (continued)

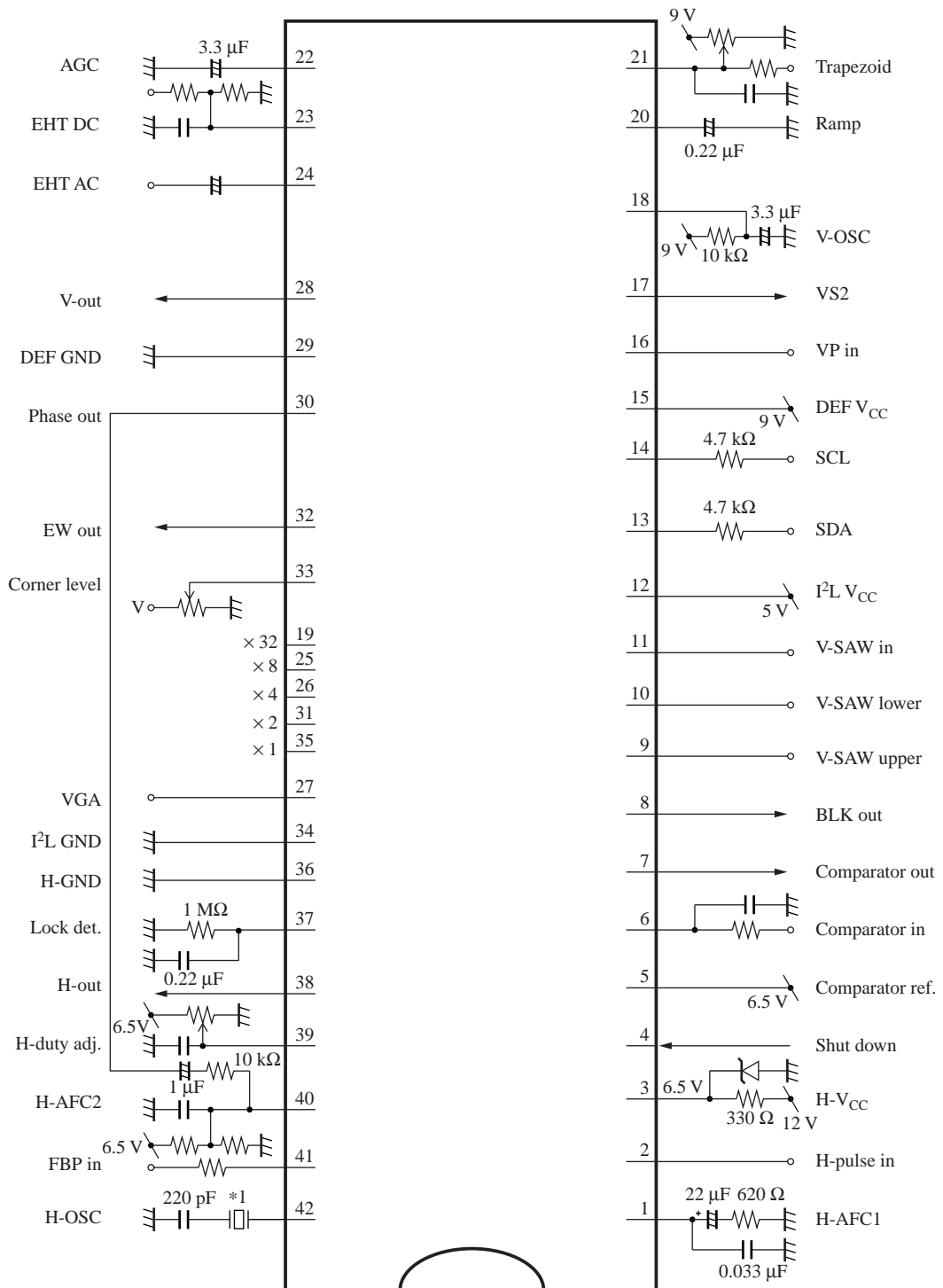
Pin No.	Equivalent circuit	Description	Voltage
31		<p>× 2: Horizontal free-running oscillation frequency control pin</p> <ul style="list-style-type: none"> <li>To be used by high/low control.</li> <li>Input is controlled by open collector output.</li> </ul>	DC
32		<p>EW out: Parabolic waveform output pin</p>	<p>AC</p>
33		<p>Corner slice: The voltage to set a slice point of upper and lower corner correction.</p> <ul style="list-style-type: none"> <li>The correction gain can be controlled independently by I<sup>2</sup>C bus for upper and lower, respectively.</li> </ul>	<p>DC</p> <p>Externally set at 0 VDC to 1.25 VDC</p>
34	—	GND: GND pin for 5 V system (I <sup>2</sup> C/I <sup>2</sup> L)	DC GND
35		<p>× 1: Horizontal free-running oscillation frequency control pin</p> <ul style="list-style-type: none"> <li>To be used by high/low control.</li> </ul>	DC
36	—	GND: GND pin for 6.5 V system (Horizontal system)	DC GND
37		<p>Lock det.: Horizontal lock detection pin</p> <ul style="list-style-type: none"> <li>Connect 0.022 μF and 1 MΩ between the pin and GND.</li> </ul>	<p>DC</p> <p>At lock mode: 6 V</p> <p>At unlocked mode: GND</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
38		<p>H-out: Horizontal output pin</p> <ul style="list-style-type: none"> <li>The length of high-period can be adjusted by a separate pin.</li> </ul>	<p>AC</p>
39		<p>H-duty: Pin for controlling the length of high-period of horizontal output pulse.</p> <ul style="list-style-type: none"> <li>Apply DC voltage from the outside.</li> </ul>	<p>DC</p> <p>1 V to 5 V</p>
40		<p>AFC2: Horizontal phase detection pin</p> <ul style="list-style-type: none"> <li>Pin for controlling phase difference between horizontal output pulse and FBP.</li> <li>Phase out waveform is also connected to this pin via capacitor.</li> <li>Connect 0.015 μF between this pin and GND.</li> </ul>	<p>DC</p> <p>1.5 V to 4.5 V</p>
41		<p>FBP input pin:</p> <ul style="list-style-type: none"> <li>Slices at 1.9 V (in the IC) and then uses as AFC2 control pulse.</li> <li>Do not input any signal under GND inside the IC.</li> </ul>	<p>AC</p>
42		<p>H-OSC: Reference oscillation pin (500 kHz)</p> <ul style="list-style-type: none"> <li>Connect CERALOCK (CSB500F48), and temperature guaranteed (N750) 220 pF capacitor in series between this pin and GND.</li> </ul>	<p>AC</p>



■ Application Circuit Example



\*1: Horizontal oscillator  
 TAFC5B500F48  
 [Murata Manufacturing Co. Ltd.]