0.5 Micron CMOS Core Library
Standard Cell Datasheets
AMI500MXSC 5.0 Volt
Section 3
Revision 1.1

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AMI500MXSC 0.5 micron CMOS Standard Cell

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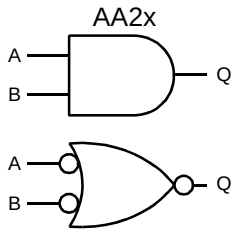
DATASHEETS

Description

AA2x is a family of 2-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... AA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: AA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	AA21	AA22	AA24	AA26
A	1.0	1.0	1.9	1.8
B	1.0	1.0	2.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA21	1.2	0.521	2.4
AA22	1.2	0.682	3.6
AA24	2.0	1.300	6.3
AA26	2.0	1.632	9.2

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

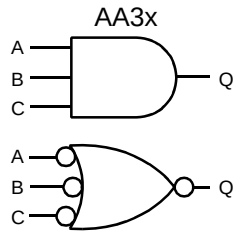
AA21	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.335 0.345	0.640 0.644	1.007 0.984	1.436 1.390	1.789 1.744
AA22	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.363 0.327	0.672 0.655	1.013 0.967	1.320 1.236	1.661 1.532
AA24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.314 0.230	0.620 0.578	0.937 0.849	1.231 1.109	1.536 1.392
AA26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.379 0.345	0.711 0.648	1.022 0.905	1.325 1.188	1.625 1.457

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AA3x is a family of 3-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

HDL Syntax

Verilog ..... AA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AA31	AA32	AA34	AA36
A	1.0	1.0	1.9	2.8
B	1.0	1.0	1.8	2.8
C	1.0	1.0	1.9	2.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA31	1.5	0.638	3.0
AA32	1.8	0.810	4.3
AA34	2.5	1.557	8.0
AA36	3.5	2.340	12.3

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

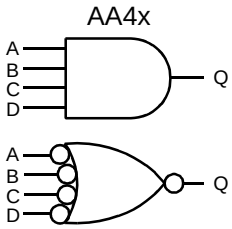
AA31	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.421 0.392	0.720 0.702	1.088 1.056	1.526 1.470	1.890 1.816
AA32	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.438 0.397	0.774 0.732	1.120 1.043	1.422 1.311	1.750 1.610
AA34	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.367 0.311	0.702 0.637	1.010 0.958	1.314 1.227	1.634 1.511
AA36	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.352 0.341	0.682 0.632	0.998 0.925	1.317 1.230	1.641 1.485

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AA4x is a family of 4-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

HDL Syntax

Verilog ..... AA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AA41	AA42	AA44	AA46
A	1.1	1.0	2.9	3.1
B	1.1	1.0	2.9	3.2
C	1.0	1.1	2.8	3.1
D	1.0	1.0	3.0	3.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQLpd (Eq-load)
AA41	2.0	0.741	3.3
AA42	2.0	0.902	4.5
AA44	4.8	2.333	11.8
AA46	5.2	2.654	13.6

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

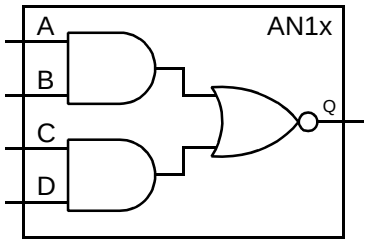
AA41	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.472 0.430	0.782 0.755	1.155 1.117	1.594 1.537	1.956 1.886
AA42	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.523 0.446	0.839 0.782	1.177 1.107	1.480 1.383	1.812 1.679
AA44	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.363 0.289	0.706 0.600	1.038 0.878	1.341 1.157	1.654 1.471
AA46	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.423 0.356	0.771 0.656	1.067 0.902	1.367 1.179	1.681 1.456

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN1x is a family of AND-NOR circuits consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

HDL Syntax

Verilog ..... AN1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN11	AN12	AN14	AN16
A	1.1	1.0	1.1	1.9
B	1.0	1.0	1.0	1.8
C	1.0	1.0	1.1	1.8
D	1.1	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN11	1.5	0.477	2.4
AN12	2.5	1.151	6.3
AN14	3.0	1.332	8.0
AN16	3.2	2.517	13.6

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

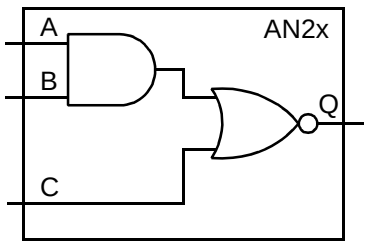
AN11	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.396 0.333	0.693 0.554	1.122 0.856	1.406 1.052	1.838 1.343
AN12	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.500 0.537	0.805 0.833	1.174 1.186	1.606 1.599	1.962 1.938
AN14	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.534 0.561	0.855 0.890	1.211 1.216	1.531 1.495	1.887 1.795
AN16	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.390 0.412	0.717 0.737	1.041 1.006	1.338 1.265	1.648 1.543

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN2x is a family of AND-NOR circuits consisting of one 2-input AND gate and a direct input into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	Q
H	H	X	L
X	X	H	L
All other combinations			H

HDL Syntax

Verilog ..... AN2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AN2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AN21	AN22	AN24	AN26
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.8
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN21	1.2	0.418	1.9
AN22	2.5	1.025	6.2
AN24	2.8	1.196	7.6
AN26	3.2	2.096	13.0

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

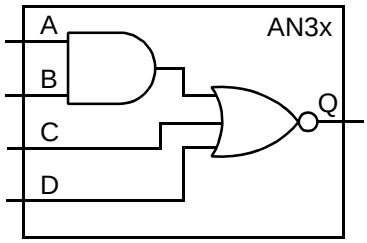
AN21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.257 0.377	0.499 0.665	0.856 1.045	1.089 1.288	1.434 1.651
AN22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.515 0.586	0.803 0.872	1.164 1.217	1.597 1.629	1.959 1.972
AN24	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.526 0.570	0.852 0.889	1.209 1.207	1.527 1.480	1.879 1.775
AN26	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.404 0.451	0.723 0.777	1.040 1.067	1.337 1.325	1.647 1.587

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN3x is a family of AND-NOR circuits consisting of one 2-input AND gate, and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... AN3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN31	AN32	AN34	AN36
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.8
C	1.0	1.0	1.0	1.8
D	1.0	1.1	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN31	1.5	0.572	2.2
AN32	2.8	1.047	6.5
AN34	2.8	1.211	7.6
AN36	3.8	2.321	14.8

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

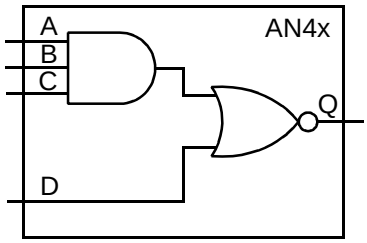
AN31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.343 0.395	0.516 0.552	0.856 0.836	1.196 1.109	1.536 1.391
AN32	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.526 0.597	0.820 0.880	1.179 1.222	1.607 1.634	1.963 1.980
AN34	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.502 0.542	0.814 0.860	1.157 1.182	1.465 1.461	1.806 1.763
AN36	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.419 0.445	0.735 0.766	1.049 1.052	1.342 1.316	1.651 1.594

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN4x is a family of AND-NOR circuits consisting of one 3-input AND gate, and a direct input into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
H	H	H	X	L
X	X	X	H	L
All other combinations				H

HDL Syntax

Verilog ..... AN4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN41	AN42	AN44	AN46
A	1.0	1.1	1.0	1.9
B	1.0	1.1	1.0	1.9
C	1.0	1.1	1.0	1.8
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN41	1.5	0.457	2.5
AN42	2.8	1.142	6.9
AN44	3.0	1.313	8.1
AN46	3.2	2.327	13.6

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

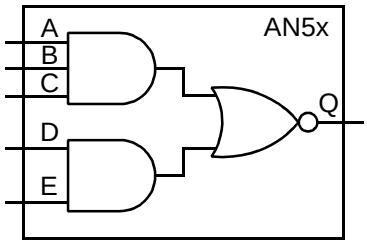
AN41	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.331 0.423	0.464 0.590	0.721 0.887	0.980 1.173	1.248 1.469
AN42	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.574 0.652	0.880 0.940	1.244 1.294	1.669 1.715	2.017 2.064
AN44	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.577 0.631	0.913 0.964	1.267 1.285	1.578 1.557	1.919 1.847
AN46	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.434 0.492	0.750 0.814	1.075 1.099	1.376 1.350	1.690 1.603

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN5x is a family of AND-NOR circuits consisting of one 3-input AND gate and one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN52	AN54	AN56
A	1.1	1.1	1.9
B	1.1	1.1	1.9
C	1.0	1.0	1.8
D	1.1	1.1	1.8
E	1.0	1.1	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN52	3.2	1.288	7.1
AN54	3.2	1.449	8.6
AN56	4.0	2.770	15.5

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

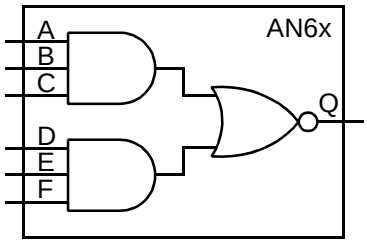
AN52	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.535 0.638	0.842 0.941	1.211 1.296	1.641 1.705	1.990 2.039
AN54	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.594 0.654	0.904 0.976	1.252 1.303	1.566 1.585	1.916 1.889
AN56	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.461 0.493	0.763 0.807	1.084 1.107	1.390 1.376	1.712 1.654

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN6x is a family of AND-NOR circuits consisting of two 3-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN62	AN64	AN66
A	1.1	1.0	1.9
B	1.1	1.0	1.9
C	1.1	1.0	1.9
D	1.0	1.1	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN62	3.2	1.399	7.7
AN64	3.8	1.576	8.8
AN66	4.2	2.975	15.8

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

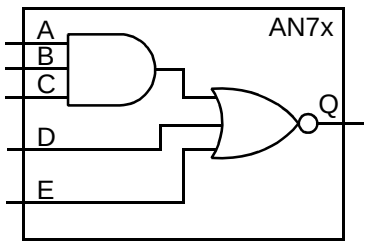
AN62	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.578 0.651	0.871 0.947	1.231 1.295	1.660 1.707	2.015 2.051
AN64	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.574 0.639	0.882 0.962	1.224 1.283	1.532 1.557	1.874 1.853
AN66	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.441 0.506	0.764 0.816	1.069 1.096	1.360 1.348	1.683 1.605

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN7x is a family of AND-NOR circuits consisting of one 3-input AND gate, and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN72	AN74	AN76
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.1	1.0	1.9
E	1.0	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN72	3.0	1.165	7.1
AN74	3.2	1.336	8.5
AN76	3.8	2.518	15.1

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

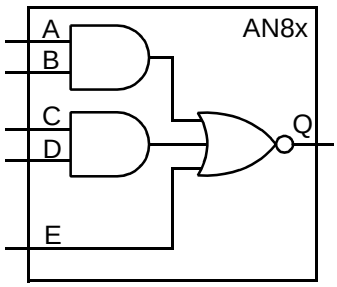
AN72	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.578 0.653	0.882 0.948	1.245 1.298	1.669 1.710	2.016 2.051
AN74	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.593 0.653	0.906 0.976	1.246 1.300	1.549 1.578	1.883 1.878
AN76	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.447 0.499	0.768 0.801	1.073 1.079	1.369 1.335	1.689 1.607

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN8x is a family of AND-NOR circuits consisting of two 2-input AND gates, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	X	X	X	L
X	X	H	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN82	AN84	AN86
A	1.1	1.0	1.9
B	1.0	1.0	1.9
C	1.1	1.0	1.9
D	1.1	1.1	1.9
E	1.0	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN82	3.5	1.462	8.9
AN84	4.0	1.643	10.5
AN86	4.5	3.096	17.8

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

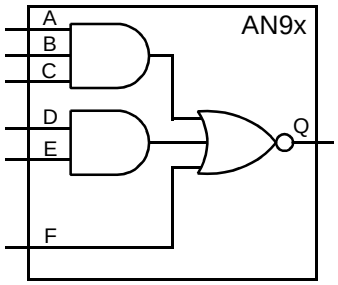
AN82	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.587 0.628	0.892 0.933	1.257 1.296	1.690 1.720	2.049 2.067
AN84	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.613 0.658	0.937 0.969	1.282 1.282	1.588 1.561	1.925 1.872
AN86	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.462 0.483	0.789 0.809	1.107 1.094	1.404 1.350	1.718 1.613

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN9x is a family of AND-NOR circuits consisting of one 3-input AND gate, one 2-input AND gate, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	X	L
X	X	X	X	X	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN9x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN9x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN92	AN94	AN96
A	1.1	1.0	1.8
B	1.1	1.0	1.8
C	1.0	1.1	1.8
D	1.0	1.1	1.9
E	1.0	1.1	1.8
F	0.9	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN92	4.0	1.592	9.5
AN94	4.2	1.760	11.0
AN96	4.8	3.324	18.2

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

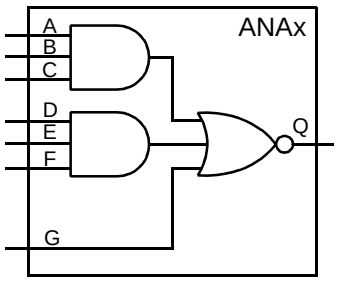
AN92	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.630 0.703	0.948 1.023	1.317 1.382	1.741 1.789	2.085 2.115
AN94	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.662 0.713	1.010 1.061	1.353 1.391	1.645 1.667	1.958 1.961
AN96	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.507 0.532	0.826 0.860	1.140 1.135	1.436 1.382	1.748 1.646

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANAx is a family of AND-NOR circuits consisting of two 3-input AND gates, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	H	X	L
X	X	X	X	X	X	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANAx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANA2	ANA4	ANA6
A	1.0	1.0	1.9
B	1.0	1.1	1.9
C	1.0	1.0	1.9
D	1.1	1.1	2.0
E	1.1	1.1	2.0
F	1.1	1.1	1.9
G	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANA2	4.2	1.706	10.3
ANA4	4.0	1.863	11.4
ANA6	4.8	3.538	19.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

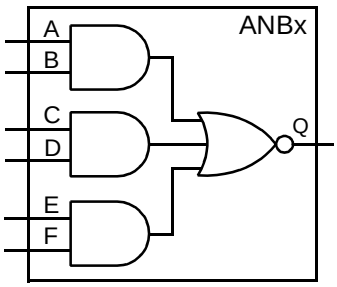
ANA2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.656 0.725	0.957 1.033	1.324 1.393	1.756 1.811	2.113 2.150
ANA4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.645 0.698	0.983 1.039	1.329 1.365	1.630 1.640	1.956 1.932
ANA6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.513 0.543	0.851 0.861	1.145 1.149	1.441 1.405	1.755 1.664

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANBx is a family of AND-NOR circuits consisting of three 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	X	X	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... ANBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ANBx port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ANB2	ANB4	ANB6
A	1.1	1.0	1.8
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.1	1.9
F	0.9	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANB2	3.8	1.599	9.1
ANB4	4.2	1.779	10.8
ANB6	4.8	3.357	18.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

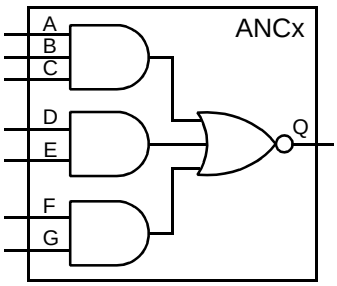
ANB2	Number of Equivalent Loads		1	5	10	16	21 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.589 0.630	0.896 0.948	1.260 1.307	1.686 1.715	2.036 2.043
ANB4	Number of Equivalent Loads		1	10	20	29	39 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.604 0.658	0.949 0.984	1.298 1.294	1.598 1.569	1.923 1.881
ANB6	Number of Equivalent Loads		1	19	38	56	75 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.471 0.501	0.782 0.830	1.095 1.115	1.388 1.379	1.696 1.662

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANCx is a family of AND-NOR circuits consisting of one 3-input AND gate and two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	X	X	L
X	X	X	X	X	H	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANC2	ANC4	ANC6
A	1.0	1.0	1.8
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.9
G	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANC2	4.2	1.726	9.7
ANC4	4.2	1.886	11.1
ANC6	5.0	3.581	19.0

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

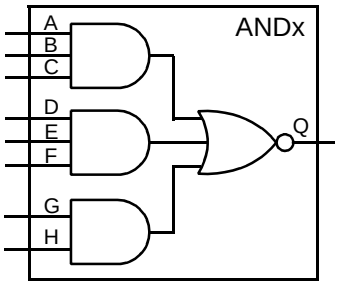
ANC2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.634 0.711	0.952 1.024	1.321 1.384	1.746 1.795	2.091 2.128
ANC4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.646 0.693	0.978 1.032	1.325 1.358	1.628 1.635	1.959 1.929
ANC6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.494 0.537	0.828 0.862	1.150 1.164	1.452 1.439	1.771 1.727

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANDx is a family of AND-NOR circuits consisting of two 3-input AND gates and one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
H	H	H	X	X	X	X	X	L
X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	H	H	L
All other combinations								H

HDL Syntax

Verilog ..... ANDx *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: ANDx port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads		
	AND2	AND4	AND6
A	1.1	1.0	1.8
B	1.1	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.1	2.0
E	1.0	1.1	1.9
F	1.0	1.1	1.9
G	1.0	1.0	2.0
H	1.1	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AND2	4.5	1.842	10.4
AND4	4.5	2.004	11.5
AND6	5.0	3.799	19.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

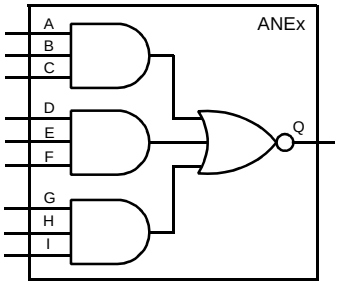
AND2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.648 0.716	0.948 1.023	1.314 1.387	1.748 1.805	2.106 2.138
AND4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.655 0.700	0.983 1.029	1.325 1.360	1.624 1.645	1.949 1.953
AND6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.476 0.568	0.815 0.866	1.138 1.148	1.424 1.419	1.712 1.707

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANEx is a family of AND-NOR circuits consisting of three 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L
All other combinations									H

HDL Syntax

Verilog ..... ANEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ANEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ANE2	ANE4	ANE6
A	1.1	1.0	1.8
B	1.1	1.0	1.8
C	1.0	1.1	1.8
D	1.1	1.1	1.9
E	1.1	1.1	1.9
F	1.1	1.1	1.9
G	1.1	1.1	1.9
H	1.1	1.1	1.9
I	1.0	1.1	1.9

AMI500MXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANE2	5.0	1.971	11.0
ANE4	5.2	2.141	12.6
ANE6	5.8	4.040	20.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

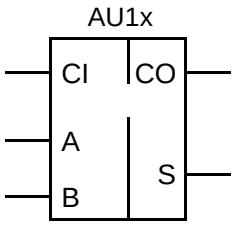
ANE2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.639 0.711	0.945 1.018	1.311 1.378	1.740 1.794	2.093 2.134
ANE4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.685 0.735	1.028 1.076	1.387 1.407	1.701 1.687	2.044 1.986
ANE6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.489 0.552	0.822 0.871	1.152 1.173	1.452 1.441	1.759 1.712

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AU1x is a family of combinational one-bit full adders.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

HDL Syntax

Verilog ..... AU1x *inst_name* (CO, S, A, B, CI);

VHDL..... *inst_name*: AU1x port map (CO, S, A, B, CI);

Pin Loading

Pin Name	Equivalent Loads	
	AU11	AU12
A	4.9	8.4
B	4.8	8.4
CI	3.7	6.5

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AU11	4.8	1.960	10.6
AU12	5.2	3.546	18.2

a. See page 2-13 for power equation.

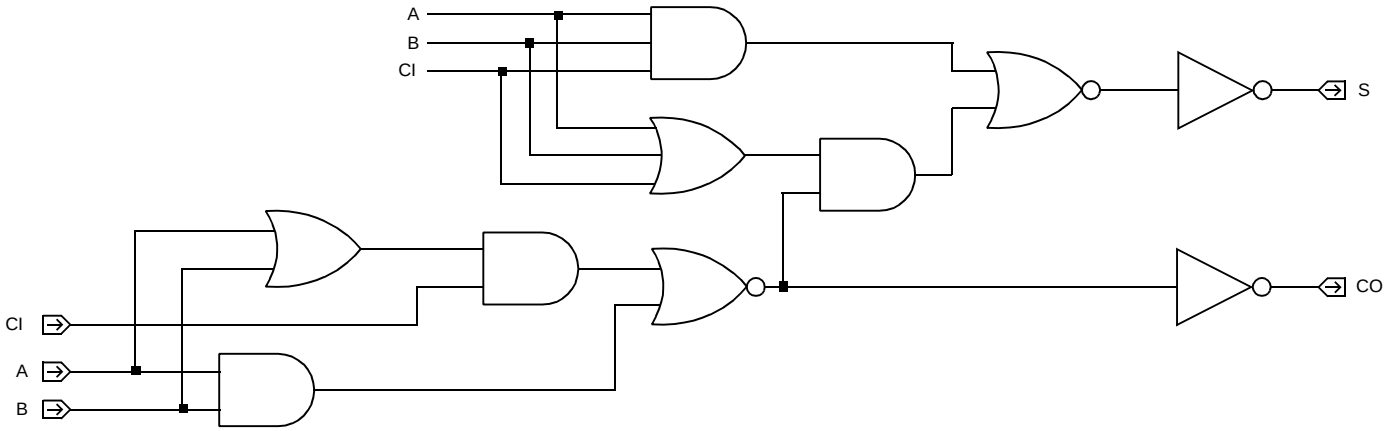
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
AU11	From: A To: S	t_{PLH} t_{PHL}	0.627 1.221	0.931 1.600	1.281 1.985	1.695 2.397	2.050 2.715
	From: B To: S	t_{PLH} t_{PHL}	0.587 1.328	0.888 1.695	1.251 2.087	1.676 2.518	2.025 2.858
	From: CI To: S	t_{PLH} t_{PHL}	0.579 1.323	0.907 1.691	1.279 2.082	1.701 2.510	2.040 2.846
	From: A To: CO	t_{PLH} t_{PHL}	0.574 0.853	0.878 1.244	1.248 1.648	1.687 2.083	2.049 2.421
	From: B To: CO	t_{PLH} t_{PHL}	0.580 0.814	0.898 1.216	1.266 1.619	1.688 2.045	2.030 2.373
	From: CI To: CO	t_{PLH} t_{PHL}	0.572 0.696	0.894 1.071	1.265 1.467	1.691 1.898	2.043 2.236
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
AU12	From: A To: S	t_{PLH} t_{PHL}	0.489 0.923	0.822 1.314	1.153 1.651	1.448 1.921	1.785 2.214
	From: B To: S	t_{PLH} t_{PHL}	0.453 0.993	0.779 1.376	1.111 1.723	1.404 2.008	1.727 2.306
	From: CI To: S	t_{PLH} t_{PHL}	0.446 0.977	0.785 1.350	1.136 1.707	1.442 2.009	1.775 2.331
	From: A To: CO	t_{PLH} t_{PHL}	0.482 0.571	0.794 0.979	1.142 1.330	1.454 1.612	1.801 1.903
	From: B To: CO	t_{PLH} t_{PHL}	0.455 0.568	0.801 0.962	1.149 1.301	1.455 1.581	1.793 1.880
	From: CI To: CO	t_{PLH} t_{PHL}	0.440 0.420	0.760 0.797	1.101 1.137	1.409 1.417	1.749 1.712

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic

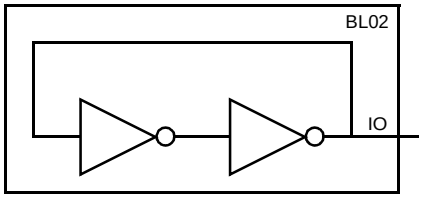


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

BL02 is a tristate bus latch that stores the final binary level on the bus when left undriven.

Logic Symbol



Truth Table

N/A

Pin Loading

	Equivalent Load
IO	1.5

Equivalent Gates 2.5

HDL Syntax

Verilog ..... BL02 *inst_name* (IO);

VHDL..... *inst_name*: BL02 port map (IO);

Size And Power Characteristics

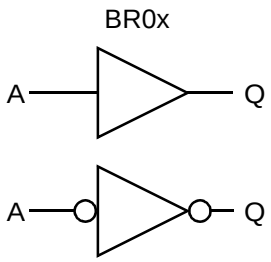
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.415	nA
EQL_{pd}	7.2	Eq-load

See page 2-13 for power equation.

Description

BR0x is a family of non-inverting bus receivers with a single output to be used as the output of tristate busses.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... BR0x *inst_name* (Q, A);

VHDL..... *inst_name*: BR0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	BR02	BR04	BR06
A	1.0	2.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
BR02	1.0	0.585	3.4
BR04	1.5	1.106	5.7
BR06	2.0	1.484	8.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

BR02	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.293 0.300	0.605 0.605	0.945 0.907	1.251 1.174	1.590 1.473
BR04	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.239 0.210	0.512 0.462	0.809 0.768	1.100 1.037	1.412 1.283
BR06	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.264 0.277	0.566 0.567	0.874 0.834	1.185 1.090	1.496 1.318

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

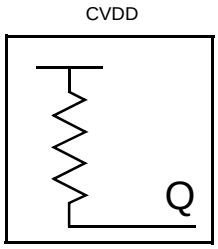
CVDD is the resistive tie-up to the core V_{DD} bus for all cell inputs.

Equivalent Gates 1.0

HDL Syntax

Verilog ..... CVDD *inst_name* (Q);

VHDL..... *inst_name*: CVDD port map (Q);



CVSS

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

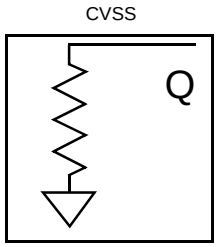
CVSS is the resistive tie-down to the core V_{SS} bus for all cell inputs.

Equivalent Gates 1.0

HDL Syntax

Verilog ..... CVSS *inst_name* (Q);

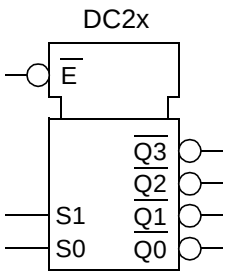
VHDL..... *inst_name*: CVSS port map (Q);



Description

DC2x is a family of two-to-four line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

HDL Syntax

Verilog ..... DC2x *inst_name* (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

VHDL..... *inst_name*: DC2x port map (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

Pin Loading

Pin Name	Equivalent Loads	
	DC21	DC22
S0	3.4	3.5
S1	3.4	3.5
EN	1.0	4.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC21	5.5	2.318	16.3
DC22	7.2	3.252	18.2

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

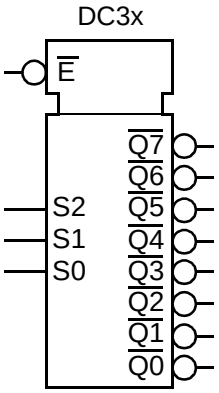
	Number of Equivalent Loads		1	2	4	6	8 (max)
DC21	From: Sx To: QN	t_{PLH} t_{PHL}	0.444 0.488	0.546 0.619	0.739 0.879	0.924 1.137	1.103 1.396
	From: EN To: QN	t_{PLH} t_{PHL}	0.626 0.637	0.713 0.779	0.899 1.047	1.095 1.303	1.297 1.553
	Number of Equivalent Loads		**1**	**5**	**10**	**16**	**21 (max)**
DC22	From: Sx To: QN	t_{PLH} t_{PHL}	0.380 0.592	0.670 0.945	1.026 1.329	1.460 1.755	1.828 2.093
	From: EN To: QN	t_{PLH} t_{PHL}	0.399 0.667	0.701 1.026	1.068 1.401	1.500 1.819	1.855 2.156

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

DC3x is a family of three-to-eight line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... DC3x *inst_name* (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

VHDL..... *inst_name* DC3x port map (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads	
	DC31	DC32
S0	6.1	6.6
S1	6.5	6.7
S2	5.7	5.8
EN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC31	12.3	5.021	40.3
DC32	17.0	7.616	58.5

a. See page 2-13 for power equation.

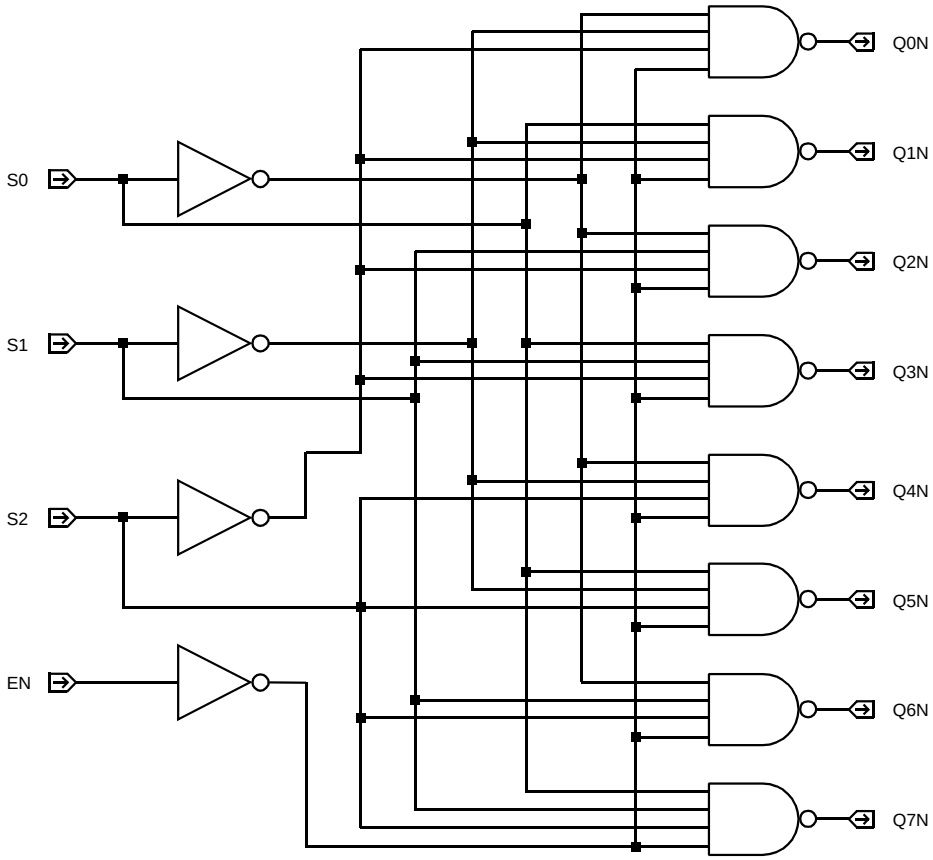
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	4	5	7 (max)
DC31	From: Sx To: QN	t_{PLH} t_{PHL}	0.570 0.685	0.684 0.854	0.909 1.169	1.021 1.319	1.244 1.611
	From: EN To: QN	t_{PLH} t_{PHL}	0.981 0.959	1.096 1.125	1.312 1.444	1.416 1.599	1.618 1.906
	Number of Equivalent Loads		**1**	**5**	**10**	**16**	**21 (max)**
DC32	From: Sx To: QN	t_{PLH} t_{PHL}	0.401 0.630	0.689 1.030	1.049 1.447	1.481 1.900	1.840 2.253
	From: EN To: QN	t_{PLH} t_{PHL}	1.328 1.362	1.619 1.778	1.980 2.180	2.413 2.598	2.772 2.915

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

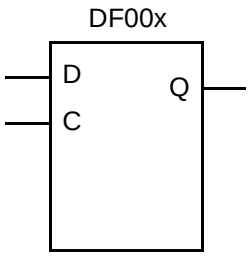
Logic Schematic



Description

DF00x is a family of static, master-slave D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q
H	↑	H
L	↑	L
X	L	NC

NC = No Change

HDL Syntax

Verilog ..... DF00x *inst_name* (Q, C, D);

VHDL..... *inst_name*: DF00x port map (Q, C, D);

Pin Loading

Pin Name	Equivalent Loads	
	DF001	DF002
D	1.1	1.1
C	1.1	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF001	4.0	1.419	8.1
DF002	4.0	1.594	9.5

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

DF001	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.884 0.728	1.196 1.038	1.560 1.401	1.979 1.820	2.319 2.161
DF002	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.850 0.713	1.149 1.070	1.490 1.399	1.802 1.673	2.151 1.962

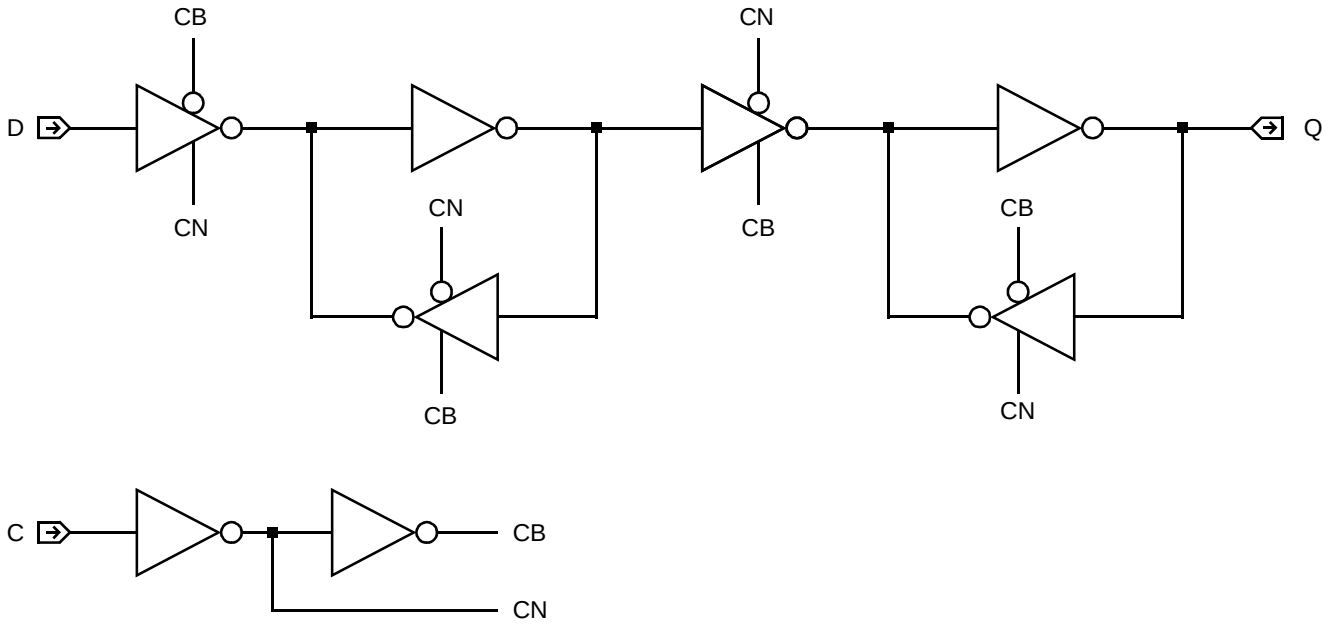
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF001	Cell DF002
Min C Width	High	t_w	0.858	0.859
Min C Width	Low	t_w	0.945	0.907
Min D Setup		t_{su}	0.530	0.535
Min D Hold		t_h	0.273	0.247

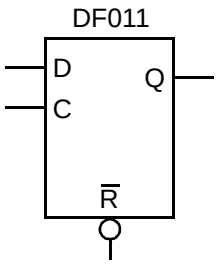
Logic Schematic



Description

DF011 is a static, master-slave D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q
L	X	X	L
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.1
C	1.1
RN	1.1

Equivalent Gates 5.2

HDL Syntax

Verilog ..... DF011 *inst_name* (Q, C, D, RN);

VHDL..... *inst_name*: DF011 port map (Q, C, D, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.028	nA
EQL_{pd}	12.9	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	1.038 0.816	1.273 0.990	1.635 1.238	1.881 1.398	2.253 1.633
RN	Q	t_{PHL}	0.538	0.692	0.910	1.061	1.284

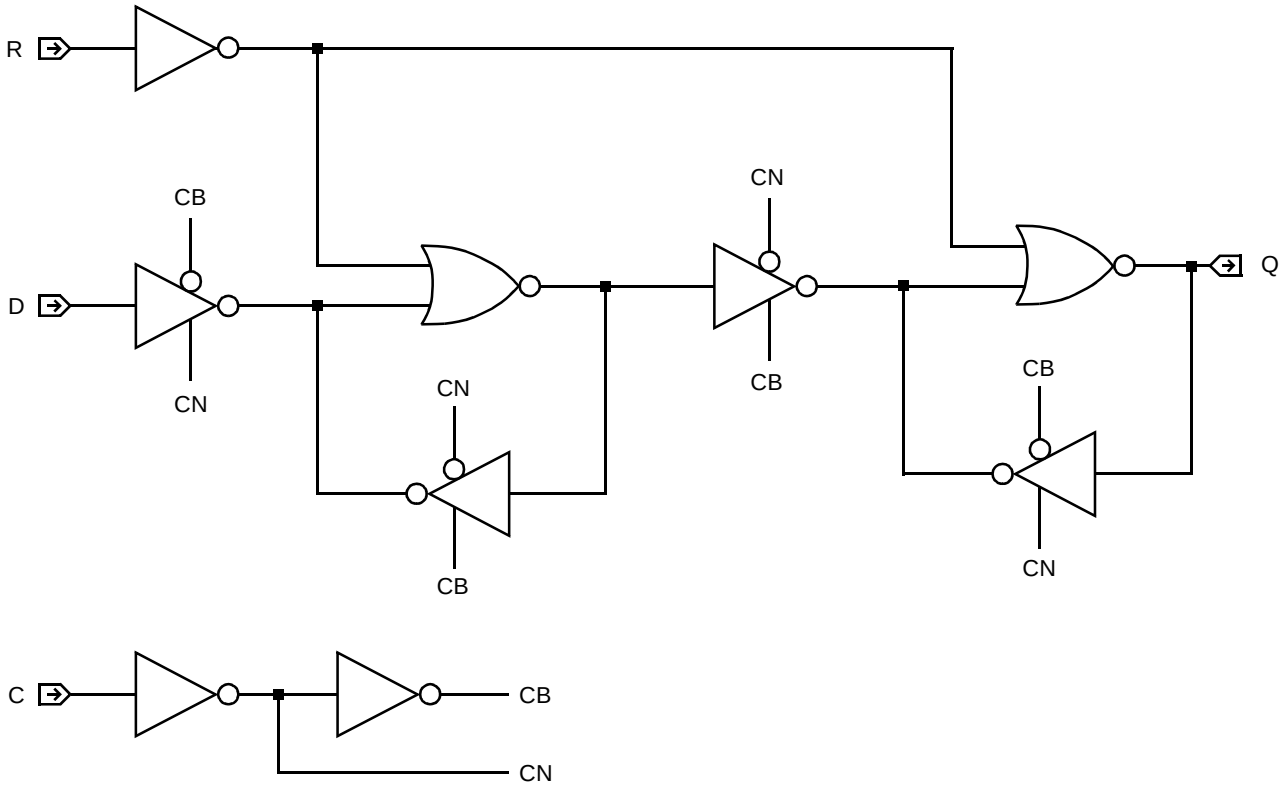
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	1.037
Min C Width	Low	t_w	0.994
Min RN Width	Low	t_w	1.043
Min D Setup		t_{su}	0.580
Min D Hold		t_h	0.265
Min RN Setup		t_{su}	0.467
Min RN Hold		t_h	0.649

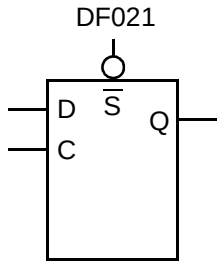
Logic Schematic



Description

DF021 is a static, master-slave D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q
L	X	X	H
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	1.1
SN	2.2

Equivalent Gates 4.8

HDL Syntax

Verilog.....DF021 *inst_name* (Q, C, D, SN);

VHDL..... *inst_name*: DF021 port map (Q, C, D, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.723	nA
EQL_{pd}	9.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	0.968 0.824	1.128 1.045	1.384 1.359	1.560 1.561	1.830 1.859
SN	Q	t_{PLH}	0.326	0.473	0.686	0.849	1.098

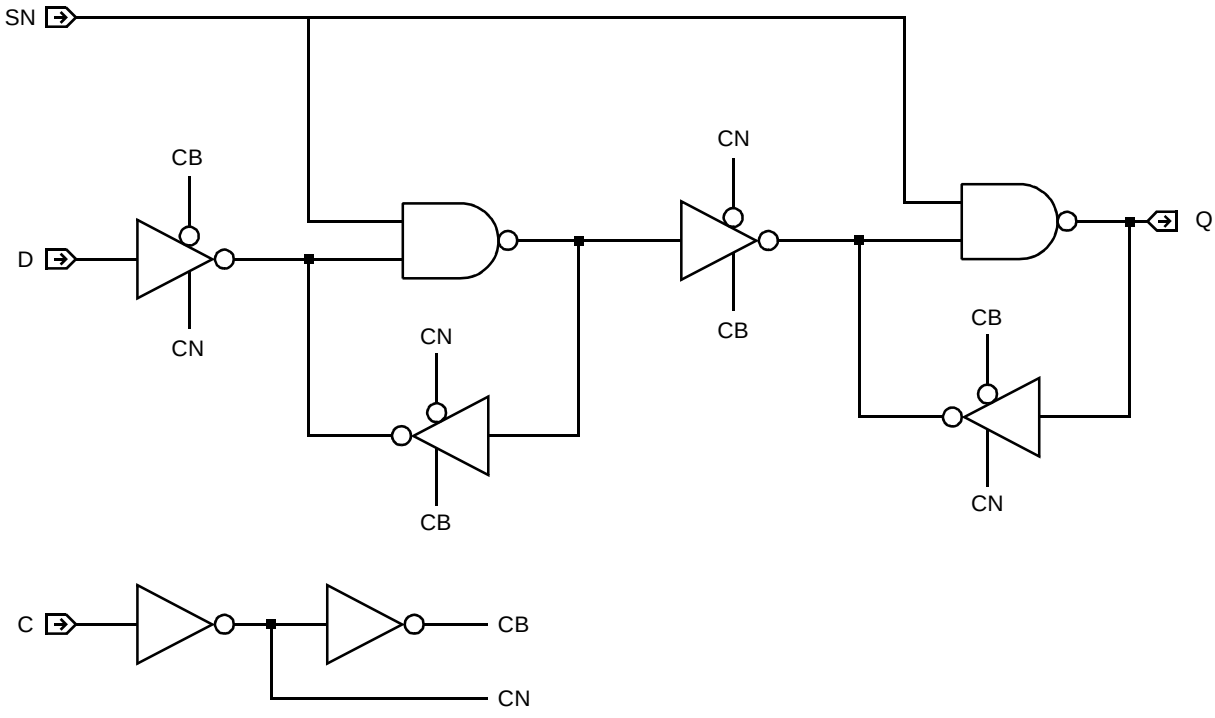
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.971
Min C Width	Low	t_w	0.975
Min SN Width	Low	t_w	0.737
Min D Setup		t_{su}	0.565
Min D Hold		t_h	0.258
Min SN Setup		t_{su}	0.259
Min SN Hold		t_h	0.856

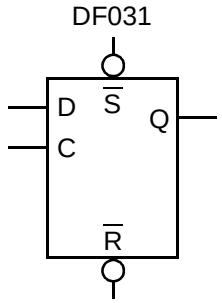
Logic Schematic



Description

DF031 is a static, master-slave D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	L	↑	L
H	H	H	↑	H
H	H	X	L	NC

NC = No Change
IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
C	1.1
SN	2.2
RN	1.0

Equivalent Gates 6.0

HDL Syntax

Verilog ..... DF031 *inst_name* (Q, D, RN, SN);

VHDL..... *inst_name*: DF031 port map (Q, D, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.937	nA
EQL_{pd}	13.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	1.049 0.820	1.356 1.051	1.798 1.392	2.087 1.617	2.513 1.953
RN	Q	t_{PHL}	0.566	0.793	1.127	1.348	1.681
SN	Q	t_{PLH}	0.285	0.427	0.607	0.748	0.964

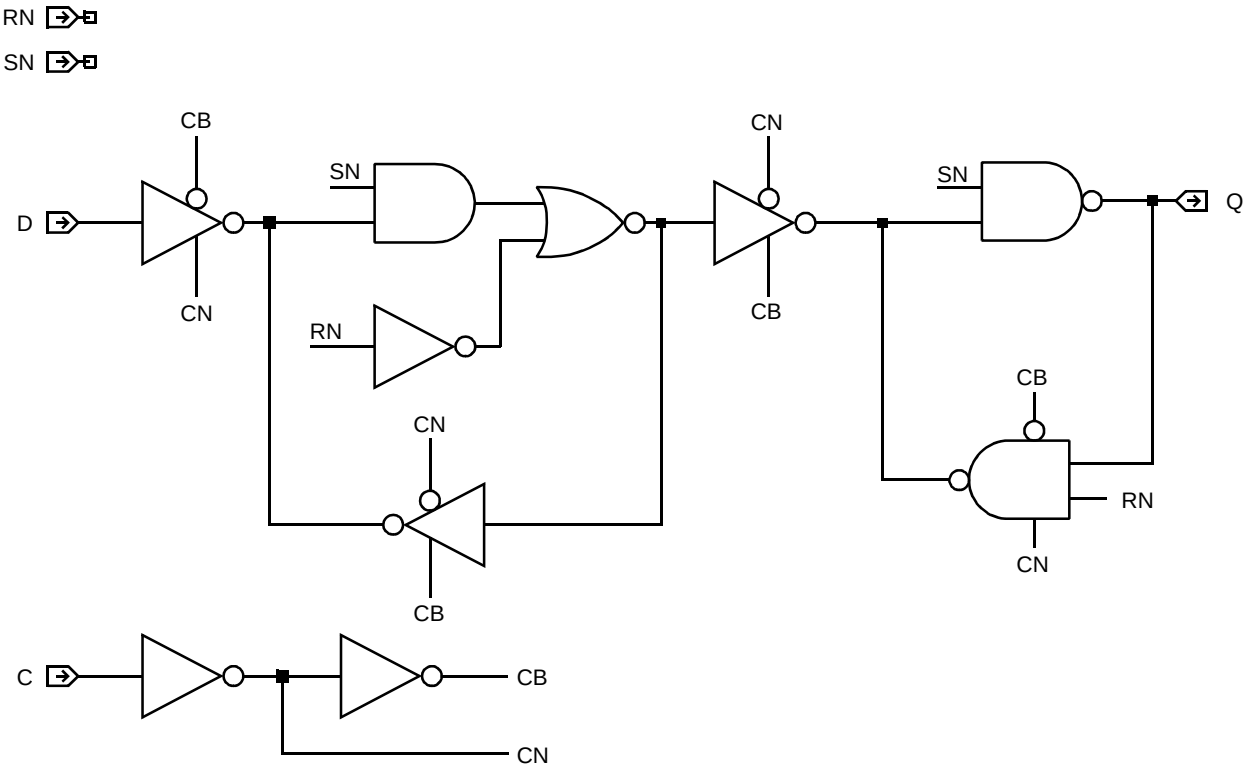
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	1.050
Min C Width	Low	t_w	1.032
Min RN Width	Low	t_w	1.056
Min SN Width	Low	t_w	0.772
Min D Setup		t_{su}	0.618
Min D Hold		t_h	0.269
Min RN Setup		t_{su}	0.536
Min RN Hold		t_h	0.636
Min SN Setup		t_{su}	0.311
Min SN Hold		t_h	0.881

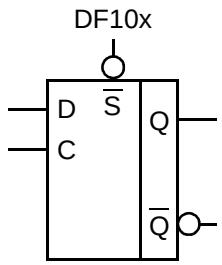
Logic Schematic



Description

DF10x is a family of static, master-slave D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF10x *inst_name* (Q, QN, C, D, SN);

VHDL..... *inst_name*: DF10x port map (Q, QN, C, D, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF101	DF102	DF104	DF106
D	1.0	1.0	1.1	1.0
C	1.1	1.1	1.1	1.1
SN	2.4	2.2	3.5	3.4

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
DF101	5.8	2.005	12.6
DF102	5.5	2.317	14.5
DF104	7.0	3.561	24.5
DF106	7.8	4.226	29.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF101	From: C To: Q	t_{PLH} t_{PHL}	0.926 0.816	1.221 1.177	1.586 1.562	2.021 1.986	2.383 2.320
	From: C To: QN	t_{PLH} t_{PHL}	1.059 1.201	1.342 1.488	1.700 1.846	2.132 2.274	2.494 2.629
	From: SN To: Q	t_{PLH}	1.133	1.450	1.822	2.252	2.602
	From: SN To: QN	t_{PHL}	0.482	0.806	1.149	1.561	1.912
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF102	From: C To: Q	t_{PLH} t_{PHL}	0.939 0.766	1.271 1.152	1.595 1.516	1.892 1.820	2.251 2.143
	From: C To: QN	t_{PLH} t_{PHL}	1.166 1.251	1.455 1.560	1.773 1.868	2.058 2.133	2.373 2.417
	From: SN To: Q	t_{PLH}	1.288	1.622	1.957	2.244	2.553
	From: SN To: QN	t_{PHL}	0.437	0.794	1.107	1.373	1.672
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF104	From: C To: Q	t_{PLH} t_{PHL}	0.980 0.777	1.284 1.194	1.604 1.514	1.906 1.779	2.225 2.037
	From: C To: QN	t_{PLH} t_{PHL}	1.085 1.240	1.327 1.528	1.632 1.810	1.943 2.067	2.289 2.332
	From: SN To: Q	t_{PLH}	1.031	1.382	1.712	2.012	2.323
	From: SN To: QN	t_{PHL}	0.328	0.663	0.919	1.169	1.440
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF106	From: C To: Q	t_{PLH} t_{PHL}	1.019 0.787	1.355 1.207	1.686 1.518	2.010 1.793	2.332 2.047
	From: C To: QN	t_{PLH} t_{PHL}	1.240 1.335	1.467 1.687	1.759 1.971	2.077 2.228	2.413 2.469
	From: SN To: Q	t_{PLH}	1.270	1.590	1.904	2.212	2.515
	From: SN To: QN	t_{PHL}	0.389	0.753	0.973	1.233	1.493

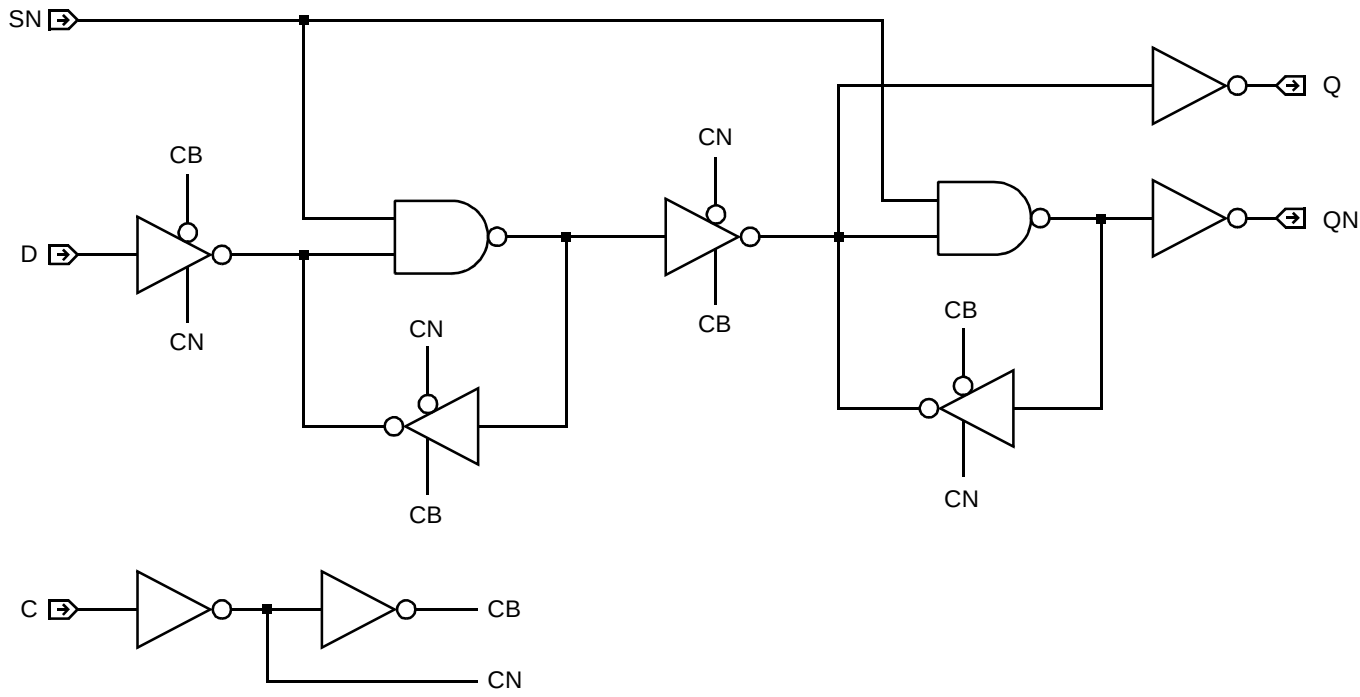
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF101	DF102	DF104	DF106
Min C Width	High	t_w	0.959	1.047	1.108	1.217
Min C Width	Low	t_w	0.989	0.960	1.132	1.123
Min SN Width		t_w	0.918	1.070	0.891	1.063
Min D Setup		t_{su}	0.588	0.563	0.657	0.649
Min D Hold		t_h	0.268	0.256	0.285	0.285
Min SN Setup		t_{su}	0.276	0.258	0.335	0.337
Min SN Hold		t_h	0.844	0.842	0.940	0.922

Logic Schematic

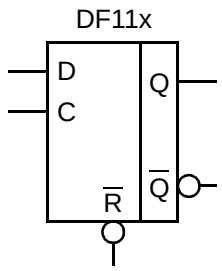


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DF11x is a family of static, master-slave D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF11x *inst_name* (Q, QN, C, D, RN);

VHDL.....inst_DF11x : DF11x port map (Q, QN, C, D, RN);

Pin Loading

Pin Name	Equivalent Loads			
	DF111	DF112	DF114	DF116
D	1.0	1.0	1.0	1.0
C	1.0	1.1	1.0	1.0
RN	1.0	1.1	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF111	6.2	2.335	15.0
DF112	6.0	2.676	17.8
DF114	7.8	3.991	27.1
DF116	8.5	4.720	32.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF111	From: C To: Q	t_{PLH} t_{PHL}	0.898 0.817	1.225 1.176	1.592 1.563	2.008 1.992	2.341 2.331
	From: C To: QN	t_{PLH} t_{PHL}	0.998 1.250	1.270 1.582	1.642 1.954	2.083 2.376	2.422 2.714
	From: RN To: Q	t_{PHL}	1.707	2.176	2.615	3.064	3.401
	From: RN To: QN	t_{PLH}	0.596	0.887	1.245	1.673	2.031
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF112	From: C To: Q	t_{PLH} t_{PHL}	0.936 0.791	1.238 1.213	1.570 1.567	1.867 1.849	2.195 2.138
	From: C To: QN	t_{PLH} t_{PHL}	1.150 1.354	1.446 1.672	1.759 1.999	2.034 2.283	2.335 2.593
	From: RN To: Q	t_{PHL}	1.804	2.361	2.750	3.038	3.320
	From: RN To: QN	t_{PLH}	0.606	0.913	1.248	1.546	1.881
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF114	From: C To: Q	t_{PLH} t_{PHL}	0.977 0.730	1.265 1.135	1.590 1.467	1.906 1.750	2.245 2.026
	From: C To: QN	t_{PLH} t_{PHL}	0.993 1.283	1.247 1.648	1.548 1.926	1.849 2.153	2.184 2.374
	From: RN To: Q	t_{PHL}	1.418	1.884	2.248	2.554	2.852
	From: RN To: QN	t_{PLH}	0.576	0.885	1.191	1.480	1.787
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF116	From: C To: Q	t_{PLH} t_{PHL}	0.998 0.763	1.357 1.252	1.671 1.551	1.957 1.823	2.225 2.097
	From: C To: QN	t_{PLH} t_{PHL}	1.150 1.443	1.388 1.793	1.684 2.077	2.000 2.334	2.331 2.575
	From: RN To: Q	t_{PHL}	1.602	2.167	2.501	2.771	3.007
	From: RN To: QN	t_{PLH}	0.593	0.908	1.210	1.502	1.789

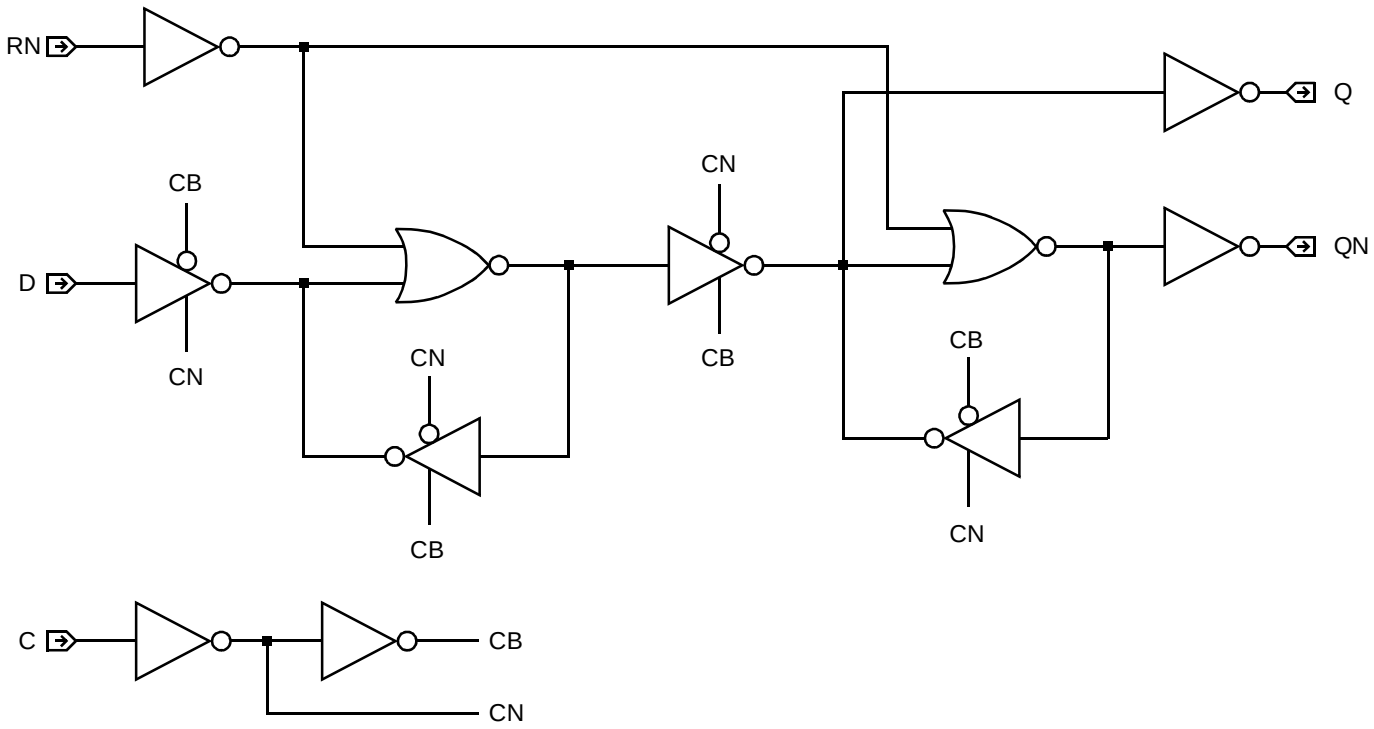
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF111	DF112	DF114	DF116
Min C Width	High	t_w	0.974	1.105	1.140	1.271
Min C Width	Low	t_w	0.933	0.941	1.081	1.081
Min RN Width		t_w	0.993	0.995	1.116	1.115
Min D Setup		t_{su}	0.563	0.560	0.622	0.622
Min D Hold		t_h	0.248	0.255	0.279	0.279
Min RN Setup		t_{su}	0.457	0.462	0.574	0.574
Min RN Hold		t_h	0.595	0.600	0.645	0.645

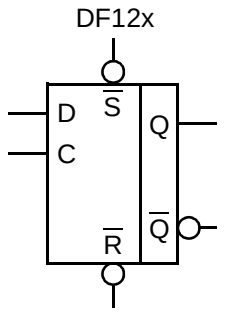
Logic Schematic



Description

DF12x is a family of static, master-slave D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DF12x *inst_name* (Q, QN, C, D, RN, SN);

VHDL..... *inst_name*: DF12x port map (Q, QN, C, D, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF121	DF122	DF124	DF126
D	1.0	1.0	1.0	1.0
C	1.1	1.1	1.1	1.1
SN	2.2	2.3	2.4	2.2
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF121	7.0	2.305	16.5
DF122	7.0	2.630	19.0
DF124	8.0	3.613	26.9
DF126	9.0	4.304	32.3

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF121	From: C To: Q	t_{PLH} t_{PHL}	0.923 0.827	1.239 1.202	1.608 1.589	2.033 2.008	2.379 2.333
	From: C To: QN	t_{PLH} t_{PHL}	1.095 1.383	1.368 1.717	1.726 2.100	2.168 2.539	2.543 2.893
	From: SN To: Q	t_{PLH}	1.139	1.453	1.828	2.266	2.626
	From: SN To: QN	t_{PHL}	0.464	0.779	1.142	1.561	1.905
	From: RN To: Q	t_{PHL}	1.750	2.208	2.653	3.117	3.471
	From: RN To: QN	t_{PLH}	0.662	0.955	1.323	1.765	2.136
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF122	From: C To: Q	t_{PLH} t_{PHL}	0.955 0.795	1.277 1.220	1.612 1.587	1.904 1.884	2.222 2.191
	From: C To: QN	t_{PLH} t_{PHL}	1.228 1.470	1.523 1.839	1.846 2.180	2.134 2.462	2.454 2.760
	From: SN To: Q	t_{PLH}	1.324	1.676	2.014	2.299	2.603
	From: SN To: QN	t_{PHL}	0.420	0.772	1.092	1.366	1.673
	From: RN To: Q	t_{PHL}	1.884	2.409	2.831	3.161	3.495
	From: RN To: QN	t_{PLH}	0.660	0.999	1.346	1.652	1.999

	Number of Equivalent Loads		1	19	38	56	75 (max)
DF124	From: C To: Q	t_{PLH} t_{PHL}	1.562 1.276	1.905 1.629	2.221 1.941	2.494 2.234	2.763 2.550
	From: C To: QN	t_{PLH} t_{PHL}	1.148 1.185	1.439 1.507	1.763 1.817	2.066 2.098	2.378 2.385
	From: SN To: Q	t_{PLH}	0.632	0.936	1.239	1.541	1.859
	From: SN To: QN	t_{PHL}	1.386	1.807	2.056	2.322	2.638
	From: RN To: Q	t_{PHL}	0.885	1.234	1.532	1.814	2.095
	From: RN To: QN	t_{PLH}	2.030	2.295	2.586	2.866	3.164
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF126	From: C To: Q	t_{PLH} t_{PHL}	1.721 1.435	2.015 1.779	2.324 2.040	2.635 2.292	2.947 2.554
	From: C To: QN	t_{PLH} t_{PHL}	0.844 1.273	1.376 1.628	1.727 1.919	2.021 2.181	2.301 2.426
	From: SN To: Q	t_{PLH}	0.724	1.040	1.368	1.691	2.011
	From: SN To: QN	t_{PHL}	1.493	1.905	2.198	2.449	2.678
	From: RN To: Q	t_{PHL}	0.974	1.355	1.602	1.849	2.146
	From: RN To: QN	t_{PLH}	2.180	2.439	2.733	3.039	3.353

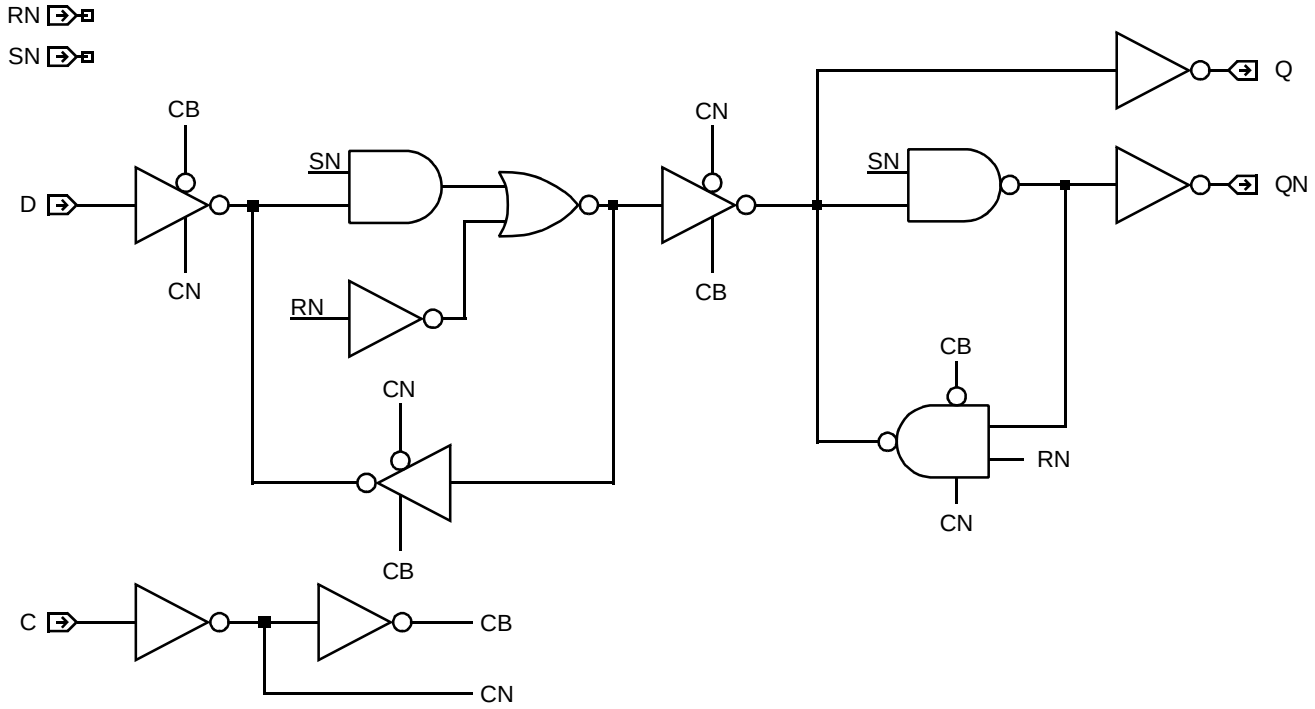
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF121	DF122	DF124	DF126
Min C Width	High	t_w	1.074	1.203	1.078	1.106
Min C Width	Low	t_w	1.003	1.008	1.005	1.012
Min RN Width	Low	t_w	1.021	1.024	1.029	1.035
Min SN Width	Low	t_w	0.923	1.115	0.950	0.957
Min D Setup		t_{su}	0.598	0.599	0.612	0.602
Min D Hold		t_h	0.268	0.268	0.262	0.271
Min RN Setup		t_{su}	0.522	0.525	0.550	0.530
Min RN Hold		t_h	0.620	0.620	0.600	0.624
Min SN Setup		t_{su}	0.305	0.307	0.327	0.306
Min SN Hold		t_h	0.854	0.858	0.831	0.861

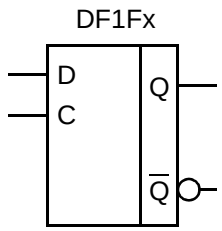
Logic Schematic



Description

DF1Fx is a family of static, master-slave D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
X	X	L	H
L	↑	L	H
H	↑	H	L
X	L	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF1Fx *inst_name* (Q, QN, C, D);

VHDL..... *inst_name*: DF1Fx port map (Q, QN, C, D)

Pin Loading

Pin Name	Equivalent Loads			
	DF1F1	DF1F2	DF1F4	DF1F6
D	1.1	1.1	1.0	1.0
C	1.1	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF1F1	5.2	1.823	11.9
DF1F2	5.0	2.161	13.7
DF1F4	6.0	3.215	20.9
DF1F6	6.8	4.131	28.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF1F1	From: C To: Q	t_{PLH} t_{PHL}	0.890 0.813	1.196 1.166	1.562 1.560	1.991 2.005	2.342 2.361
	From: C To: QN	t_{PLH} t_{PHL}	0.970 1.143	1.249 1.415	1.603 1.767	2.031 2.197	2.390 2.559
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF1F2	From: C To: Q	t_{PLH} t_{PHL}	0.887 0.784	1.198 1.180	1.554 1.520	1.878 1.805	2.242 2.117
	From: C To: QN	t_{PLH} t_{PHL}	1.087 1.127	1.344 1.460	1.660 1.774	1.959 2.037	2.300 2.315
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF1F4	From: C To: Q	t_{PLH} t_{PHL}	1.293 1.112	1.561 1.461	1.848 1.765	2.139 2.030	2.483 2.296
	From: C To: QN	t_{PLH} t_{PHL}	0.871 0.986	1.144 1.270	1.454 1.568	1.758 1.850	2.086 2.146
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF1F6	From: C To: Q	t_{PLH} t_{PHL}	1.299 1.117	1.569 1.445	1.878 1.725	2.201 2.002	2.534 2.288
	From: C To: QN	t_{PLH} t_{PHL}	0.897 1.071	1.193 1.425	1.520 1.691	1.847 1.965	2.173 2.253

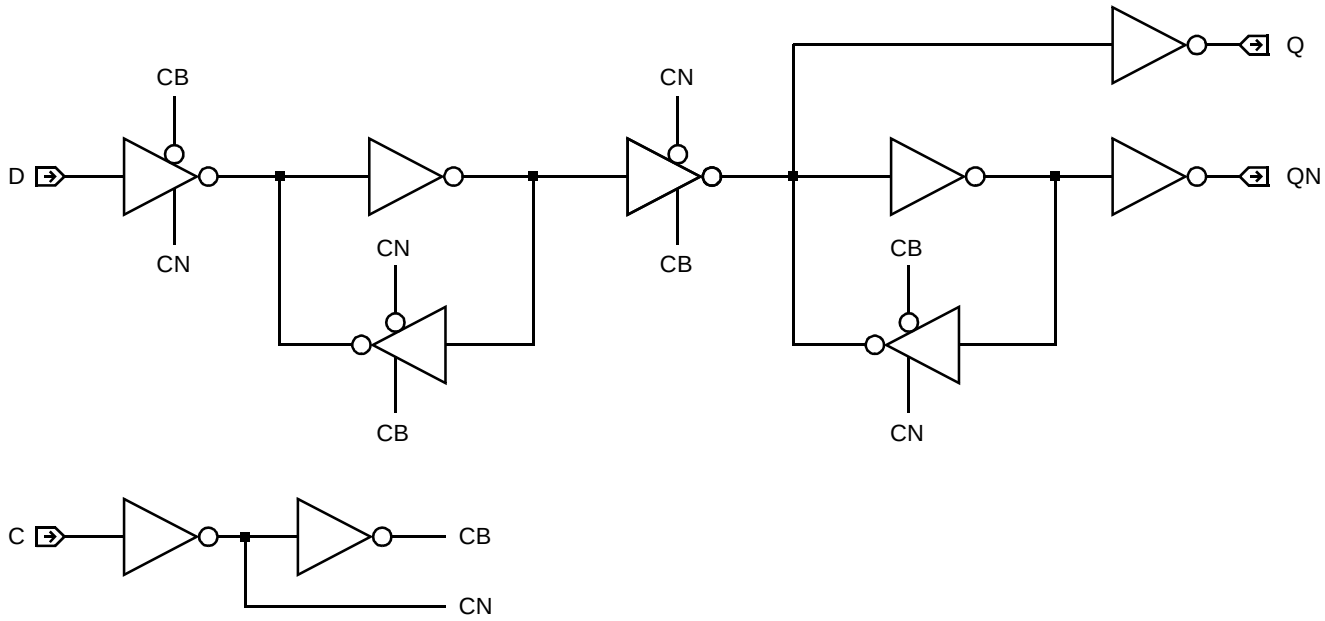
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF1F1	DF1F2	DF1F4	DF1F6
Min C Width	High	t_w	0.914	0.968	0.882	0.933
Min C Width	Low	t_w	0.918	0.890	0.897	0.883
Min D Setup		t_{su}	0.535	0.523	0.537	0.532
Min D Hold		t_h	0.255	0.251	0.248	0.247

Logic Schematic

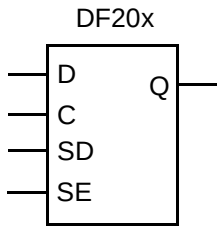


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DF20x is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q
↑	H	X	L	H
↑	L	X	L	L
↑	X	H	H	H
↑	X	L	H	L
L	X	X	X	NC

NC = No Change

HDL Syntax

Verilog ..... DF20x *inst_name* (Q, C, D, SD, SE);

VHDL..... *inst_name*: DF20x port map (Q, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads	
	DF201	DF202
C	1.0	1.0
D	1.0	1.0
SD	1.0	1.0
SE	2.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF201	5.2	2.000	13.4
DF202	5.2	2.010	13.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

DF201	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.935 0.783	1.220 1.082	1.581 1.442	2.016 1.867	2.380 2.216
DF202	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.846 0.725	1.149 1.072	1.503 1.404	1.829 1.684	2.197 1.982

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

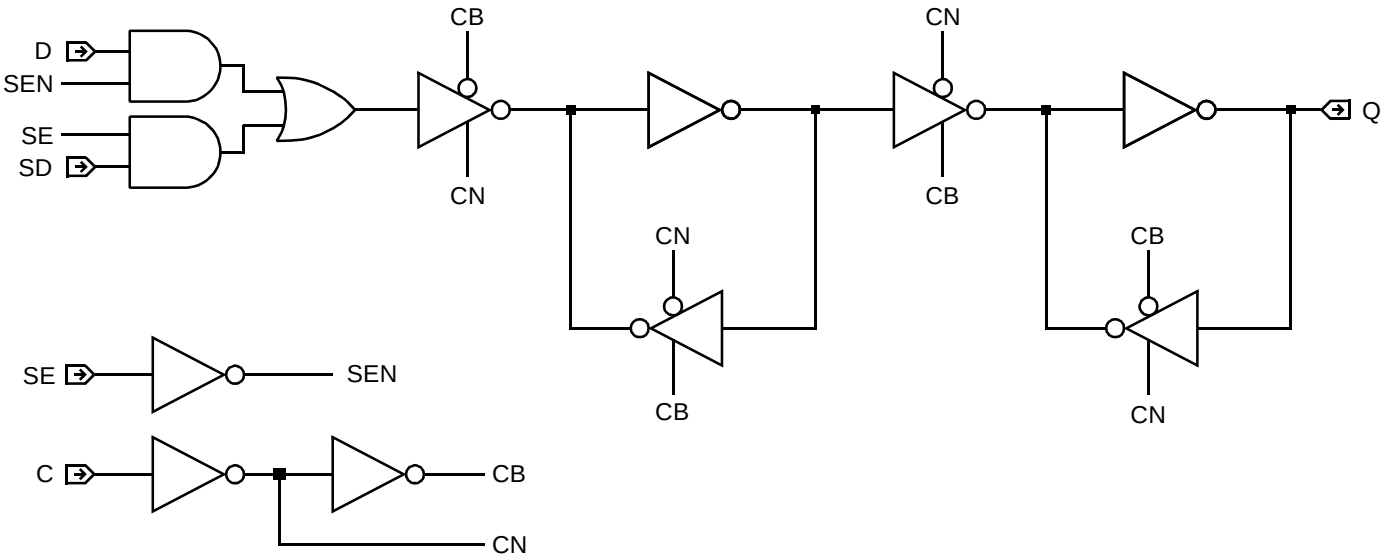
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			DF201	**DF202**
Min C Width	High	t_w	0.933	0.874
Min C Width	Low	t_w	1.351	1.227
Min D Setup		t_{su}	1.026	0.977
Min D Hold		t_h	0.271	0.263
Min SD Setup		t_{su}	1.026	0.977
Min SD Hold		t_h	0.271	0.263
Min SE Setup		t_{su}	1.209	1.160
Min SE Hold		t_h	0.271	0.263

AMI500MXSC 0.5 micron CMOS Standard Cell

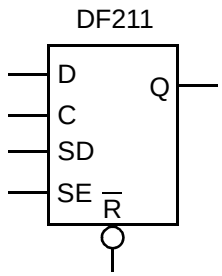
Logic Schematic



Description

DF211 is a static, master-slave, multiplexed scan D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q
↑	H	H	X	L	H
↑	L	H	X	L	L
↑	X	H	H	H	H
↑	X	H	L	H	L
X	X	L	X	X	L
L	X	H	X	X	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.1
D	1.0
RN	1.1
SD	1.0
SE	2.3

Equivalent Gates 6.2

HDL Syntax

Verilog ..... DF211 *inst_name* (Q, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF211 port map (Q, C, D, RN, SD, SE);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.517	nA
EQL_{pd}	17.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	1.054 0.830	1.282 1.011	1.643 1.255	1.891 1.410	2.271 1.634
RN	Q	t_{PHL}	0.547	0.709	0.917	1.069	1.292

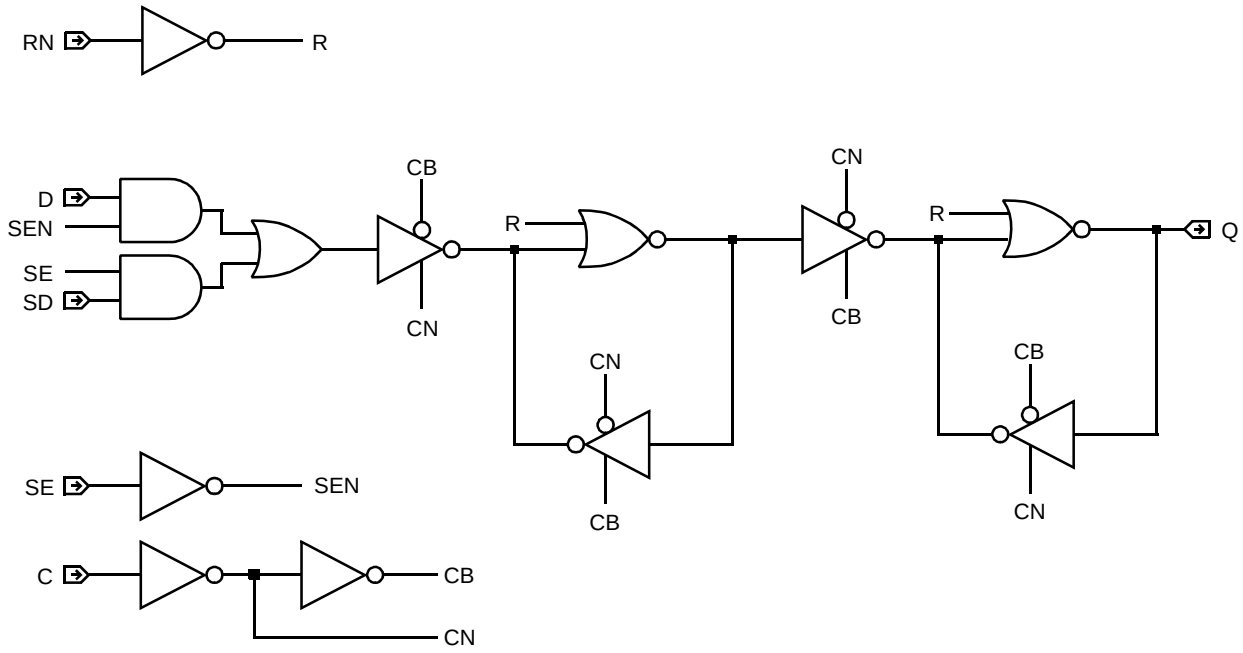
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	1.062
Min C Width	Low	t_w	1.389
Min RN Width	Low	t_w	0.769
Min D Setup		t_{su}	1.066
Min D Hold		t_h	0.270
Min SD Setup		t_{su}	1.066
Min SD Hold		t_h	0.270
Min SE Setup		t_{su}	1.251
Min SE Hold		t_h	0.270
Min RN Setup		t_{su}	0.499
Min RN Hold		t_h	0.489

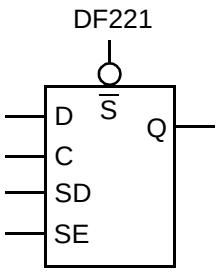
Logic Schematic



Description

DF221 is a static, master-slave, multiplexed scan D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q
↑	H	X	L	H	H
↑	L	X	L	H	L
↑	X	H	H	H	H
↑	X	L	H	H	L
X	X	X	X	L	H
L	X	X	X	H	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.0
D	1.0
SD	1.0
SE	2.3
SN	2.2

Equivalent Gates 5.8

HDL Syntax

Verilog ..... DF221 *inst_name* (Q, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF221 port map (Q, C, D, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.205	nA
EQL_{pd}	14.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	0.988 0.854	1.168 1.085	1.425 1.396	1.591 1.591	1.835 1.871
SN	Q	t_{PLH}	0.331	0.486	0.692	0.861	1.109

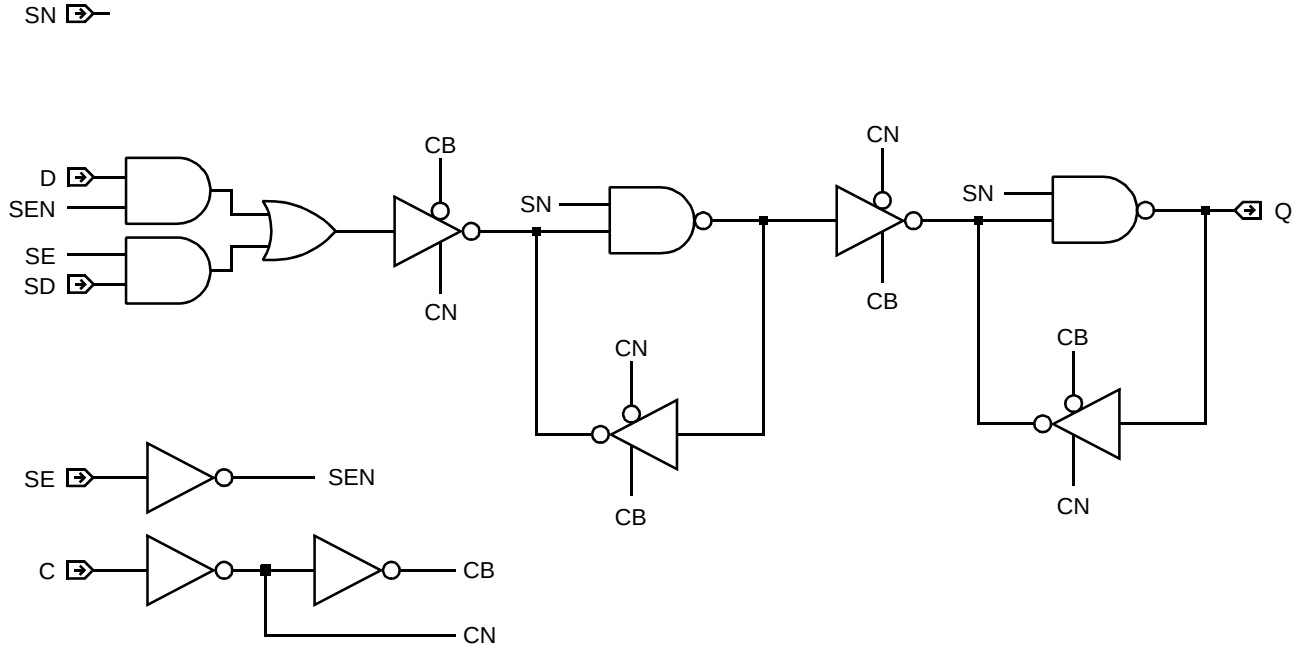
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.985
Min C Width	Low	t_w	1.417
Min SN Width	Low	t_w	0.643
Min D Setup		t_{su}	1.095
Min D Hold		t_h	0.269
Min SD Setup		t_{su}	1.095
Min SD Hold		t_h	0.269
Min SE Setup		t_{su}	1.279
Min SE Hold		t_h	0.269
Min SN Setup		t_{su}	0.292
Min SN Hold		t_h	0.728

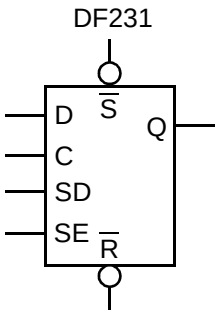
Logic Schematic



Description

DF231 is a static, master-slave, multiplexed scan D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q
↑	H	H	X	L	H	H
↑	L	H	X	L	H	L
↑	X	H	H	H	H	H
↑	X	H	L	H	H	L
X	X	L	X	X	H	L
X	X	H	X	X	L	H
X	X	L	X	X	L	IL
L	X	H	X	X	H	NC

NC = No Change IL = Illegal Condition

Pin Loading

	Equivalent Load
C	1.1
D	1.0
RN	1.0
SD	1.0
SE	2.3
SN	2.4

Equivalent Gates 7.2

HDL Syntax

Verilog ..... DF231 *inst_name* (Q, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF231 port map (Q, C, D, RN, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.340	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	1.028 0.811	1.306 1.059	1.747 1.398	2.049 1.612	2.513 1.923
RN	Q	t_{PHL}	0.549	0.779	1.094	1.312	1.631
SN	Q	t_{PLH}	0.290	0.434	0.599	0.743	0.955

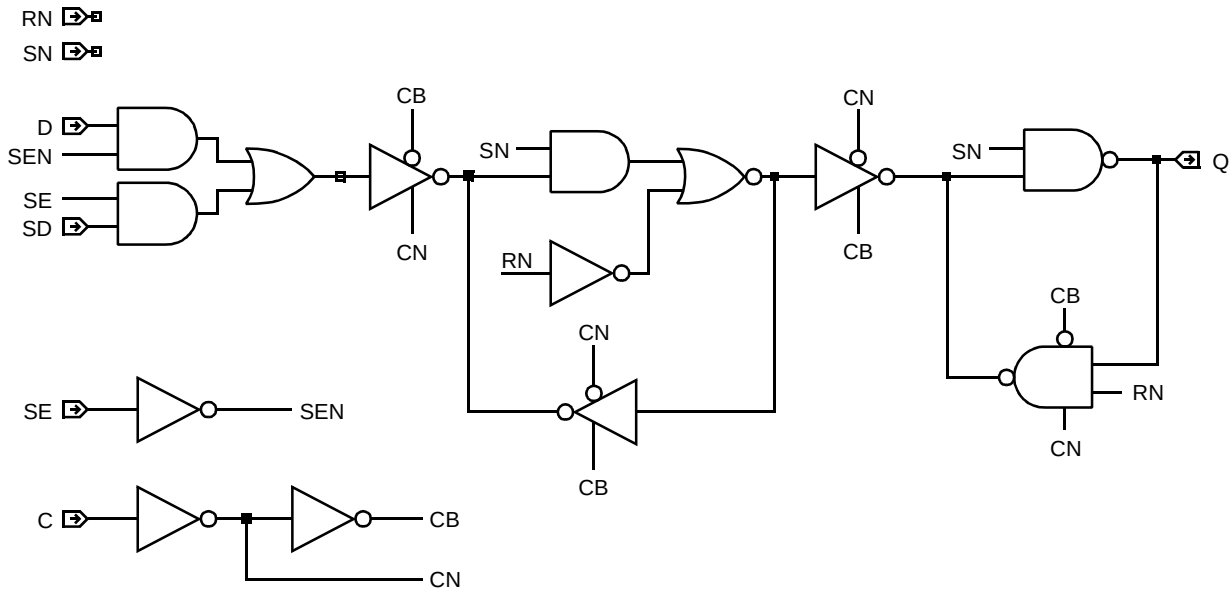
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	1.030
Min C Width	Low	t_w	1.319
Min RN Width	Low	t_w	1.063
Min SN Width	Low	t_w	0.816
Min D Setup		t_{su}	1.063
Min D Hold		t_h	0.268
Min SD Setup		t_{su}	1.063
Min SD Hold		t_h	0.268
Min SE Setup		t_{su}	1.246
Min SE Hold		t_h	0.268
Min RN Setup		t_{su}	0.540
Min RN Hold		t_h	0.653
Min SN Setup		t_{su}	0.324
Min SN Hold		t_h	0.875

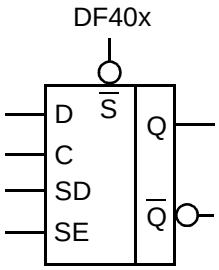
Logic Schematic



Description

DF40x is a family of static, master-slave, multiplexed scan D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q	QN
↑	H	X	L	H	H	L
↑	L	X	L	H	L	H
↑	X	H	H	H	H	L
↑	X	L	H	H	L	H
X	X	X	X	L	H	L
L	X	X	X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF40x *inst_name* (Q, QN, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF40x port map (Q, QN, C, D, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF401	DF402	DF404	DF406
C	1.0	1.1	1.1	1.1
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3
SN	2.1	2.2	3.3	3.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF401	6.8	2.573	17.5
DF402	6.8	2.897	20.0
DF404	8.5	3.954	27.4
DF406	9.2	4.636	32.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF401	From: C To: Q	t_{PLH} t_{PHL}	0.984 0.855	1.293 1.233	1.659 1.620	2.087 2.036	2.441 2.373
	From: C To: QN	t_{PLH} t_{PHL}	1.110 1.284	1.387 1.619	1.753 1.978	2.184 2.372	2.551 2.699
	From: SN To: Q	t_{PLH}	0.825	1.122	1.488	1.921	2.280
	From: SN To: QN	t_{PHL}	0.483	0.807	1.172	1.589	1.924
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF402	From: C To: Q	t_{PLH} t_{PHL}	1.023 0.829	1.333 1.236	1.667 1.588	1.980 1.879	2.326 2.181
	From: C To: QN	t_{PLH} t_{PHL}	1.262 1.366	1.570 1.702	1.887 2.009	2.157 2.262	2.473 2.537
	From: SN To: Q	t_{PLH}	0.930	1.224	1.552	1.846	2.172
	From: S To: QN	t_{PHL}	0.468	0.813	1.139	1.411	1.704
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF404	From: C To: Q	t_{PLH} t_{PHL}	0.997 0.806	1.326 1.250	1.638 1.586	1.917 1.859	2.248 2.122
	From: C To: QN	t_{PLH} t_{PHL}	1.085 1.251	1.317 1.543	1.617 1.838	1.925 2.083	2.269 2.321
	From: SN To: Q	t_{PLH}	1.048	1.370	1.685	1.975	2.298
	From: SN To: QN	t_{PHL}	0.417	0.674	0.923	1.175	1.445
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF406	From: C To: Q	t_{PLH} t_{PHL}	1.066 0.789	1.385 1.232	1.692 1.551	2.003 1.827	2.319 2.090
	From: C To: QN	t_{PLH} t_{PHL}	1.202 1.376	1.465 1.703	1.765 1.970	2.077 2.221	2.398 2.482
	From: SN To: Q	t_{PLH}	1.256	1.606	1.911	2.220	2.533
	From: SN To: QN	t_{PHL}	0.342	0.709	0.985	1.243	1.493

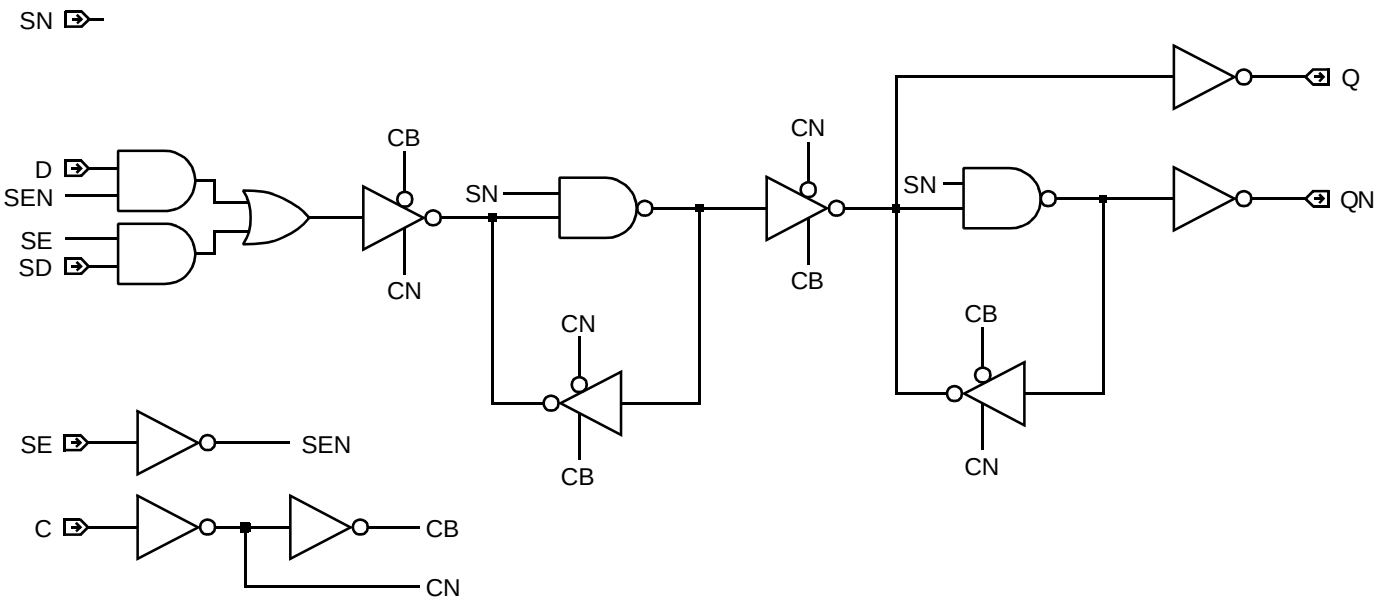
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF401	DF402	DF404	DF406
Min C Width	High	t_w	1.036	1.145	1.114	1.225
Min C Width	Low	t_w	1.415	1.421	1.464	1.464
Min SN Width	Low	t_w	0.659	0.762	0.887	1.056
Min D Setup		t_{su}	1.091	1.091	1.119	1.119
Min D Hold		t_h	0.271	0.272	0.285	0.286
Min SD Setup		t_{su}	1.091	1.091	1.119	1.119
Min SD Hold		t_h	0.271	0.272	0.285	0.286
Min SE Setup		t_{su}	1.274	1.276	1.310	1.309
Min SE Hold		t_h	0.271	0.272	0.285	0.286
Min SN Setup		t_{su}	0.292	0.292	0.340	0.340
Min SN Hold		t_h	0.727	0.732	0.966	0.965

Logic Schematic

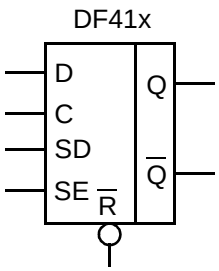


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DF41x is a family of static, master-slave, multiplexed scan D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q	QN
↑	H	H	X	L	H	L
↑	L	H	X	L	L	H
↑	X	H	H	H	H	L
↑	X	H	L	H	L	H
X	X	L	X	X	L	H
L	X	H	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF41x *inst_name* (Q, QN, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF41x port map (Q, QN, C, D, RN, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF411	DF412	DF414	DF416
C	1.1	1.1	1.1	1.1
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.1
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF411	7.2	2.910	20.5
DF412	7.2	3.257	23.0
DF414	9.0	4.405	31.3
DF416	10.0	5.147	37.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF411	From: C To: Q	t_{PLH} t_{PHL}	0.985 0.870	1.315 1.231	1.683 1.620	2.094 2.051	2.449 2.392
	From: C To: QN	t_{PLH} t_{PHL}	1.100 1.401	1.385 1.776	1.741 2.149	2.164 2.545	2.533 2.869
	From: RN To: Q	t_{PHL}	1.152	1.526	1.910	2.319	2.651
	From: RN To: QN	t_{PLH}	0.631	0.922	1.280	1.710	2.081
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF412	From: C To: Q	t_{PLH} t_{PHL}	1.077 0.841	1.371 1.276	1.686 1.629	1.973 1.906	2.296 2.203
	From: C To: QN	t_{PLH} t_{PHL}	1.236 1.479	1.519 1.867	1.833 2.189	2.113 2.444	2.435 2.741
	From: RN To: Q	t_{PHL}	1.183	1.582	1.919	2.187	2.475
	From: RN To: QN	t_{PLH}	0.614	0.933	1.272	1.575	1.910
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF414	From: C To: Q	t_{PLH} t_{PHL}	0.967 0.941	1.325 1.382	1.627 1.723	1.898 1.997	2.175 2.256
	From: C To: QN	t_{PLH} t_{PHL}	1.056 1.304	1.318 1.687	1.602 1.955	1.904 2.191	2.230 2.468
	From: RN To: Q	t_{PHL}	1.466	1.942	2.276	2.552	2.821
	From: RN To: QN	t_{PLH}	0.578	0.869	1.171	1.465	1.806
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF416	From: C To: Q	t_{PLH} t_{PHL}	1.107 0.797	1.459 1.278	1.753 1.584	2.033 1.853	2.309 2.114
	From: C To: QN	t_{PLH} t_{PHL}	1.202 1.455	1.453 1.863	1.738 2.137	2.035 2.361	2.342 2.591
	From: RN To: Q	t_{PHL}	1.658	2.183	2.502	2.783	3.027
	From: RN To: QN	t_{PLH}	0.609	0.918	1.221	1.528	1.842

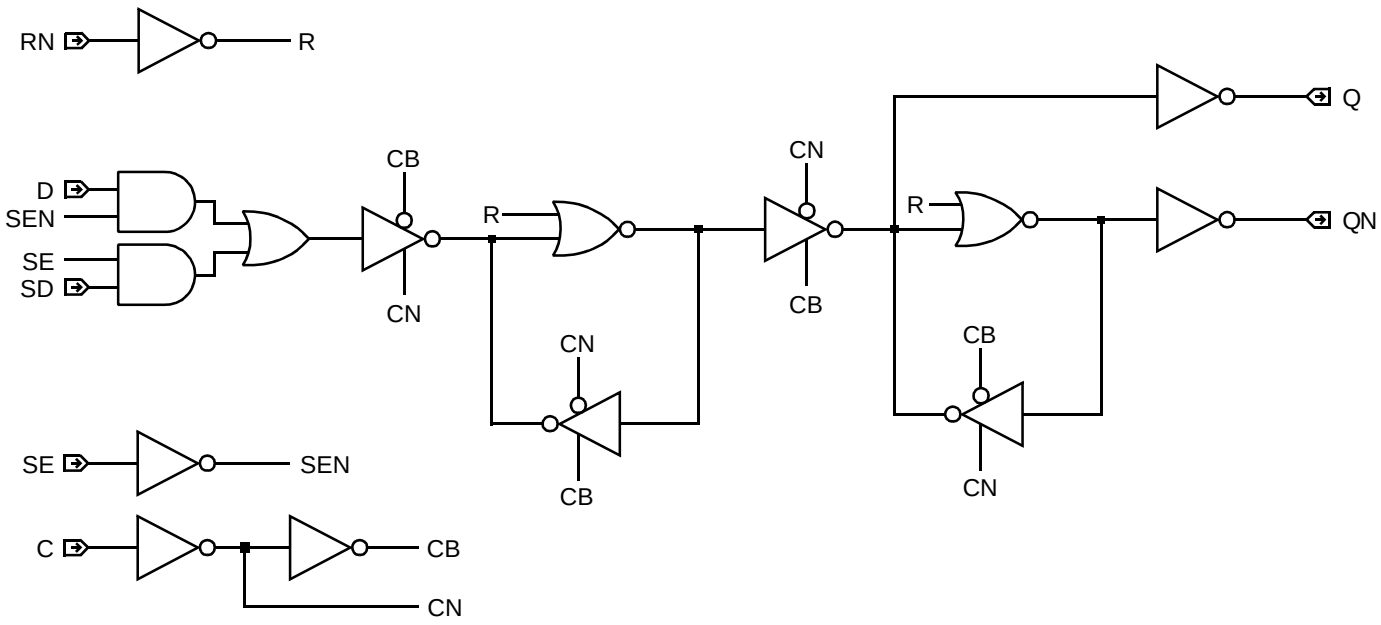
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF411	DF412	DF414	DF416
Min C Width	High	t_w	1.099	1.215	1.167	1.304
Min C Width	Low	t_w	1.405	1.405	1.446	1.446
Min RN Width	Low	t_w	0.771	0.771	1.181	1.183
Min D Setup		t_{su}	1.074	1.074	1.104	1.104
Min D Hold		t_h	0.273	0.273	0.286	0.287
Min SD Setup		t_{su}	1.074	1.074	1.104	1.104
Min SD Hold		t_h	0.273	0.273	0.286	0.287
Min SE Setup		t_{su}	1.260	1.260	1.292	1.292
Min SE Hold		t_h	0.273	0.273	0.286	0.287
Min RN Setup		t_{su}	0.498	0.498	0.599	0.600
Min RN Hold		t_h	0.496	0.496	0.698	0.698

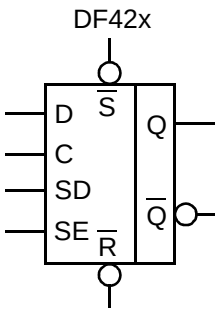
Logic Schematic



Description

DF42x is a family of static, master-slave, multiplexed scan D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	H	H	X	L	H	H	L
↑	L	H	X	L	H	L	H
↑	X	H	H	H	H	H	L
↑	X	H	L	H	H	L	H
X	X	L	X	X	H	L	H
X	X	H	X	X	L	H	L
X	X	L	X	X	L	IL	IL
L	X	H	X	X	H	NC	NC

NC = No Change IL = Illegal Condition

HDL Syntax

Verilog ..... DF421x *inst_name* (Q, QN, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF421x port map (Q, QN, C, D, RN, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF421	DF422	DF424	DF426
C	1.1	1.1	1.1	1.1
D	1.0	1.0	1.0	1.0
RN	1.1	1.1	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3
SN	2.4	2.4	2.4	2.5

AMI500MXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF421	8.2	2.709	20.4
DF422	8.2	3.031	23.0
DF424	9.5	4.027	30.4
DF426	10.2	4.709	36.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF421	From: C To: Q	t_{PLH} t_{PHL}	0.921 0.810	1.227 1.185	1.596 1.573	2.022 1.990	2.392 2.317
	From: C To: QN	t_{PLH} t_{PHL}	1.082 1.385	1.395 1.767	1.755 2.144	2.165 2.540	2.516 2.876
	From: RN To: Q	t_{PHL}	1.710	2.168	2.608	3.063	3.408
	From: RN To: QN	t_{PLH}	0.673	0.981	1.350	1.780	2.141
	From: SN To: Q	t_{PLH}	1.114	1.433	1.807	2.240	2.592
	From: SN To: QN	t_{PHL}	0.468	0.786	1.153	1.567	1.899
DF422	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.940 0.807	1.260 1.211	1.597 1.566	1.909 1.854	2.255 2.155
	From: C To: QN	t_{PLH} t_{PHL}	1.237 1.478	1.524 1.862	1.845 2.199	2.135 2.474	2.466 2.769
	From: RN To: Q	t_{PHL}	1.838	2.354	2.760	3.073	3.420
	From: RN To: QN	t_{PLH}	0.677	1.018	1.368	1.666	1.999
	From: SN To: Q	t_{PLH}	1.304	1.646	1.984	2.269	2.594
	From: SN To: QN	t_{PHL}	0.434	0.784	1.102	1.376	1.695

	Number of Equivalent Loads		1	19	38	56	75 (max)
DF424	From: C To: Q	t_{PLH} t_{PHL}	1.579 1.327	1.893 1.710	2.200 1.983	2.483 2.206	2.774 2.430
	From: C To: QN	t_{PLH} t_{PHL}	1.035 1.281	1.348 1.582	1.664 1.807	1.943 2.046	2.245 2.321
	From: RN To: Q	t_{PHL}	0.864	1.196	1.491	1.742	1.991
	From: RN To: QN	t_{PLH}	2.032	2.333	2.634	2.913	3.203
	From: SN To: Q	t_{PLH}	0.612	0.907	1.222	1.522	1.844
	From: SN To: QN	t_{PHL}	1.414	1.755	2.024	2.253	2.481
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF426	From: C To: Q	t_{PLH} t_{PHL}	1.715 1.414	2.002 1.786	2.313 2.069	2.627 2.319	2.943 2.549
	From: C To: QN	t_{PLH} t_{PHL}	1.108 1.210	1.441 1.618	1.694 1.890	1.997 2.150	2.319 2.400
	From: RN To: Q	t_{PHL}	1.007	1.373	1.635	1.913	2.147
	From: RN To: QN	t_{PLH}	2.130	2.460	2.734	3.003	3.286
	From: SN To: Q	t_{PLH}	0.717	1.041	1.344	1.650	1.964
	From: SN To: QN	t_{PHL}	1.510	1.879	2.170	2.431	2.673

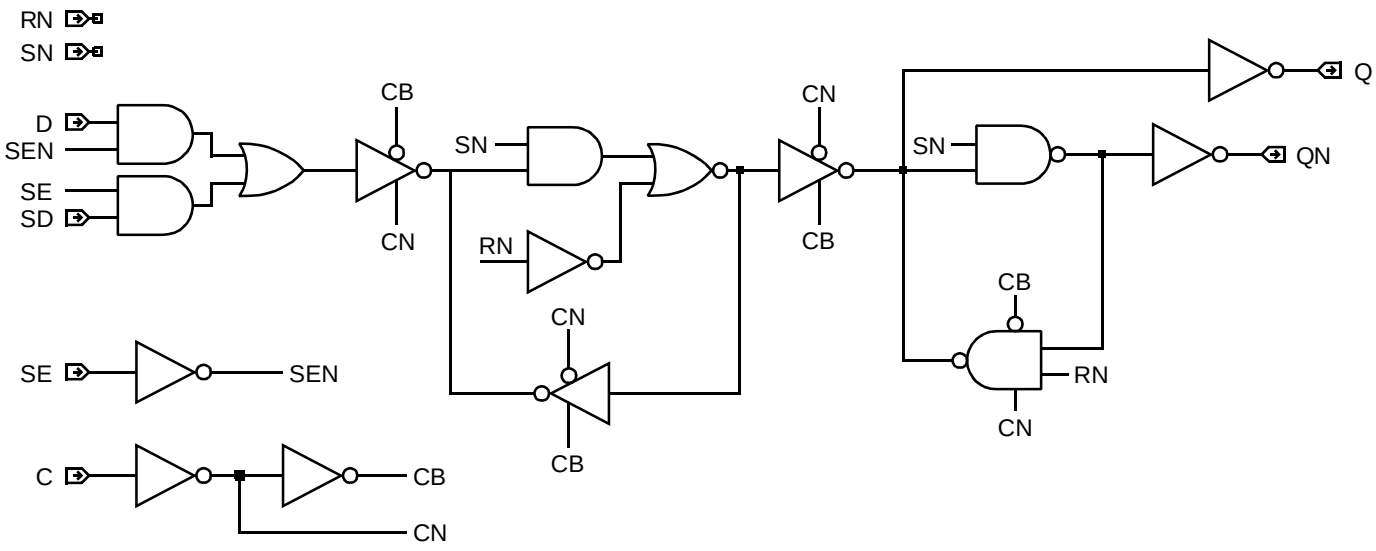
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF421	DF422	DF424	DF426
Min C Width	High	t_w	1.065	1.197	1.085	1.103
Min C Width	Low	t_w	1.321	1.307	1.324	1.320
Min RN Width	Low	t_w	1.078	1.066	1.067	1.067
Min SN Width	Low	t_w	0.901	1.085	0.936	0.944
Min D Setup		t_{su}	1.066	1.056	1.067	1.061
Min D Hold		t_h	0.266	0.265	0.268	0.267
Min SD Setup		t_{su}	1.066	1.056	1.067	1.061
Min SD Hold		t_h	0.266	0.265	0.268	0.267
Min SE Setup		t_{su}	1.249	1.240	1.250	1.243
Min SE Hold		t_h	0.266	0.265	0.268	0.267
Min RN Setup		t_{su}	0.549	0.543	0.543	0.542
Min RN Hold		t_h	0.652	0.645	0.654	0.652
Min SN Setup		t_{su}	0.321	0.317	0.326	0.319
Min SN Hold		t_h	0.881	0.872	0.881	0.881

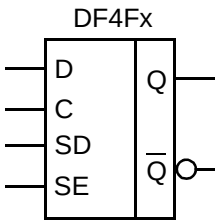
Logic Schematic



Description

DF4Fx is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q	QN
↑	H	X	L	H	L
↑	L	X	L	L	H
↑	X	H	H	H	L
↑	X	L	H	L	H
L	X	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF4Fx *inst_name* (Q, QN, C, D, SD, SE);

VHDL..... *inst_name*: DF4Fx port map (Q, QN, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF4F1	DF4F2	DF4F4	DF4F6
C	1.0	1.1	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.4	2.3	2.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF4F1	6.2	2.395	16.5
DF4F2	6.2	2.740	19.1
DF4F4	7.2	3.631	24.2
DF4F6	8.0	4.545	31.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF4F1	From: C To: Q	t_{PLH} t_{PHL}	0.964 0.866	1.262 1.216	1.627 1.602	2.062 2.016	2.423 2.351
	From: C To: QN	t_{PLH} t_{PHL}	1.027 1.210	1.311 1.485	1.666 1.839	2.088 2.267	2.459 2.638
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF4F2	From: C To: Q	t_{PLH} t_{PHL}	0.998 0.810	1.318 1.235	1.651 1.588	1.941 1.868	2.257 2.157
	From: C To: QN	t_{PLH} t_{PHL}	1.153 1.286	1.422 1.610	1.735 1.912	2.020 2.164	2.348 2.436
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF4F4	From: C To: Q	t_{PLH} t_{PHL}	1.351 1.143	1.588 1.432	1.885 1.713	2.189 1.969	2.528 2.229
	From: C To: QN	t_{PLH} t_{PHL}	0.869 1.026	1.153 1.301	1.471 1.585	1.767 1.851	2.080 2.132
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF4F6	From: C To: Q	t_{PLH} t_{PHL}	1.318 1.216	1.578 1.499	1.877 1.775	2.184 2.032	2.502 2.270
	From: C To: QN	t_{PLH} t_{PHL}	0.926 1.077	1.202 1.436	1.502 1.726	1.819 1.986	2.152 2.229

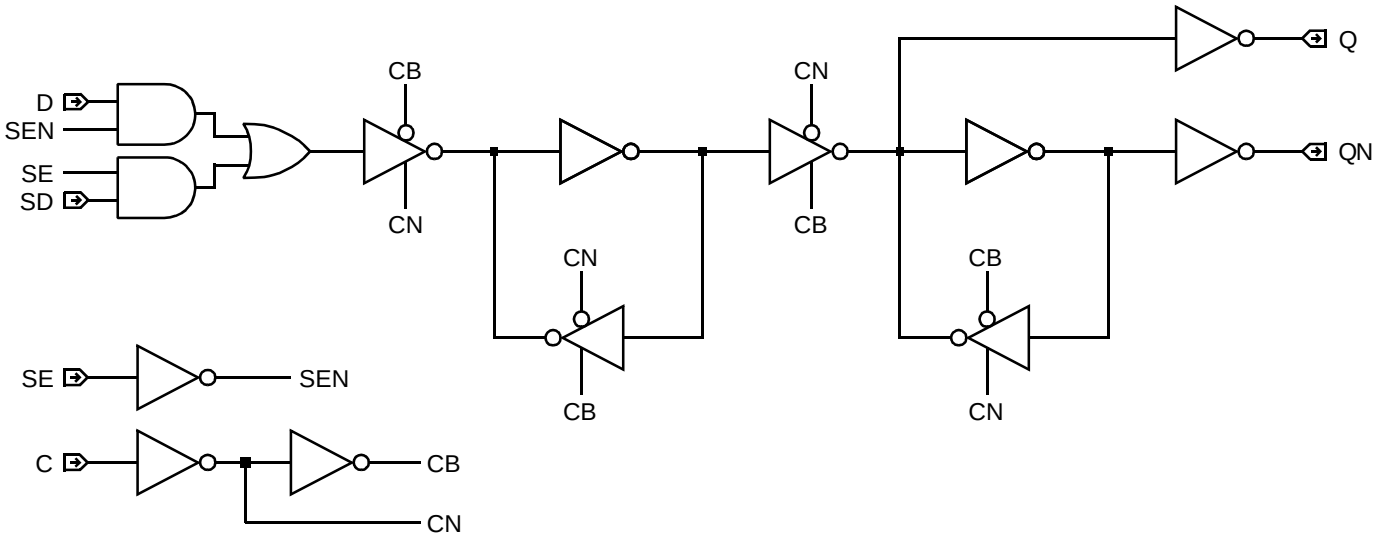
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF4F1	DF4F2	DF4F4	DF4F6
Min C Width	High	t_w	0.976	1.074	0.900	0.952
Min C Width	Low	t_w	1.325	1.352	1.222	1.222
Min D Setup		t_{su}	1.014	1.028	0.977	0.977
Min D Hold		t_h	0.264	0.270	0.259	0.259
Min SD Setup		t_{su}	1.014	1.028	0.977	0.977
Min SD Hold		t_h	0.264	0.270	0.259	0.259
Min SE Setup		t_{su}	1.198	1.211	1.159	1.159
Min SE Hold		t_h	0.264	0.270	0.259	0.259

Logic Schematic

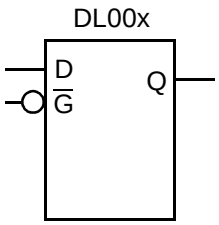


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DL00x is a family of transparent, unbuffered D latch with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

GN	D	Q
L	L	L
L	H	H
H	X	NC

NC = No Change

HDL Syntax

Verilog ..... DL00x *inst_name* (Q, D, GN);

VHDL..... *inst_name*: DL00x port map (Q, D, GN);

Pin Loading

Pin Name	Equivalent Loads	
	DL001	DL002
D	1.0	1.0
GN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL001	2.5	0.998	4.3
DL002	2.5	1.089	4.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DL001	From: D To: Q	t_{PLH} t_{PHL}	0.503 0.622	0.805 0.938	1.166 1.281	1.588 1.688	1.935 2.048
	From: GN To: Q	t_{PLH} t_{PHL}	0.645 0.880	0.945 1.179	1.306 1.539	1.730 1.963	2.079 2.312
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DL002	From: D To: Q	t_{PLH} t_{PHL}	0.463 0.543	0.792 0.917	1.142 1.253	1.450 1.528	1.787 1.817
	From: GN To: Q	t_{PLH} t_{PHL}	0.593 0.773	0.915 1.120	1.260 1.453	1.567 1.732	1.904 2.030

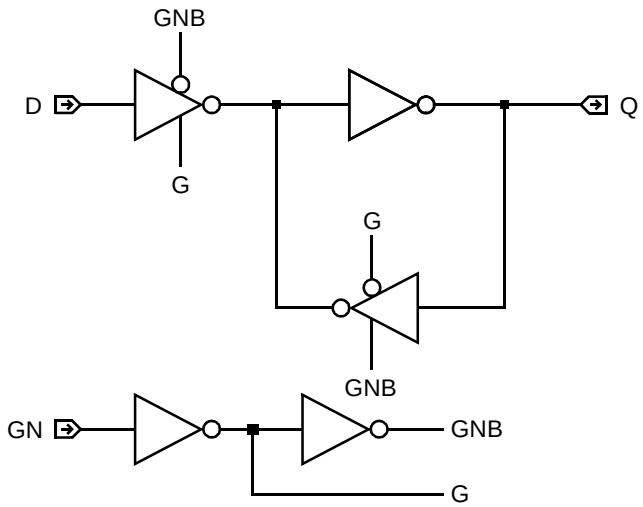
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DL001	Cell DL002
Min GN Width	Low	t_w	0.882	0.786
Min D Setup		t_{su}	0.615	0.556
Min D Hold		t_h	0.213	0.212

Logic Schematic



Core Logic

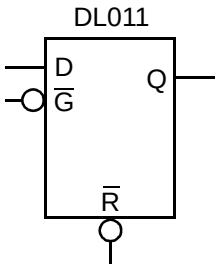
DL011

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DL011 is a transparent, unbuffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q
H	L	L	L
H	H	L	H
H	X	H	NC
L	X	X	L

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
RN	1.0

Equivalent Gates 3.2

HDL Syntax

Verilog ..... DL011 *inst_name* (Q, D, GN, RN);

VHDL..... *inst_name*: DL011 port map (Q, D, GN, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.270	nA
EQL_{pd}	5.5	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
D	Q	t_{PLH} t_{PHL}	0.557 0.602	0.804 0.786	1.162 1.027	1.400 1.177	1.763 1.389
GN	Q	t_{PLH} t_{PHL}	0.679 0.827	0.924 1.008	1.286 1.251	1.526 1.404	1.884 1.624
RN	Q	t_{PLH} t_{PHL}	0.458 0.380	0.700 0.539	1.061 0.770	1.300 0.920	1.658 1.143

Delay (ns)

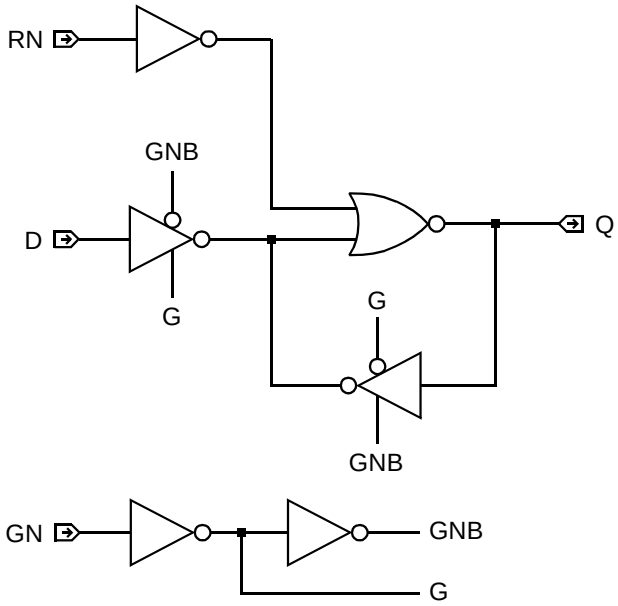
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.830
Min RN Width	Low	t_w	0.900
Min D Setup		t_{su}	0.600
Min D Hold		t_h	0.214
Min RN Setup		t_{su}	0.461
Min RN Hold		t_h	0.306

Logic Schematic



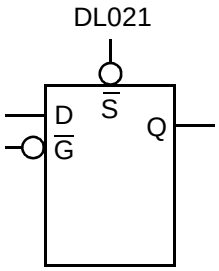
DL021

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DL021 is a transparent, unbuffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q
L	X	X	H
H	H	X	NC
H	L	L	L
H	L	H	H

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
SN	1.0

Equivalent Gates 2.8

HDL Syntax

Verilog ..... DL021 *inst_name* (Q, D, GN, SN);

VHDL..... *inst_name*: DL021 port map (Q, D, GN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.006	nA
EQL_{pd}	3.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
D	Q	t_{PLH} t_{PHL}	0.498 0.624	0.673 0.841	0.931 1.151	1.101 1.351	1.355 1.647
GN	Q	t_{PLH} t_{PHL}	0.625 0.848	0.798 1.052	1.054 1.364	1.223 1.575	1.475 1.892
SN	Q	t_{PLH} t_{PHL}	0.249 0.333	0.422 0.524	0.671 0.786	0.834 0.961	1.080 1.220

Delay (ns)

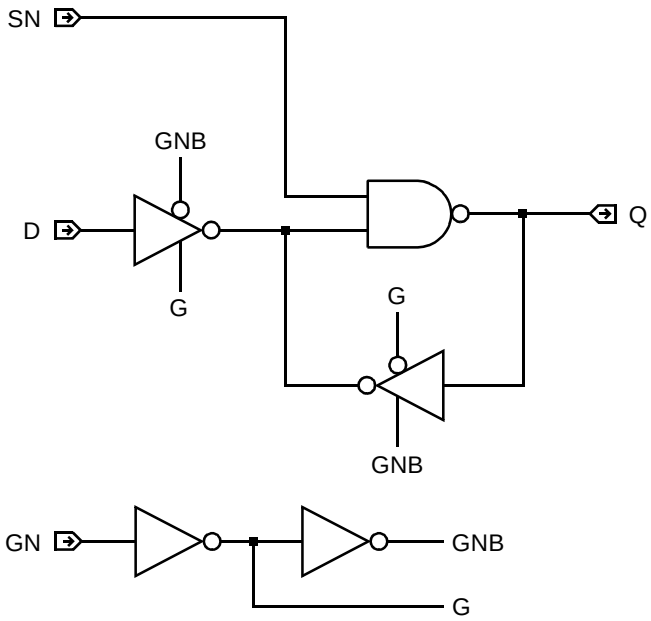
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.851
Min SN Width	Low	t_w	0.805
Min D Setup		t_{su}	0.625
Min D Hold		t_h	0.198
Min SN Setup		t_{su}	0.332
Min SN Hold		t_h	0.673

Logic Schematic



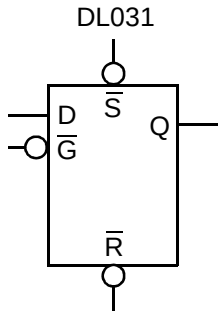
DL031

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DL031 is a transparent, unbuffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	X	H	NC
H	H	L	L	L
H	H	H	L	H

NC = No Change IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
GN	1.1
SN	1.0
RN	1.0

Core Logic

Equivalent Gates 3.5

HDL Syntax

Verilog ..... DL031 *inst_name* (Q, D, GN, RN, SN);

VHDL..... *inst_name*: DL031 port map (Q, D, GN, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.267	nA
EQL_{pd}	5.5	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	6	8	11 (max)
D	Q	t_{PLH} t_{PHL}	0.633 0.784	0.830 1.013	1.098 1.334	1.267 1.541	1.513 1.843
GN	Q	t_{PLH} t_{PHL}	0.759 1.047	0.936 1.265	1.200 1.587	1.376 1.799	1.638 2.116
SN	Q	t_{PLH} t_{PHL}	0.265 0.302	0.437 0.519	0.688 0.817	0.854 1.009	1.100 1.289
RN	Q	t_{PLH} t_{PHL}	0.678 0.661	0.865 0.901	1.130 1.218	1.302 1.415	1.556 1.696

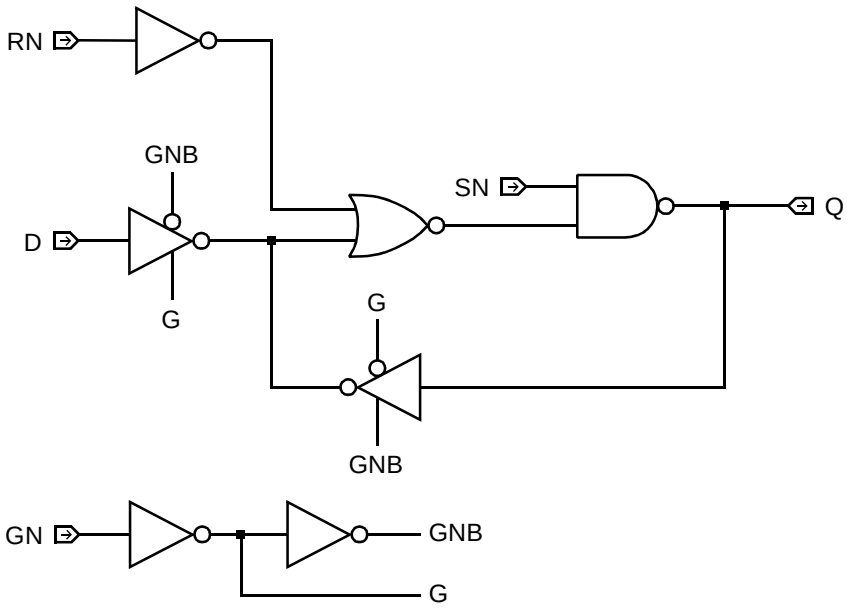
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	1.050
Min RN Width	Low	t_w	0.250
Min SN Width	Low	t_w	0.681
Min D Setup		t_{su}	0.800
Min D Hold		t_h	0.207
Min SN Setup		t_{su}	0.309
Min SN Hold		t_h	0.590
Min RN Setup		t_{su}	0.681
Min RN Hold		t_h	0.305

Logic Schematic

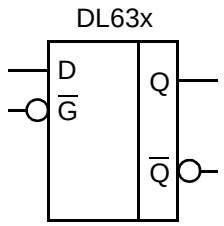


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DL63x is a family of transparent, buffered D latches with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

D	GN	Q	QN
L	L	L	H
H	L	H	L
X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DL63x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL63x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL631	DL632	DL634	DL636
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL631	4.0	1.506	8.2
DL632	4.0	1.854	10.8
DL634	4.5	2.710	15.6
DL636	5.2	3.624	22.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DL631	From: D To: Q	t_{PLH} t_{PHL}	0.807 0.861	1.086 1.133	1.456 1.486	1.894 1.916	2.239 2.279
	From: D To: QN	t_{PLH} t_{PHL}	0.751 0.712	1.038 1.026	1.397 1.389	1.827 1.805	2.185 2.143
	From: GN To: Q	t_{PLH} t_{PHL}	0.935 1.114	1.214 1.396	1.570 1.744	2.003 2.159	2.368 2.505
	From: GN To: QN	t_{PLH} t_{PHL}	0.975 0.832	1.267 1.150	1.626 1.512	2.052 1.924	2.405 2.256
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DL632	From: D To: Q	t_{PLH} t_{PHL}	0.902 0.908	1.192 1.235	1.513 1.547	1.800 1.809	2.120 2.088
	From: D To: QN	t_{PLH} t_{PHL}	0.734 0.683	1.055 1.029	1.396 1.358	1.698 1.636	2.029 1.930
	From: GN To: Q	t_{PLH} t_{PHL}	1.022 1.166	1.319 1.455	1.640 1.755	1.925 2.017	2.238 2.303
	From: GN To: QN	t_{PLH} t_{PHL}	0.979 0.811	1.277 1.159	1.604 1.485	1.898 1.758	2.222 2.047
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DL634	From: D To: Q	t_{PLH} t_{PHL}	0.917 0.955	1.187 1.254	1.500 1.569	1.808 1.850	2.141 2.115
	From: D To: QN	t_{PLH} t_{PHL}	0.690 0.610	0.990 0.944	1.296 1.228	1.586 1.479	1.894 1.731
	From: GN To: Q	t_{PLH} t_{PHL}	1.013 1.163	1.286 1.533	1.607 1.816	1.925 2.052	2.271 2.281
	From: GN To: QN	t_{PLH} t_{PHL}	0.912 0.730	1.214 1.034	1.535 1.323	1.839 1.585	2.162 1.853

	Number of Equivalent Loads		1	28	56	84	112 (max)
DL636	From: D To: Q	t_{PLH} t_{PHL}	0.926 0.976	1.226 1.224	1.513 1.494	1.793 1.769	2.067 2.047
	From: D To: QN	t_{PLH} t_{PHL}	0.749 0.657	1.050 1.045	1.369 1.341	1.688 1.603	2.006 1.843
	From: GN To: Q	t_{PLH} t_{PHL}	1.062 1.172	1.279 1.478	1.563 1.755	1.877 2.016	2.211 2.268
	From: GN To: QN	t_{PLH} t_{PHL}	0.973 0.804	1.321 1.175	1.623 1.474	1.918 1.736	2.201 1.976

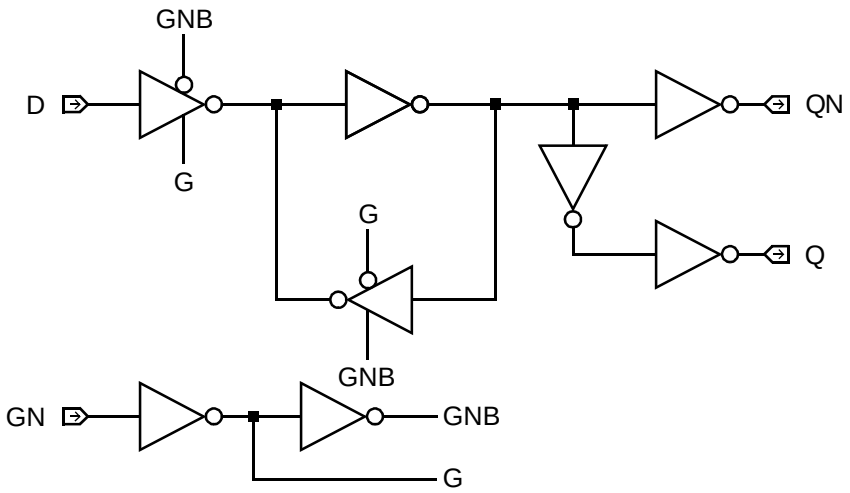
Delay will vary with input conditions. See page 2-Reference for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DL631	DL632	DL634	DL636
Min GN Width	Low	t_w	0.820	0.857	0.843	0.903
Min D Setup		t_{su}	0.576	0.612	0.600	0.664
Min D Hold		t_h	0.213	0.213	0.214	0.210

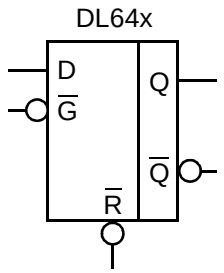
Logic Schematic



Description

DL64x is a family of transparent, buffered D latches with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

HDL Syntax

Verilog ..... DL64x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL64x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL641	DL642	DL644	DL646
D	1.0	1.0	1.0	1.0
GN	1.1	1.1	1.0	1.0
RN	1.0	1.1	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL641	4.0	1.490	8.5
DL642	4.0	1.813	11.0
DL644	5.8	3.441	20.6
DL646	6.2	4.161	26.1

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DL641	From: D To: Q	t_{PLH} t_{PHL}	0.646 0.797	0.992 1.185	1.370 1.572	1.790 1.992	2.123 2.327
	From: D To: QN	t_{PLH} t_{PHL}	0.965 0.889	1.267 1.209	1.622 1.568	2.031 1.974	2.364 2.300
	From: GN To: Q	t_{PLH} t_{PHL}	0.756 1.038	1.102 1.418	1.480 1.818	1.902 2.255	2.236 2.598
	From: GN To: QN	t_{PLH} t_{PHL}	1.219 1.009	1.522 1.309	1.877 1.669	2.290 2.090	2.626 2.435
	From: RN To: Q	t_{PLH} t_{PHL}	0.672 0.596	1.006 0.962	1.385 1.342	1.817 1.753	2.166 2.074
	From: RN To: QN	t_{PLH} t_{PHL}	0.798 0.924	1.073 1.248	1.417 1.609	1.843 2.015	2.206 2.340
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DL642	From: D To: Q	t_{PLH} t_{PHL}	0.658 0.753	1.025 1.196	1.380 1.561	1.682 1.849	2.005 2.143
	From: D To: QN	t_{PLH} t_{PHL}	1.131 0.960	1.408 1.268	1.720 1.578	2.002 1.844	2.317 2.132
	From: GN To: Q	t_{PLH} t_{PHL}	0.794 1.024	1.140 1.454	1.485 1.811	1.781 2.092	2.099 2.377
	From: GN To: QN	t_{PLH} t_{PHL}	1.358 1.096	1.655 1.419	1.969 1.728	2.246 1.989	2.550 2.268
	From: RN To: Q	t_{PLH} t_{PHL}	0.692 0.531	1.071 0.948	1.424 1.290	1.718 1.559	2.028 1.834
	From: RN To: QN	t_{PLH} t_{PHL}	0.880 1.003	1.143 1.302	1.458 1.613	1.752 1.886	2.085 2.183

	Number of Equivalent Loads		1	19	38	56	75 (max)
DL644	From: D To: Q	t_{PLH} t_{PHL}	0.958 0.855	1.281 1.178	1.574 1.475	1.872 1.737	2.206 2.001
	From: D To: QN	t_{PLH} t_{PHL}	1.017 1.081	1.331 1.391	1.649 1.668	1.944 1.913	2.252 2.161
	From: GN To: Q	t_{PLH} t_{PHL}	1.039 1.087	1.362 1.417	1.679 1.702	1.967 1.944	2.261 2.181
	From: GN To: QN	t_{PLH} t_{PHL}	1.276 1.208	1.597 1.513	1.912 1.762	2.201 2.027	2.501 2.332
	From: RN To: Q	t_{PLH} t_{PHL}	0.804 0.646	1.140 0.990	1.442 1.282	1.732 1.538	2.052 1.795
	From: RN To: QN	t_{PLH} t_{PHL}	0.914 1.004	1.190 1.289	1.496 1.550	1.791 1.795	2.109 2.059
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DL646	From: D To: Q	t_{PLH} t_{PHL}	0.972 0.881	1.174 1.133	1.371 1.336	1.575 1.507	1.815 1.674
	From: D To: QN	t_{PLH} t_{PHL}	1.134 1.188	1.360 1.392	1.553 1.584	1.738 1.760	1.937 1.944
	From: GN To: Q	t_{PLH} t_{PHL}	1.123 1.142	1.297 1.428	1.494 1.619	1.685 1.771	1.892 1.914
	From: GN To: QN	t_{PLH} t_{PHL}	1.394 1.282	1.590 1.538	1.785 1.721	1.964 1.869	2.150 2.011
	From: RN To: Q	t_{PLH} t_{PHL}	0.867 0.679	1.121 0.924	1.320 1.128	1.498 1.302	1.692 1.474
	From: RN To: QN	t_{PLH} t_{PHL}	0.914 1.080	1.109 1.284	1.319 1.476	1.517 1.653	1.725 1.837

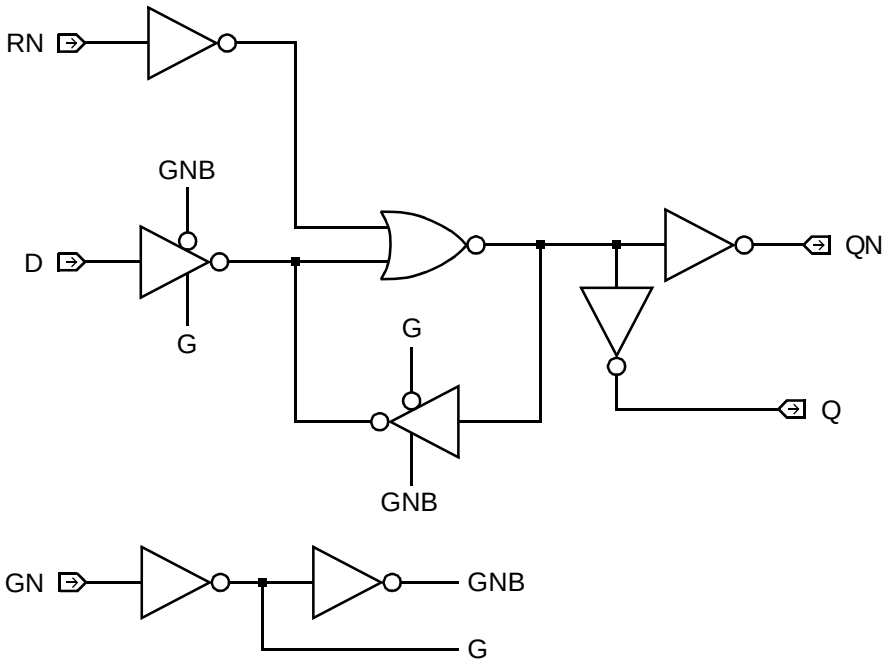
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL641	DL642	DL644	DL646
Min GN Width	Low	t_w	0.793	0.941	0.831	0.831
Min RN Width	Low	t_w	0.605	0.700	0.906	0.906
Min D Setup		t_{su}	0.793	0.941	0.585	0.584
Min D Hold		t_h	0.207	0.208	0.216	0.216
Min RN Setup		t_{su}	0.475	0.533	0.443	0.444
Min RN Hold		t_h	0.303	0.304	0.516	0.516

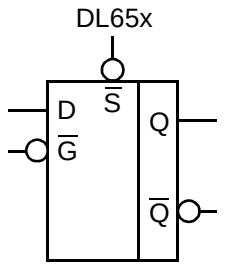
Logic Schematic



Description

DL65x is a family of transparent, buffered D latches with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

HDL Syntax

Verilog ..... DL65x *inst_name* (Q, QN, D, GN, SN);

VHDL..... *inst_name*: DL65x port map (Q, QN, D, GN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL651	DL652	DL654	DL656
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
SN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL651	4.5	1.567	8.6
DL652	4.5	1.904	11.0
DL654	5.2	3.128	19.3
DL656	6.0	3.861	24.7

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DL651	From: D To: Q	t_{PLH} t_{PHL}	0.874 0.959	1.168 1.254	1.526 1.604	1.948 2.013	2.297 2.347
	From: D To: QN	t_{PLH} t_{PHL}	0.800 0.781	1.117 1.110	1.482 1.469	1.901 1.880	2.239 2.224
	From: GN To: Q	t_{PLH} t_{PHL}	0.988 1.187	1.305 1.484	1.663 1.835	2.068 2.242	2.393 2.574
	From: GN To: QN	t_{PLH} t_{PHL}	1.044 0.892	1.345 1.244	1.710 1.612	2.140 2.011	2.495 2.322
	From: SN To: Q	t_{PLH} t_{PHL}	0.639 0.655	0.923 0.908	1.278 1.235	1.706 1.648	2.063 2.006
	From: SN To: QN	t_{PLH} t_{PHL}	0.496 0.535	0.803 0.882	1.159 1.248	1.580 1.656	1.939 1.987
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DL652	From: D To: Q	t_{PLH} t_{PHL}	0.955 1.027	1.259 1.326	1.582 1.626	1.868 1.883	2.182 2.160
	From: D To: QN	t_{PLH} t_{PHL}	0.804 0.740	1.131 1.097	1.476 1.431	1.779 1.710	2.112 2.005
	From: GN To: Q	t_{PLH} t_{PHL}	1.084 1.246	1.382 1.540	1.702 1.840	1.985 2.100	2.297 2.382
	From: GN To: QN	t_{PLH} t_{PHL}	1.052 0.867	1.376 1.227	1.705 1.558	1.991 1.832	2.300 2.121
	From: SN To: Q	t_{PLH} t_{PHL}	0.711 0.689	1.013 0.981	1.343 1.293	1.638 1.568	1.964 1.869
	From: SN To: QN	t_{PLH} t_{PHL}	0.493 0.487	0.832 0.877	1.159 1.208	1.443 1.479	1.759 1.769

	Number of Equivalent Loads		1	19	38	56	75 (max)
DL654	From: D To: Q	t_{PLH} t_{PHL}	0.844 0.903	1.125 1.259	1.432 1.545	1.730 1.787	2.049 2.025
	From: D To: QN	t_{PLH} t_{PHL}	1.104 0.883	1.365 1.242	1.670 1.513	1.971 1.759	2.297 2.027
	From: GN To: Q	t_{PLH} t_{PHL}	0.957 1.166	1.230 1.478	1.536 1.761	1.833 2.025	2.151 2.311
	From: GN To: QN	t_{PLH} t_{PHL}	1.344 1.132	1.567 1.381	1.885 1.656	2.216 1.929	2.574 2.233
	From: SN To: Q	t_{PLH} t_{PHL}	0.527 0.603	0.865 0.923	1.191 1.218	1.501 1.482	1.835 1.752
	From: SN To: QN	t_{PLH} t_{PHL}	0.783 0.753	1.081 1.016	1.378 1.301	1.669 1.573	1.990 1.863
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DL656	From: D To: Q	t_{PLH} t_{PHL}	0.872 0.967	1.183 1.253	1.482 1.545	1.776 1.819	2.069 2.070
	From: D To: QN	t_{PLH} t_{PHL}	1.143 1.072	1.466 1.361	1.780 1.640	2.086 1.911	2.387 2.176
	From: GN To: Q	t_{PLH} t_{PHL}	0.997 1.194	1.299 1.533	1.588 1.818	1.880 2.079	2.175 2.326
	From: GN To: QN	t_{PLH} t_{PHL}	1.409 1.180	1.687 1.498	2.000 1.785	2.324 2.056	2.656 2.314
	From: SN To: Q	t_{PLH} t_{PHL}	0.617 0.614	0.915 0.964	1.223 1.241	1.529 1.512	1.832 1.779
	From: SN To: QN	t_{PLH} t_{PHL}	0.874 0.789	1.143 1.113	1.457 1.408	1.780 1.681	2.105 1.942

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

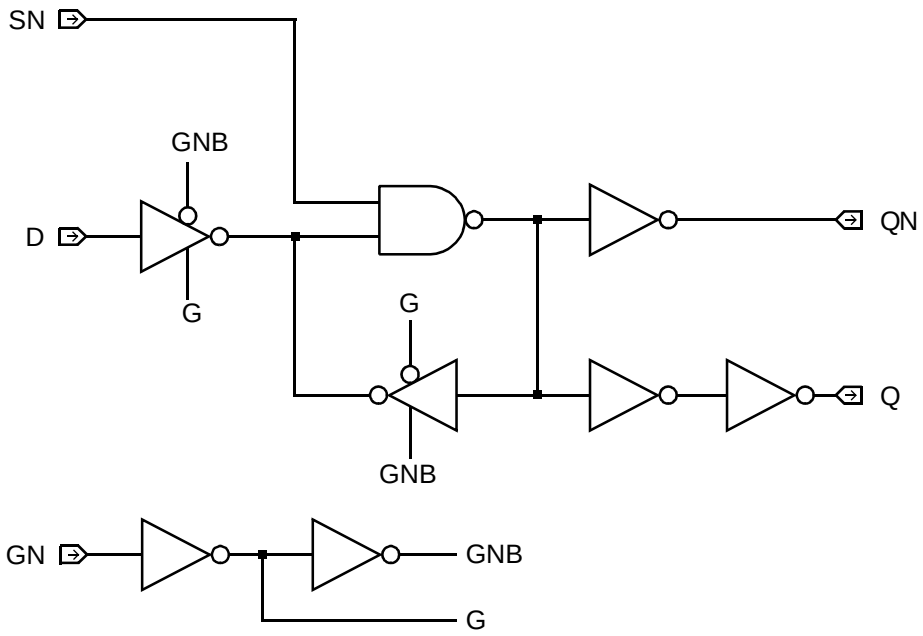
AMI500MXSC 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL651	DL652	DL654	DL656
Min GN Width	Low	t_w	0.870	0.913	0.854	0.853
Min SN Width	Low	t_w	0.808	0.867	0.794	0.791
Min D Setup		t_{su}	0.627	0.669	0.610	0.610
Min D Hold		t_h	0.198	0.198	0.198	0.198
Min SN Setup		t_{su}	0.317	0.360	0.299	0.297
Min SN Hold		t_h	0.671	0.670	0.675	0.674

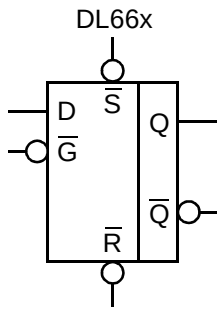
Logic Schematic



Description

DL66x is a family of transparent, buffered D latches with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DL66x *inst_name* (Q, QN, D, GN, RN, SN);

VHDL..... *inst_name*: DL66x port map (Q, QN, D, GN, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL661	DL662	DL664	DL666
D	1.1	1.1	1.0	1.0
GN	1.1	1.1	1.0	1.0
SN	1.0	1.0	2.0	2.0
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL661	4.8	1.810	10.8
DL662	4.8	2.133	13.0
DL664	7.2	3.640	25.1
DL666	8.0	4.321	30.5

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DL661	From: D To: Q	t_{PLH} t_{PHL}	1.078 1.197	1.376 1.463	1.733 1.811	2.151 2.239	2.495 2.602
	From: D To: QN	t_{PLH} t_{PHL}	1.001 0.955	1.319 1.301	1.687 1.678	2.108 2.098	2.449 2.431
	From: GN To: Q	t_{PLH} t_{PHL}	1.193 1.434	1.509 1.748	1.866 2.099	2.271 2.493	2.595 2.809
	From: GN To: QN	t_{PLH} t_{PHL}	1.262 1.074	1.579 1.405	1.947 1.782	2.371 2.210	2.715 2.555
	From: SN To: Q	t_{PLH} t_{PHL}	0.708 0.702	0.983 1.000	1.337 1.351	1.769 1.757	2.133 2.089
	From: SN To: QN	t_{PLH} t_{PHL}	0.523 0.582	0.841 0.943	1.199 1.318	1.617 1.734	1.968 2.075
	From: R To: Q	t_{PLH} t_{PHL}	1.126 1.042	1.414 1.341	1.770 1.692	2.194 2.099	2.547 2.430
	From: RN To: QN	t_{PLH} t_{PHL}	0.866 0.997	1.184 1.323	1.554 1.702	1.980 2.137	2.325 2.491
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DL662	From: D To: Q	t_{PLH} t_{PHL}	1.151 1.239	1.424 1.528	1.755 1.831	2.065 2.096	2.417 2.386
	From: D To: QN	t_{PLH} t_{PHL}	1.018 0.901	1.346 1.285	1.678 1.624	1.965 1.900	2.275 2.186
	From: GN To: Q	t_{PLH} t_{PHL}	1.291 1.497	1.557 1.805	1.873 2.107	2.167 2.363	2.500 2.638
	From: GN To: QN	t_{PLH} t_{PHL}	1.266 1.053	1.620 1.420	1.949 1.743	2.224 2.005	2.513 2.278
	From: SN To: Q	t_{PLH} t_{PHL}	0.762 0.733	1.068 1.018	1.396 1.331	1.688 1.611	2.008 1.920
	From: SN To: QN	t_{PLH} t_{PHL}	0.508 0.522	0.859 0.916	1.197 1.257	1.489 1.533	1.813 1.819
	From: RN To: Q	t_{PLH} t_{PHL}	1.199 1.095	1.505 1.371	1.821 1.675	2.097 1.948	2.396 2.250
	From: RN To: QN	t_{PLH} t_{PHL}	0.885 0.955	1.215 1.342	1.546 1.672	1.832 1.937	2.141 2.211

	Number of Equivalent Loads		1	19	38	56	75 (max)
DL664	From: D To: Q	t_{PLH} t_{PHL}	0.899 0.929	1.224 1.223	1.565 1.508	1.882 1.769	2.215 2.038
	From: D To: QN	t_{PLH} t_{PHL}	1.087 1.089	1.360 1.399	1.664 1.692	1.956 1.950	2.268 2.209
	From: GN To: Q	t_{PLH} t_{PHL}	1.066 1.124	1.346 1.449	1.685 1.725	1.986 1.980	2.273 2.248
	From: GN To: QN	t_{PLH} t_{PHL}	1.263 1.258	1.605 1.547	1.924 1.817	2.212 2.059	2.507 2.306
	From: SN To: Q	t_{PLH} t_{PHL}	0.456 0.512	0.747 0.854	1.070 1.128	1.378 1.378	1.703 1.643
	From: SN To: QN	t_{PLH} t_{PHL}	0.675 0.604	0.941 0.887	1.265 1.174	1.578 1.439	1.895 1.710
	From: RN To: Q	t_{PLH} t_{PHL}	0.764 0.678	1.106 0.992	1.431 1.280	1.720 1.542	2.011 1.813
	From: RN To: QN	t_{PLH} t_{PHL}	0.840 0.956	1.130 1.268	1.433 1.528	1.731 1.768	2.058 2.029
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DL666	From: D To: Q	t_{PLH} t_{PHL}	0.968 0.900	1.302 1.256	1.591 1.550	1.889 1.815	2.194 2.060
	From: D To: QN	t_{PLH} t_{PHL}	1.160 1.248	1.460 1.546	1.772 1.784	2.085 2.032	2.397 2.302
	From: GN To: Q	t_{PLH} t_{PHL}	1.078 1.149	1.401 1.476	1.717 1.758	2.024 2.017	2.326 2.262
	From: GN To: QN	t_{PLH} t_{PHL}	1.416 1.318	1.691 1.654	1.990 1.936	2.298 2.195	2.615 2.440
	From: SN To: Q	t_{PLH} t_{PHL}	0.462 0.522	0.767 0.851	1.078 1.141	1.381 1.410	1.674 1.668
	From: SN To: QN	t_{PLH} t_{PHL}	0.779 0.663	1.047 0.981	1.354 1.262	1.660 1.533	1.959 1.809
	From: RN To: Q	t_{PLH} t_{PHL}	0.822 0.681	1.120 1.033	1.428 1.320	1.735 1.577	2.042 1.815
	From: RN To: QN	t_{PLH} t_{PHL}	0.919 1.084	1.222 1.367	1.520 1.619	1.813 1.865	2.103 2.144

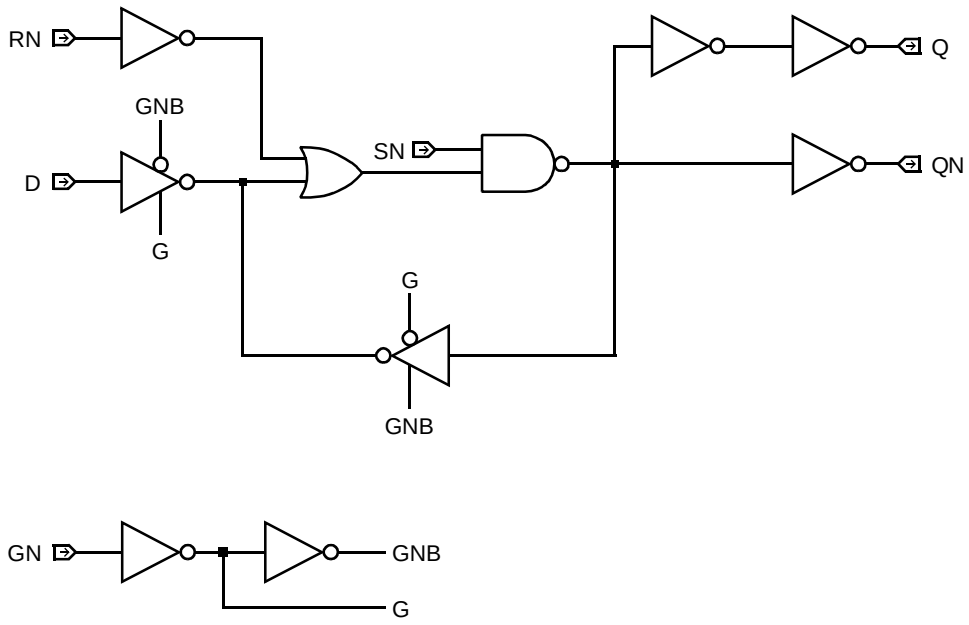
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL661	DL662	DL664	DL666
Min GN Width	Low	t_w	1.090	1.129	0.852	0.850
Min RN Width	Low	t_w	0.703	0.738	0.390	0.389
Min SN Width	Low	t_w	0.740	0.791	0.848	0.845
Min D Setup		t_{su}	0.817	0.854	0.610	0.608
Min D Hold		t_h	0.206	0.206	0.199	0.199
Min SN Setup		t_{su}	0.351	0.383	0.226	0.225
Min SN Hold		t_h	0.592	0.593	0.779	0.780
Min RN Setup		t_{su}	0.704	0.739	0.455	0.453
Min RN Hold		t_h	0.304	0.304	0.667	0.667

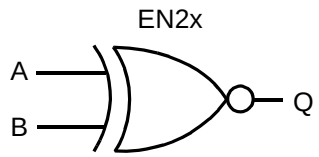
Logic Schematic



Description

EN2x is a family of 2-input gates which perform the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... EN2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EN2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EN21	EN22	EN23	EN24	EN26
A	2.0	3.8	3.9	3.7	3.8
B	2.0	3.8	3.7	3.7	3.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EN21	1.8	0.686	3.5
EN22	2.2	1.334	6.2
EN23	3.0	1.830	10.0
EN24	3.0	2.161	11.6
EN26	3.2	2.527	14.7

a. See page 2-13 for power equation.

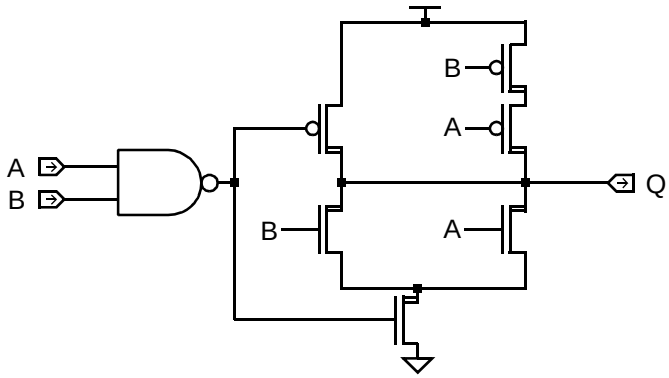
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

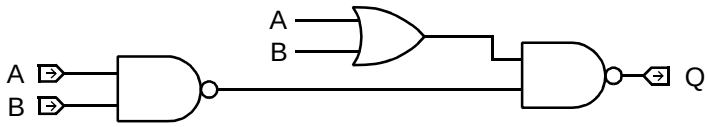
EN21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.465 0.285	0.630 0.494	0.874 0.780	1.035 0.968	1.276 1.244
EN22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.323 0.197	0.463 0.409	0.628 0.643	0.818 0.917	0.972 1.145
EN23	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.324 0.564	0.641 0.897	0.987 1.226	1.296 1.508	1.638 1.810
EN24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.382 0.611	0.676 0.978	0.972 1.265	1.264 1.521	1.579 1.783
EN26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.410 0.619	0.735 1.026	1.075 1.334	1.417 1.610	1.763 1.867

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



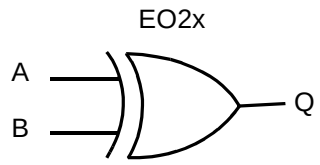
LOGICAL



Description

EO2x is a family of 2-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... EO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EO21	EO22	EO23	EO24	EO26
A	2.1	3.7	3.8	3.8	3.8
B	2.1	3.7	3.8	3.8	3.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO21	2.0	0.817	3.7
EO22	2.0	1.438	6.7
EO23	3.0	1.707	10.2
EO24	3.5	2.053	12.7
EO26	3.8	2.371	15.1

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

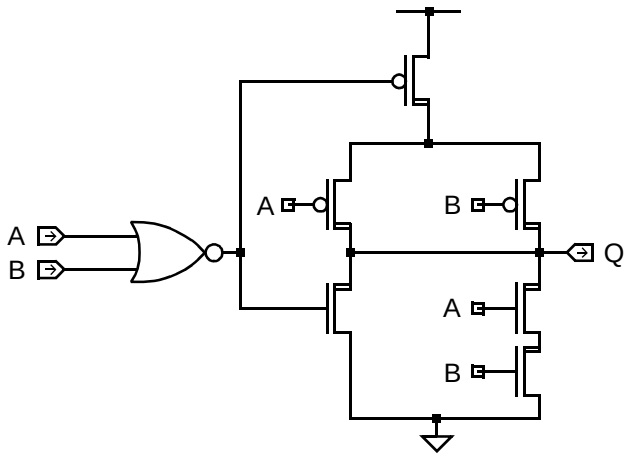
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

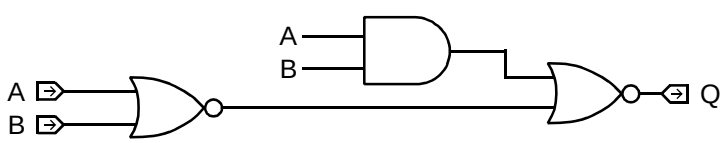
EO21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.502 0.321	0.755 0.557	1.135 0.903	1.390 1.135	1.773 1.468
EO22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.378 0.209	0.606 0.456	0.890 0.729	1.227 1.041	1.506 1.302
EO23	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.322 0.491	0.646 0.806	0.977 1.128	1.274 1.407	1.612 1.710
EO24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.385 0.501	0.658 0.853	0.941 1.127	1.230 1.386	1.546 1.663
EO26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.414 0.501	0.745 0.872	1.027 1.178	1.317 1.452	1.619 1.707

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



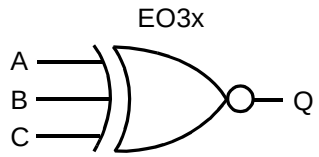
LOGICAL



Description

EO3x is a family of 3-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

HDL Syntax

Verilog ..... EO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: EO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	EO31	EO32	EO33	EO34	EO36
A	2.0	2.1	2.1	2.1	2.1
B	2.0	2.1	2.1	2.1	2.1
C	2.0	3.0	3.0	3.0	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO31	3.5	1.495	9.0
EO32	4.0	1.882	12.9
EO33	4.5	1.824	15.6
EO34	4.8	2.164	18.0
EO36	5.0	2.510	20.5

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

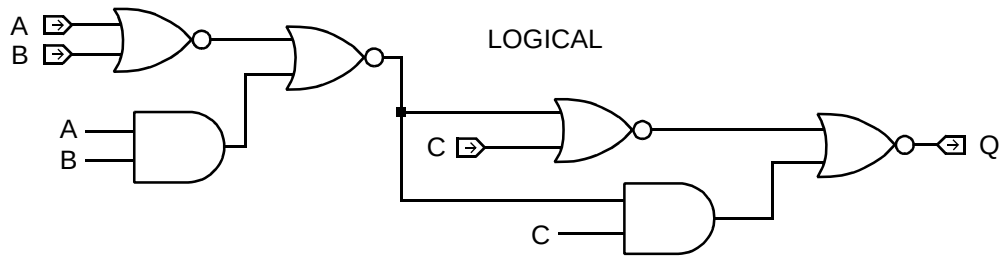
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

EO31	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.032 0.910	1.256 1.201	1.606 1.605	1.845 1.863	2.209 2.240
EO32	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.161 0.945	1.409 1.205	1.691 1.511	2.012 1.847	2.270 2.113
EO33	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.987 1.341	1.304 1.652	1.636 1.959	1.928 2.222	2.248 2.504
EO34	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.020 1.296	1.377 1.667	1.695 1.969	1.971 2.215	2.246 2.448
EO36	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.140 1.367	1.424 1.711	1.686 2.003	2.018 2.272	2.298 2.528

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

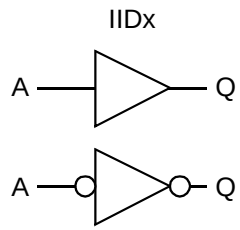
Logic Schematic



Description

IIDx is a family of non-inverting clock drivers with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... IIDx *inst_name* (Q, A);

VHDL..... *inst_name*: IIDx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads				
	IID1	IID2	IID3	IID4	IID6
A	1.0	1.0	1.8	1.8	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IID1	1.0	0.411	2.2
IID2	1.0	0.585	3.4
IID3	1.2	0.933	4.8
IID4	1.8	1.123	5.9
IID6	1.8	1.475	8.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

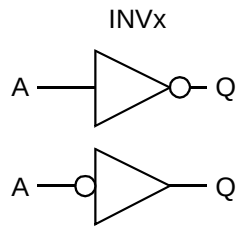
IID1	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.317 0.309	0.623 0.596	0.987 0.928	1.413 1.334	1.762 1.692
IID2	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.292 0.291	0.611 0.597	0.944 0.898	1.245 1.161	1.587 1.454
IID3	**Number of Equivalent Loads**		**1**	**14**	**28**	**43**	**57 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.225 0.203	0.505 0.493	0.811 0.761	1.141 1.042	1.452 1.307
IID4	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.226 0.242	0.540 0.530	0.850 0.791	1.148 1.041	1.462 1.309
IID6	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.284 0.243	0.578 0.583	0.880 0.829	1.180 1.092	1.477 1.372

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

INVx is a family of inverters which perform the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

HDL Syntax

Verilog ..... INVx *inst_name* (Q, A);

VHDL..... *inst_name*: INVx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads					
	INV1	INV2	INV3	INV4	INV5	INV6
A	1.0	1.8	2.9	3.9	4.7	5.4

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
INV1	0.8	0.223	0.6
INV2	1.0	0.408	1.0
INV3	1.0	0.585	1.3
INV4	1.2	0.760	1.6
INV5	1.2	0.932	2.0
INV6	1.5	1.113	2.2

a. See page 2-13 power equation

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

INV1	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.087 0.205	0.432 0.548	0.811 0.882	1.229 1.265	1.571 1.602
INV2	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.115 0.171	0.435 0.493	0.749 0.765	1.036 1.013	1.367 1.313
INV3	**Number of Equivalent Loads**		**1**	**14**	**28**	**43**	**57 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.072 0.102	0.410 0.441	0.697 0.715	1.000 0.987	1.302 1.246
INV4	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.118 0.163	0.397 0.449	0.693 0.715	0.968 0.976	1.252 1.240
INV5	**Number of Equivalent Loads**		**1**	**24**	**47**	**70**	**94 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.076 0.055	0.392 0.411	0.683 0.648	0.976 0.903	1.293 1.211
INV6	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.043 0.078	0.416 0.395	0.709 0.691	1.006 0.968	1.341 1.214

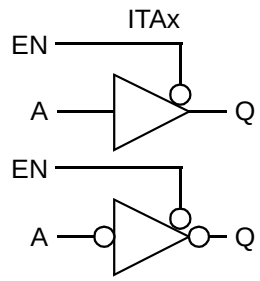
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ITAx is a family of non-inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

HDL Syntax

Verilog ..... ITAx *inst_name* (Q, A, EN);

VHDL..... *inst_name*: ITAx port map (Q, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITA1	ITA2	ITA4	ITA6
A	1.0	1.0	1.0	1.0
EN	1.5	1.9	2.8	3.8
Q	0.6	1.0	1.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITA1	2.0	0.631	3.7
ITA2	2.0	0.807	5.7
ITA4	2.0	1.144	9.5
ITA6	2.8	1.528	14.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITA1	Number of Equivalent Loads		1	16	32	47	63 (max)
	From: A To: Q	t_{PLH} t_{PHL}	0.456 0.413	2.343 2.250	4.364 4.213	6.259 6.054	8.280 8.018
	From: EN To: Q	t_{ZH} t_{ZL}	0.268 0.315	2.148 2.170	4.136 4.133	6.008 5.974	8.014 7.941
ITA2	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: A To: Q	t_{PLH} t_{PHL}	0.406 0.318	2.008 1.730	3.674 3.189	5.349 4.646	7.032 6.102
	From: EN To: Q	t_{ZH} t_{ZL}	0.166 0.230	1.875 1.689	3.412 3.134	5.031 4.584	6.791 6.059
ITA4	Number of Equivalent Loads		1	52	105	158	210 (max)
	From: A To: Q	t_{PLH} t_{PHL}	0.443 0.403	1.949 1.778	3.528 3.150	5.108 4.523	6.657 5.883
	From: EN To: Q	t_{ZH} t_{ZL}	0.196 0.236	1.664 1.626	3.164 3.013	4.724 4.377	6.307 5.702
ITA6	Number of Equivalent Loads		1	77	154	231	308 (max)
	From: A To: Q	t_{PLH} t_{PHL}	0.509 0.525	2.014 1.911	3.532 3.253	5.048 4.585	6.567 5.915
	From: EN To: Q	t_{ZH} t_{ZL}	0.142 0.297	1.725 1.716	3.166 3.033	4.630 4.353	6.141 5.697

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

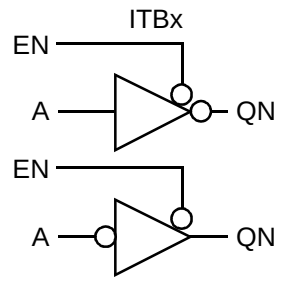
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ITA1	ITA2	ITA4	ITA6
EN	Q	t_{HZ} t_{LZ}	0.212 0.219	0.210 0.254	0.206 0.336	0.202 0.422

Description

ITBx is a family of inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITBx *inst_name* (QN, A, EN);

VHDL..... *inst_name*: ITBx port map (QN, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITB1	ITB2	ITB4	ITB6
A	1.0	1.9	3.7	5.6
EN	1.5	1.9	2.8	3.7
QN	0.6	0.9	1.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITB1	1.2	0.424	2.1
ITB2	1.2	0.591	3.2
ITB4	1.8	0.956	5.3
ITB6	2.2	1.333	8.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITB1	**Number of Equivalent Loads**		**1**	**16**	**32**	**47**	**63 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.296 0.324	2.218 2.181	4.204 4.106	6.077 5.938	8.123 7.939
	From: EN To: QN	t_{ZH} t_{ZL}	0.386 0.347	2.093 2.168	4.011 4.127	5.882 5.973	7.813 7.949
ITB2	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.215 0.136	1.804 1.646	3.463 3.093	5.128 4.534	6.799 6.006
	From: EN To: QN	t_{ZH} t_{ZL}	0.162 0.231	1.827 1.668	3.426 3.144	5.037 4.618	6.717 6.093
ITB4	**Number of Equivalent Loads**		**1**	**52**	**105**	**158**	**210 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.134 0.124	1.695 1.563	3.262 2.940	4.835 4.312	6.395 5.671
	From: EN To: QN	t_{ZH} t_{ZL}	0.181 0.238	1.652 1.641	3.175 3.028	4.729 4.412	6.280 5.782
ITB6	**Number of Equivalent Loads**		**1**	**77**	**154**	**231**	**308 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.115 0.159	1.678 1.533	3.191 2.867	4.676 4.197	6.145 5.528
	From: EN To: QN	t_{ZH} t_{ZL}	0.057 0.265	1.710 1.706	3.249 3.034	4.687 4.356	6.058 5.696

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

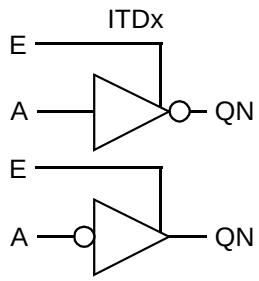
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			ITB1	**ITB2**	**ITB4**	**ITB6**
EN	QN	t_{HZ} t_{LZ}	0.212 0.223	0.210 0.263	0.207 0.334	0.202 0.415

Description

ITD1x is a family of inverting internal tristate buffers with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITDx *inst_name* (QN, A, E);

VHDL..... *inst_name*: ITDx port map (QN, A, E);

Pin Loading

Pin Name	Equivalent Loads			
	ITD1	ITD2	ITD4	ITD6
A	1.0	1.8	3.7	5.6
E	1.5	1.9	2.8	3.8
QN	0.6	0.9	1.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITD1	1.2	0.423	2.1
ITD2	1.5	0.600	3.1
ITD4	1.8	0.955	5.2
ITD6	2.2	1.329	7.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITD1	**Number of Equivalent Loads**		**1**	**16**	**32**	**47**	**63 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.288 0.319	2.191 2.231	4.207 4.173	6.092 6.000	8.100 7.983
	From: E To: QN	t_{ZH} t_{ZL}	0.308 0.155	2.170 2.277	4.179 4.164	6.076 5.914	8.108 7.874
ITD2	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.211 0.228	1.812 1.665	3.463 3.099	5.119 4.554	6.783 6.037
	From: E To: QN	t_{ZH} t_{ZL}	0.233 0.225	1.848 1.707	3.492 3.071	5.149 4.446	6.836 5.859
ITD4	**Number of Equivalent Loads**		**1**	**52**	**105**	**158**	**210 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.153 0.156	1.696 1.554	3.293 2.904	4.880 4.264	6.429 5.626
	From: E To: QN	t_{ZH} t_{ZL}	0.214 0.195	1.751 1.630	3.337 2.949	4.926 4.304	6.492 5.684
ITD6	**Number of Equivalent Loads**		**1**	**77**	**154**	**231**	**308 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.146 0.118	1.658 1.534	3.153 2.835	4.671 4.153	6.226 5.514
	From: E To: QN	t_{ZH} t_{ZL}	0.213 0.108	1.758 1.691	3.285 2.909	4.796 4.152	6.298 5.480

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

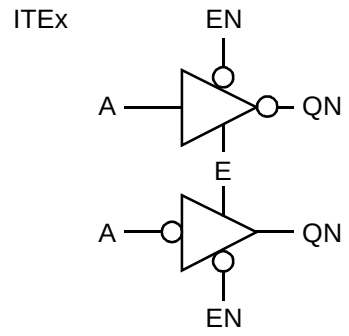
Delay (ns) From	To	Parameter	Cell ITD1	ITD2	ITD4	ITD6
E	QN	t_{HZ} t_{LZ}	0.216 0.085	0.248 0.083	0.360 0.083	0.455 0.083

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ITEx is a family of two-phase enable inverting internal tristate buffers.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

IL = Illegal

HDL Syntax

Verilog ..... ITEx *inst_name* (QN, A, E, EN);

VHDL..... *inst_name*: ITEx port map (QN, A, E, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITE1	ITE2	ITE4	ITE6
A	1.0	1.8	3.7	5.6
E	0.5	1.0	1.9	2.8
EN	0.5	0.9	1.8	2.7
QN	0.6	1.0	2.0	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITE1	1.0	0.235	1.0
ITE2	1.0	0.410	1.8
ITE4	1.5	0.784	3.5
ITE6	2.0	1.142	4.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITE1	Number of Equivalent Loads		1	16	32	47	63 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.297 0.223	2.214 2.158	4.223 4.101	6.110 5.915	8.138 7.887
	From: EN To: QN	t_{ZH}	0.156	2.236	4.235	6.088	8.094
	From: E To: QN	t_{ZL}	0.384	2.262	4.175	5.945	7.827
ITE2	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.223 0.177	1.826 1.657	3.477 3.110	5.142 4.560	6.828 6.022
	From: EN To: QN	t_{ZH}	0.239	1.920	3.522	5.139	6.795
	From: E To: QN	t_{ZL}	0.201	1.769	3.186	4.623	6.122
ITE4	Number of Equivalent Loads		1	52	105	158	210 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.180 0.149	1.685 1.536	3.233 2.900	4.785 4.269	6.318 5.627
	From: EN To: QN	t_{ZH}	0.205	1.795	3.299	4.824	6.359
	From: E To: QN	t_{ZL}	0.240	1.636	2.961	4.283	5.589
ITE6	Number of Equivalent Loads		1	77	154	231	308 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.163 0.161	1.664 1.535	3.151 2.805	4.658 4.125	6.197 5.519
	From: EN To: QN	t_{ZH}	0.164	1.746	3.275	4.774	6.254
	From: E To: QN	t_{ZL}	0.238	1.739	3.068	4.392	5.742

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

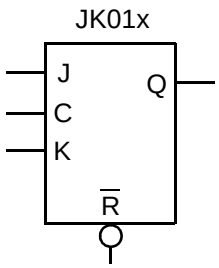
Delay (ns) From	To	Parameter	Cell			
			ITE1	ITE2	ITE4	ITE6
EN	QN	t_{HZ}	0.213	0.211	0.207	0.203
E	QN	t_{LZ}	0.085	0.084	0.084	0.082

JK01x

Description

JK01x is a family of static, master-slave JK flip-flops. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)
L	X	X	X	L
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK01x *inst_name* (Q, C, J, K, RN);

VHDL..... *inst_name*: JK01x port map (Q, C, J, K, RN);

Pin Loading

Pin Name	Equivalent Loads	
	JK011	JK012
J	1.1	1.1
K	1.1	1.1
C	1.0	1.0
RN	1.1	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK011	6.8	2.499	20.2
JK012	7.0	2.749	21.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	8	11 (max)
JK011	From: C To: Q	t_{PLH} t_{PHL}	1.269 1.135	1.510 1.349	1.874 1.626	2.117 1.797	2.484 2.040
	From: RN To: Q	t_{PHL}	0.521	0.686	0.901	1.056	1.285
	Number of Equivalent Loads		**1**	**5**	**10**	**16**	**21 (max)**
JK012	From: C To: Q	t_{PLH} t_{PHL}	1.142 0.993	1.395 1.231	1.677 1.454	1.994 1.680	2.248 1.849
	From: RN To: Q	t_{PHL}	0.443	0.618	0.788	0.966	1.125

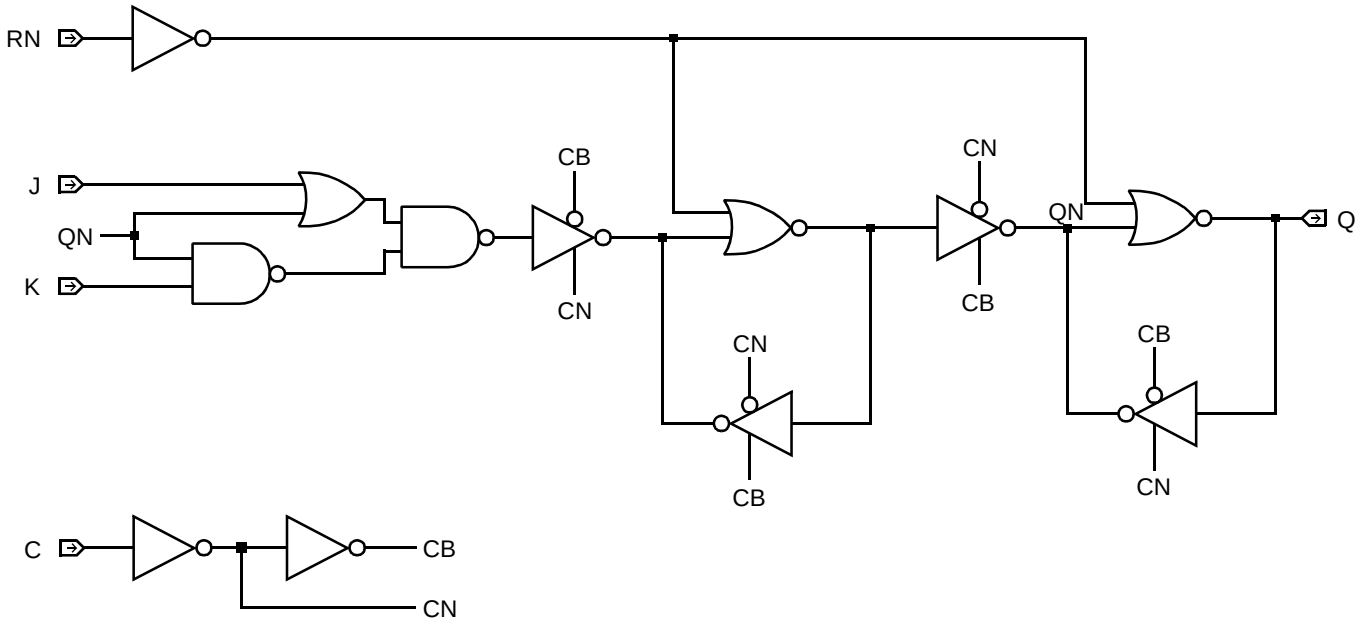
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK011	JK012
Min C Width	High	t_w	1.278	1.151
Min C Width	Low	t_w	1.043	1.032
Min RN Width	Low	t_w	1.020	1.072
Min J Setup		t_{su}	1.010	1.013
Min J Hold		t_h	0.290	0.282
Min K Setup		t_{su}	0.860	0.850
Min K Hold		t_h	0.290	0.282
Min RN Setup		t_{su}	0.474	0.513
Min RN Hold		t_h	0.663	0.649

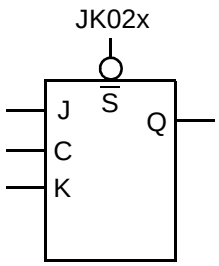
Logic Schematic



Description

JK02x is a family of static, master-slave JK flip-flops. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)
L	X	X	X	H
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK02x *inst_name* (Q, C, J, K, SN);

VHDL..... *inst_name*: JK02x port map (Q, C, J, K, SN);

Pin Loading

Pin Name	Equivalent Loads	
	JK021	JK022
J	1.0	1.0
K	1.0	1.0
C	1.0	1.0
SN	2.2	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK021	6.2	2.382	16.5
JK022	6.2	2.581	17.3

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	8	11 (max)
JK021	From: C To: Q	t_{PLH} t_{PHL}	1.144 1.108	1.342 1.357	1.602 1.693	1.763 1.903	1.992 2.207
	From: SN To: Q	t_{PLH}	0.311	0.483	0.686	0.849	1.095
	Number of Equivalent Loads		**1**	**5**	**10**	**16**	**21 (max)**
JK022	From: C To: Q	t_{PLH} t_{PHL}	1.066 0.970	1.235 1.229	1.441 1.497	1.684 1.787	1.884 2.012
	From: SN To: Q	t_{PLH}	0.165	0.334	0.541	0.742	0.934

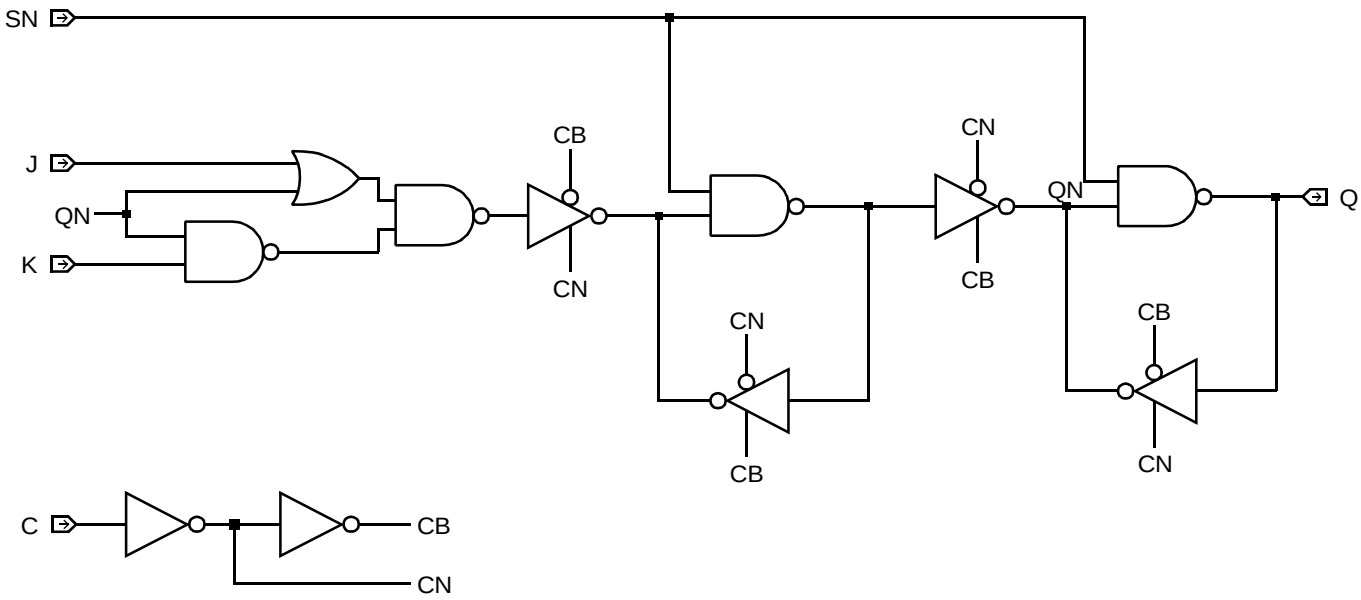
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK021	JK022
Min C Width	High	t_w	1.134	1.070
Min C Width	Low	t_w	0.975	0.999
Min SN Width	Low	t_w	0.798	1.142
Min J Setup		t_{su}	0.975	0.997
Min J Hold		t_h	0.261	0.264
Min K Setup		t_{su}	0.793	0.815
Min K Hold		t_h	0.261	0.264
Min SN Setup		t_{su}	0.261	0.270
Min SN Hold		t_h	0.843	0.864

Logic Schematic



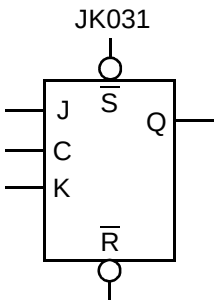
JK031

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

JK031 is a static, master-slave JK flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)
L	L	X	X	X	IL
L	H	X	X	X	L
H	L	X	X	X	H
H	H	L	L	↑	NC
H	H	L	H	↑	L
H	H	H	L	↑	H
H	H	H	H	↑	$\overline{Q(n)}$

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	1.0
SN	2.3
RN	2.3

Equivalent Gates 8.5

HDL Syntax

Verilog ..... JK031 *inst_name* (Q, C, J, K, RN, SN);

VHDL..... *inst_name*: JK031 port map (Q, C, J, K, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.734	nA
EQL_{pd}	21.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	1.212 1.192	1.396 1.455	1.658 1.790	1.828 1.993	2.077 2.280
RN	Q	t_{PHL}	1.384	1.640	1.977	2.187	2.486
SN	Q	t_{PLH}	0.283	0.476	0.721	0.857	1.101

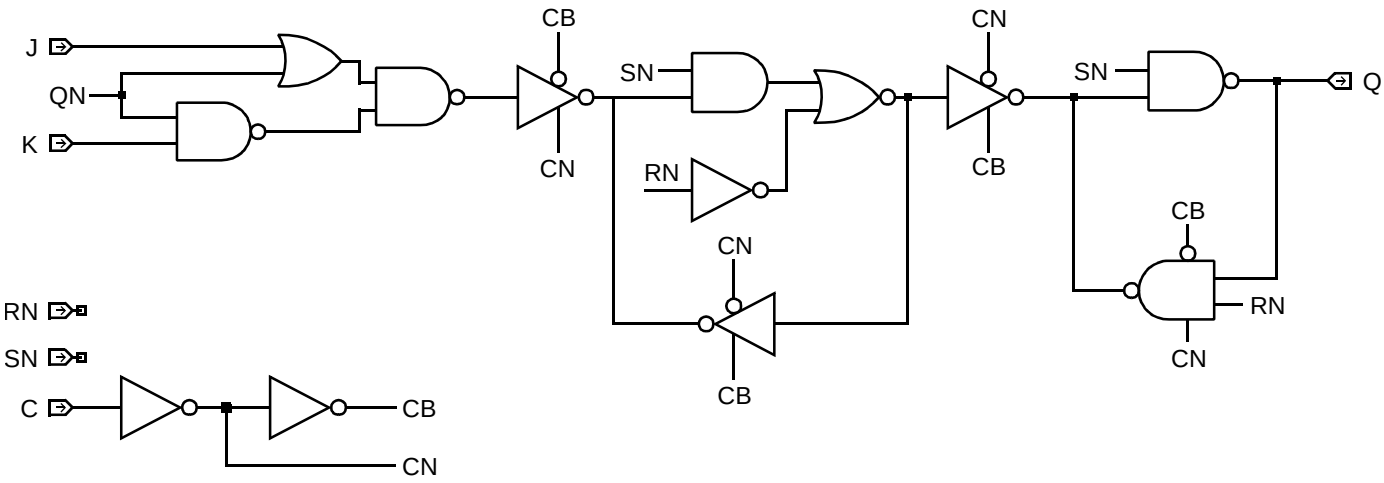
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	1.207
Min C Width	Low	t_w	1.117
Min RN Width	Low	t_w	1.380
Min SN Width	Low	t_w	0.963
Min J Setup		t_{su}	1.087
Min J Hold		t_h	0.276
Min K Setup		t_{su}	0.903
Min K Hold		t_h	0.276
Min RN Setup		t_{su}	0.440
Min RN Hold		t_h	0.633
Min SN Setup		t_{su}	0.354
Min SN Hold		t_h	0.900

Logic Schematic



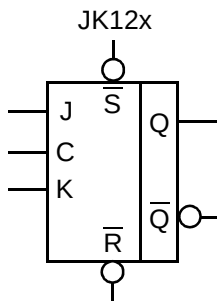
JK12x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

JK12x is a family of static, master-slave JK flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... JK12x *inst_name* (Q, QN, C, J, K, RN, SN);

VHDL..... *inst_name*: JK12x port map (Q, QN, C, J, K, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	JK121	JK122	JK124	JK126
J	1.0	1.0	1.0	1.0
K	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.4	2.2	2.3	2.3
RN	2.2	1.1	1.1	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK121	9.2	3.096	24.5
JK122	9.2	3.670	30.5
JK124	9.8	4.307	34.3
JK126	10.2	5.066	40.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
JK121	From: C To: Q	t_{PLH} t_{PHL}	1.183 1.128	1.471 1.554	1.844 1.978	2.300 2.426	2.684 2.770
	From: C To: QN	t_{PLH} t_{PHL}	1.424 1.526	1.724 1.808	2.085 2.173	2.507 2.621	2.853 2.998
	From: RN To: Q	t_{PHL}	1.332	1.775	2.199	2.635	2.966
	From: RN To: QN	t_{PLH}	1.602	1.883	2.242	2.679	3.047
	From: SN To: Q	t_{PLH}	1.176	1.529	1.906	2.321	2.648
	From: SN To: QN	t_{PHL}	0.510	0.846	1.213	1.637	1.989
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
JK122	From: C To: Q	t_{PLH} t_{PHL}	1.730 1.437	1.966 1.780	2.287 2.100	2.602 2.368	2.974 2.651
	From: C To: QN	t_{PLH} t_{PHL}	0.949 1.083	1.251 1.388	1.574 1.701	1.860 1.974	2.175 2.270
	From: RN To: Q	t_{PHL}	1.059	1.399	1.720	1.988	2.274
	From: RN To: QN	t_{PLH}	1.947	2.259	2.582	2.863	3.169
	From: SN To: Q	t_{PLH}	0.711	1.038	1.377	1.673	2.002
	From: SN To: QN	t_{PHL}	1.336	1.625	1.927	2.192	2.480

AMI500MXSC 0.5 micron CMOS Standard Cell

	Number of Equivalent Loads		1	19	38	56	75 (max)
JK124	From: C To: Q	t_{PLH} t_{PHL}	1.793 1.469	2.112 1.860	2.424 2.141	2.705 2.386	2.992 2.625
	From: C To: QN	t_{PLH} t_{PHL}	0.993 1.145	1.294 1.457	1.597 1.751	1.879 2.024	2.173 2.308
	From: RN To: Q	t_{PHL}	1.045	1.454	1.764	2.016	2.262
	From: RN To: QN	t_{PLH}	2.013	2.315	2.615	2.890	3.176
	From: SN To: Q	t_{PLH}	0.739	1.085	1.393	1.683	2.000
	From: SN To: QN	t_{PHL}	1.331	1.732	2.017	2.263	2.511
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
JK126	From: C To: Q	t_{PLH} t_{PHL}	1.923 1.575	2.242 2.048	2.544 2.357	2.836 2.610	3.120 2.829
	From: C To: QN	t_{PLH} t_{PHL}	1.005 1.280	1.343 1.656	1.667 1.963	1.979 2.240	2.284 2.501
	From: RN To: Q	t_{PHL}	1.165	1.617	1.928	2.198	2.441
	From: RN To: QN	t_{PLH}	1.519	1.810	2.113	2.418	2.723
	From: SN To: Q	t_{PLH}	0.860	1.158	1.482	1.794	2.091
	From: SN To: QN	t_{PHL}	1.093	1.484	1.780	2.044	2.289

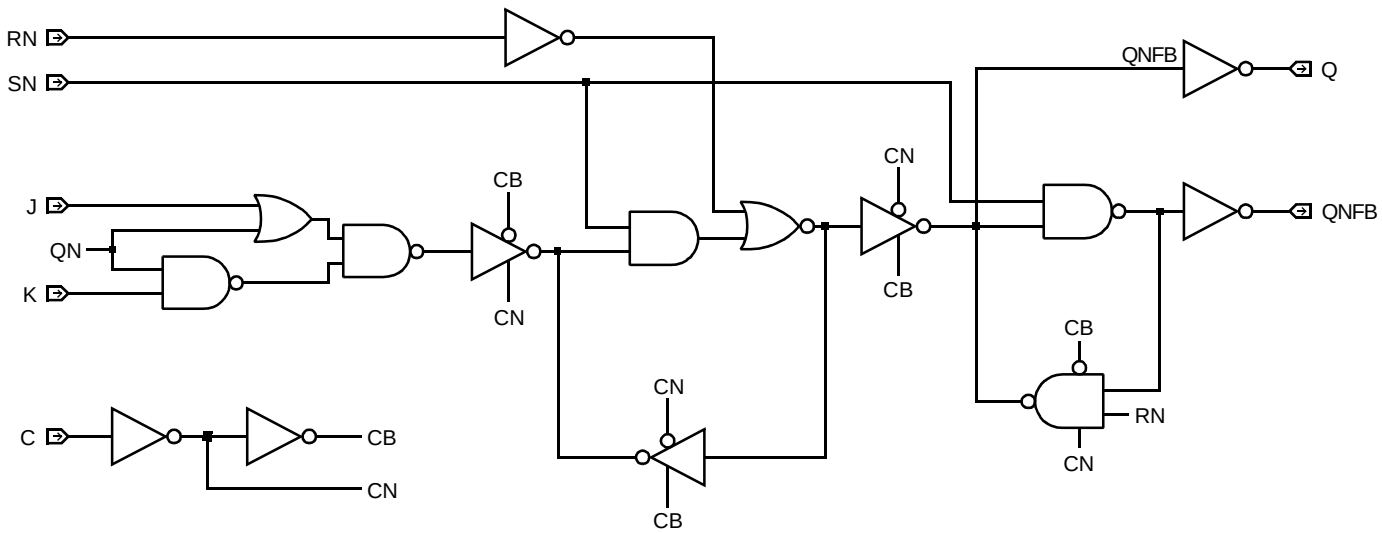
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			JK121	JK122	JK124	JK126
Min C Width	High	t_w	1.246	1.100	1.073	1.159
Min C Width	Low	t_w	1.118	1.049	1.049	1.049
Min RN Width	Low	t_w	1.426	1.068	1.070	1.068
Min SN Width	Low	t_w	0.954	0.943	0.912	0.757
Min J Setup		t_{su}	1.087	1.049	1.049	1.049
Min J Hold		t_h	0.275	0.262	0.262	0.271
Min K Setup		t_{su}	0.903	0.883	0.883	0.883
Min K Hold		t_h	0.275	0.262	0.262	0.271
Min RN Setup		t_{su}	0.439	0.562	0.564	0.562
Min RN Hold		t_h	0.632	0.617	0.617	0.627
Min SN Setup		t_{su}	0.354	0.320	0.320	0.320
Min SN Hold		t_h	0.899	0.859	0.858	0.876

Logic Schematic

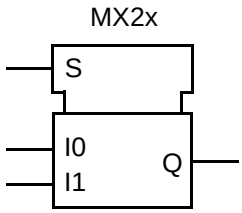


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

MX2x is a family of two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

HDL Syntax

Verilog ..... MX2x *inst_name* (Q, I0, I1, S);

VHDL..... *inst_name*: MX2x port map (Q, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MX21	MX22	MX24	MX26
I0	1.0	1.0	2.0	2.0
I1	1.0	1.0	2.0	2.0
S	1.6	1.6	4.0	4.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX21	2.0	0.714	4.6
MX22	2.0	0.888	5.8
MX24	3.2	1.880	11.2
MX26	3.5	2.242	14.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
MX21	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.445 0.538	0.755 0.866	1.122 1.235	1.549 1.650	1.898 1.983
	From: S To: Q	t_{PLH} t_{PHL}	0.638 0.786	0.953 1.122	1.330 1.492	1.765 1.904	2.118 2.231
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
MX22	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.473 0.525	0.785 0.906	1.125 1.246	1.428 1.529	1.763 1.829
	From: S To: Q	t_{PLH} t_{PHL}	0.671 0.782	0.992 1.151	1.337 1.491	1.643 1.773	1.980 2.070
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
MX24	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.443 0.429	0.754 0.824	1.059 1.118	1.356 1.376	1.663 1.641
	From: S To: Q	t_{PLH} t_{PHL}	0.478 0.590	0.794 0.983	1.118 1.285	1.416 1.540	1.722 1.791
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
MX26	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.471 0.527	0.812 0.927	1.117 1.224	1.413 1.504	1.715 1.779
	From: S To: Q	t_{PLH} t_{PHL}	0.527 0.615	0.863 1.049	1.174 1.372	1.482 1.645	1.791 1.896

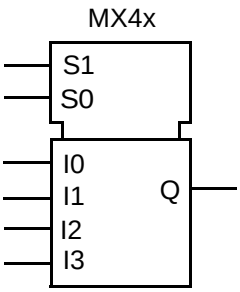
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

MX4x is a family of four-to-one digital multiplexers.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

HDL Syntax

Verilog ..... MX4x *inst_name* (Q, I0, I1, I2, I3, S0, S1);

VHDL..... *inst_name*: MX4x port map (Q, I0, I1, I2, I3, S0, S1);

Pin Loading

Pin Name	Equivalent Loads			
	MX41	MX42	MX44	MX46
I0	1.1	1.1	1.1	1.1
I1	1.1	1.1	1.1	1.1
I2	1.1	1.1	1.1	1.1
I3	1.0	1.0	1.0	1.0
S0	3.5	3.6	3.6	3.7
S1	3.5	2.5	2.4	2.4

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX41	4.5	1.459	12.6
MX42	5.8	2.466	18.0
MX44	6.5	3.084	23.4
MX46	6.8	3.420	26.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

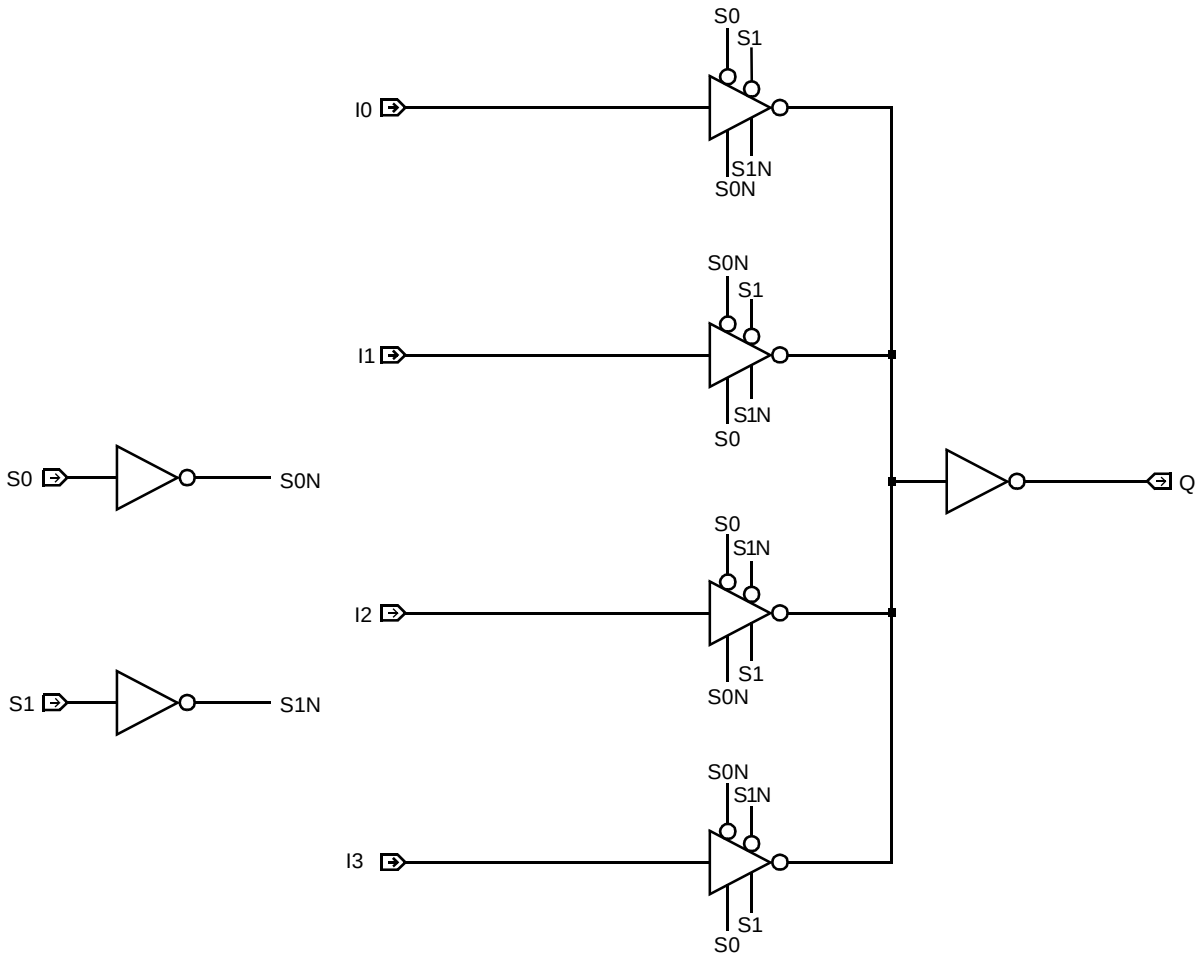
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
MX41	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.803 1.236	1.154 1.702	1.532 2.141	1.950 2.589	2.279 2.926
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.970 1.509	1.325 1.948	1.700 2.381	2.109 2.836	2.429 3.184
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
MX42	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.862 0.940	1.174 1.240	1.504 1.546	1.794 1.812	2.113 2.099
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.038 1.198	1.336 1.530	1.665 1.836	1.962 2.090	2.291 2.358
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
MX44	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.893 0.983	1.214 1.271	1.538 1.528	1.840 1.784	2.154 2.085
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.118 1.260	1.438 1.546	1.735 1.818	2.014 2.086	2.307 2.396
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
MX46	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.928 0.990	1.244 1.345	1.562 1.614	1.871 1.878	2.174 2.137
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.153 1.247	1.430 1.608	1.746 1.911	2.073 2.177	2.409 2.421

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

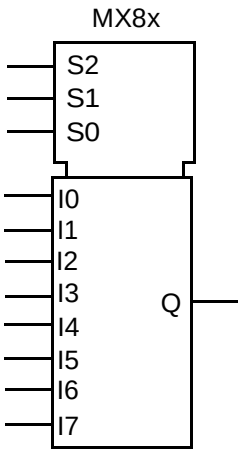
Logic Schematic



Description

MX8x is a family of eight-to-one digital multiplexers.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

HDL Syntax

Verilog ..... MX8x *inst_name* (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

VHDL..... *inst_name*: MX8x port map (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads			
	MX81	MX82	MX84	MX86
I0	1.1	1.1	1.0	1.1
I1	1.1	1.1	1.1	1.1
I2	1.0	1.0	1.1	1.0
I3	1.2	1.2	1.2	1.1
I4	1.0	1.0	1.0	1.0
I5	1.1	1.0	1.1	1.1
I6	1.0	1.0	1.0	1.0
I7	1.1	1.1	1.1	1.1
S0	6.2	6.3	6.3	6.5
S1	3.7	3.8	3.9	4.0
S2	2.4	2.5	3.4	3.4

AMI500MXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX81	9.5	3.555	32.0
MX82	11.0	4.757	41.3
MX84	10.8	4.456	40.8
MX86	12.0	4.869	44.0

a. See page 2-13 for power equation.

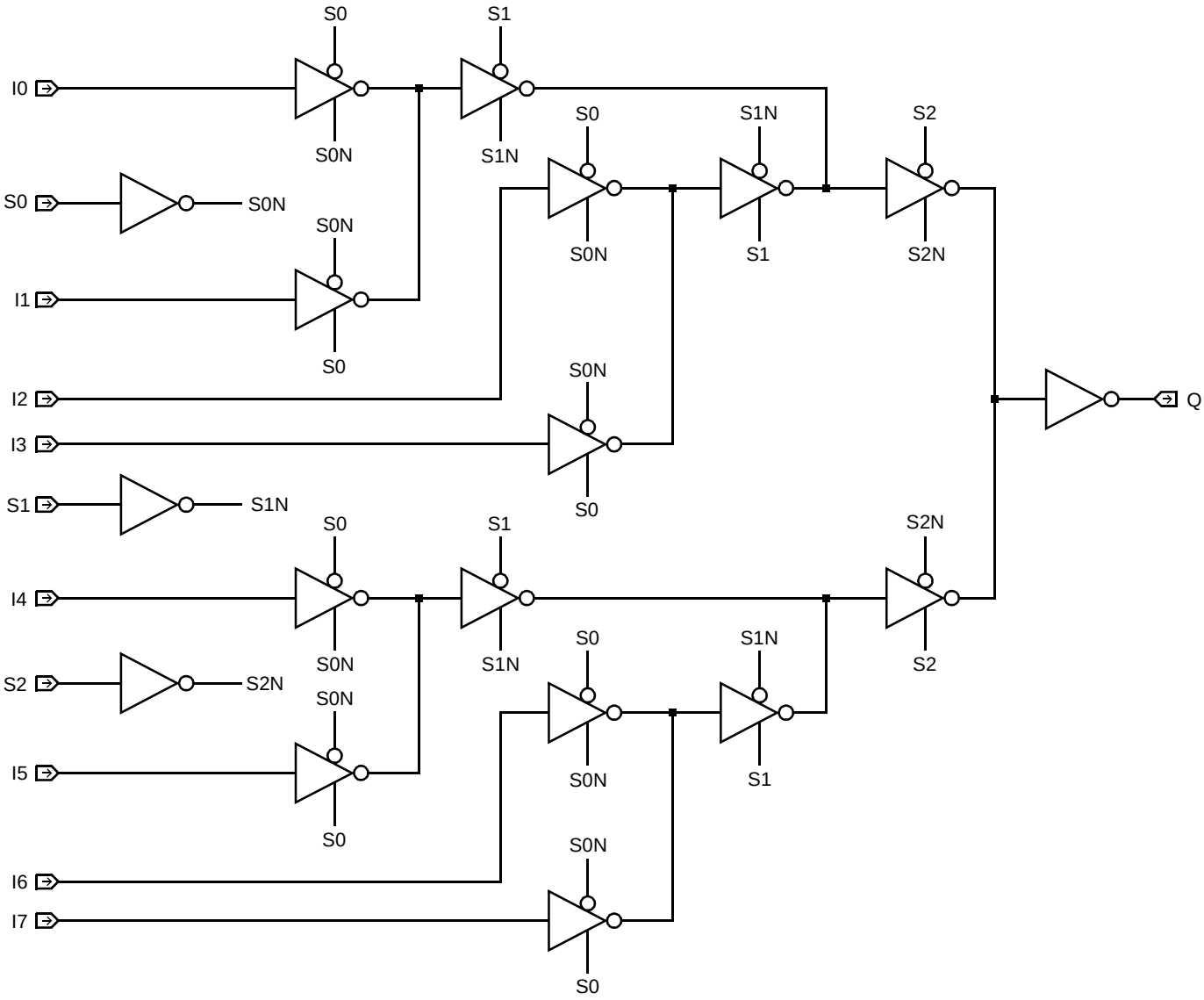
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

MX81	Number of Equivalent Loads		1	5	10	16	21 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	1.204 1.309	1.520 1.663	1.888 2.044	2.311 2.466	2.654 2.798
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.585 1.673	1.878 2.025	2.243 2.406	2.682 2.829	3.047 3.164
MX82	Number of Equivalent Loads		1	10	20	29	39 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	1.235 1.261	1.423 1.543	1.620 1.805	1.791 2.024	1.979 2.255
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.618 1.607	1.807 1.908	2.002 2.167	2.172 2.375	2.358 2.590
MX84	Number of Equivalent Loads		1	19	38	56	75 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	1.317 1.280	1.594 1.681	1.896 1.977	2.186 2.218	2.494 2.447
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.696 1.628	2.047 1.967	2.344 2.285	2.601 2.572	2.857 2.864
MX86	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	1.242 1.266	1.546 1.775	1.864 2.135	2.183 2.444	2.503 2.725
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.668 1.646	1.971 2.105	2.253 2.466	2.524 2.787	2.786 3.086

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic

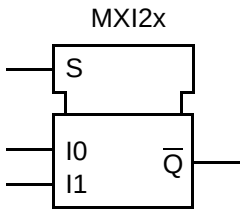


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

MXI2x is a family of inverting two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	QN
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

HDL Syntax

Verilog ..... MXI2x *inst_name* (QN, I0, I1, S);

VHDL..... *inst_name*: MXI2x port map (QN, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MXI21	MXI22	MXI24	MXI26
I0	1.0	1.0	1.1	1.1
I1	1.0	1.0	1.0	1.0
S	1.6	1.6	2.2	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MXI21	2.5	0.910	6.1
MXI22	2.5	1.084	7.3
MXI24	3.2	1.815	11.6
MXI26	3.8	2.440	16.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
MXI21	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.638 0.637	0.922 0.925	1.280 1.279	1.711 1.695	2.072 2.035
	From: S To: QN	t_{PLH} t_{PHL}	0.880 0.809	1.193 1.103	1.553 1.454	1.965 1.864	2.298 2.200
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
MXI22	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.637 0.604	0.932 0.904	1.270 1.217	1.580 1.491	1.927 1.790
	From: S To: QN	t_{PLH} t_{PHL}	0.907 0.800	1.211 1.103	1.529 1.415	1.817 1.687	2.147 1.983
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
MXI24	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.598 0.666	0.931 1.012	1.246 1.255	1.535 1.498	1.833 1.780
	From: S To: QN	t_{PLH} t_{PHL}	0.821 0.712	1.147 1.083	1.431 1.398	1.736 1.664	2.046 1.928
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
MXI26	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.524 0.571	0.843 0.907	1.160 1.173	1.471 1.426	1.777 1.686
	From: S To: QN	t_{PLH} t_{PHL}	0.753 0.674	1.065 0.988	1.365 1.256	1.666 1.509	2.013 1.754

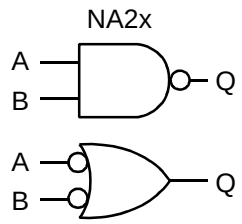
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA2x is a family of 2-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... NA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NA21	NA22	NA23	NA24	NA26
A	1.0	1.8	3.7	1.8	1.8
B	1.0	1.8	3.7	1.8	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA21	1.0	0.346	0.9
NA22	1.2	0.642	1.5
NA23	2.0	1.230	2.7
NA24	2.2	1.643	9.2
NA26	2.5	1.979	11.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.165 0.270	0.355 0.484	0.608 0.771	0.767 0.958	1.004 1.239
NA22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.134 0.173	0.295 0.384	0.471 0.593	0.680 0.830	0.860 1.029
NA23	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.102 0.136	0.285 0.403	0.443 0.643	0.591 0.842	0.779 1.058
NA24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.281 0.378	0.633 0.675	0.950 0.960	1.237 1.214	1.547 1.473
NA26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.366 0.423	0.668 0.747	0.973 0.973	1.274 1.242	1.579 1.529

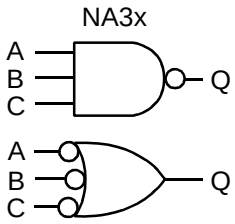
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA3x is a family of 3-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

HDL Syntax

Verilog ..... NA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NA31	NA32	NA33	NA34	NA36
A	1.0	1.9	1.9	1.9	1.9
B	1.0	1.9	1.9	1.9	1.9
C	1.0	1.9	1.9	1.9	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA31	1.2	0.464	1.3
NA32	1.5	0.867	2.4
NA33	2.2	1.387	6.7
NA34	2.8	1.876	10.0
NA36	3.0	2.212	12.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.211 0.318	0.319 0.460	0.524 0.722	0.717 0.971	0.901 1.211
NA32	**Number of Equivalent Loads**		**1**	**4**	**8**	**11**	**15 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.182 0.226	0.318 0.406	0.468 0.617	0.582 0.774	0.748 0.989
NA33	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.403 0.459	0.713 0.765	1.054 1.081	1.359 1.356	1.697 1.656
NA34	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.376 0.431	0.690 0.728	1.001 1.013	1.290 1.264	1.595 1.527
NA36	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.400 0.480	0.706 0.791	1.003 1.059	1.307 1.325	1.637 1.603

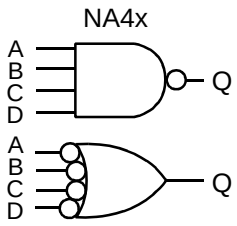
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA4x is a family of 4-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

HDL Syntax

Verilog ..... NA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NA41	NA42	NA43	NA44	NA46
A	1.0	2.0	2.0	2.0	2.0
B	1.0	2.0	2.0	2.0	2.0
C	1.0	2.0	2.0	2.0	2.0
D	1.0	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA41	1.8	0.567	1.7
NA42	2.2	1.056	2.9
NA43	3.0	1.576	7.2
NA44	3.2	2.056	10.5
NA46	3.5	2.392	13.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.267 0.378	0.395 0.535	0.630 0.820	0.740 0.962	0.949 1.260
NA42	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.197 0.265	0.312 0.428	0.464 0.648	0.557 0.796	0.688 1.027
NA43	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.430 0.506	0.744 0.809	1.085 1.127	1.388 1.404	1.723 1.703
NA44	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.400 0.494	0.698 0.796	1.000 1.079	1.298 1.334	1.634 1.599
NA46	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.436 0.553	0.740 0.854	1.037 1.116	1.342 1.379	1.646 1.640

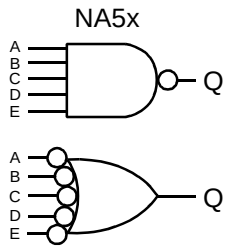
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA5x is a family of 5-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

HDL Syntax

Verilog ..... NA5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NA5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NA51	NA52	NA53	NA54	NA56
A	1.0	1.0	1.9	1.9	1.9
B	1.0	0.9	1.9	1.9	1.9
C	1.0	1.0	2.0	2.0	1.9
D	1.0	1.0	1.9	2.0	1.8
E	1.0	1.0	2.0	2.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA51	2.0	0.666	2.2
NA52	3.0	1.166	6.9
NA53	3.5	2.018	9.8
NA54	3.5	2.511	14.1
NA56	4.0	2.853	16.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA51	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.312 0.444	0.424 0.631	0.530 0.808	0.636 0.979	0.851 1.315
NA52	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.514 0.652	0.813 0.963	1.178 1.320	1.609 1.734	1.966 2.073
NA53	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.423 0.567	0.744 0.910	1.085 1.242	1.386 1.523	1.715 1.822
NA54	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.384 0.495	0.683 0.843	0.997 1.145	1.296 1.402	1.613 1.656
NA56	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.409 0.561	0.717 0.950	1.028 1.236	1.336 1.500	1.643 1.752

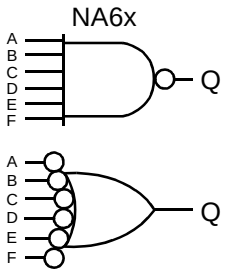
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA6x is a family of 6-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: NA6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads				
	NA61	NA62	NA63	NA64	NA66
A	1.0	1.9	1.9	1.9	1.9
B	1.0	1.9	1.9	1.9	1.9
C	1.0	2.0	2.0	2.0	2.0
D	1.0	2.0	2.0	2.0	2.0
E	1.0	1.9	1.9	1.9	1.9
F	1.0	2.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA61	3.2	1.283	7.5
NA62	3.5	2.417	13.0
NA63	4.0	2.588	14.0
NA64	4.0	2.745	15.1
NA66	4.2	3.082	17.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA61	Number of Equivalent Loads		1	5	10	16	21 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.553 0.698	0.848 1.003	1.210 1.370	1.641 1.799	1.997 2.151
NA62	Number of Equivalent Loads		1	10	20	29	39 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.397 0.506	0.688 0.822	1.025 1.145	1.334 1.424	1.682 1.727
NA63	Number of Equivalent Loads		1	14	28	43	57 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.408 0.510	0.673 0.828	0.979 1.120	1.319 1.410	1.642 1.669
NA64	Number of Equivalent Loads		1	19	38	56	75 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.443 0.539	0.745 0.888	1.058 1.181	1.357 1.436	1.681 1.688
NA66	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.450 0.552	0.734 0.946	1.032 1.260	1.337 1.534	1.646 1.784

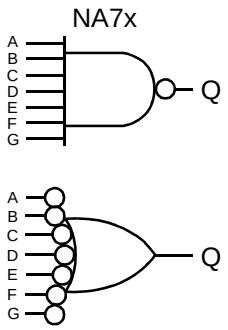
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA7x is a family of 7-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	X	X	X	X	X	X	H
X	L	X	X	X	X	X	H
X	X	L	X	X	X	X	H
X	X	X	L	X	X	X	H
X	X	X	X	L	X	X	H
X	X	X	X	X	L	X	H
X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA7x *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: NA7x port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads				
	NA71	NA72	NA73	NA74	NA76
A	1.9	1.9	1.9	1.9	1.9
B	1.9	1.9	1.9	1.9	1.9
C	2.0	2.0	2.0	2.0	2.0
D	2.1	2.1	2.0	2.1	2.0
E	2.0	2.0	2.0	2.1	2.0
F	2.0	2.0	1.9	2.0	2.0
G	2.0	2.0	1.9	2.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA71	4.5	2.504	11.9
NA72	4.5	2.852	17.0
NA73	4.8	3.013	17.8
NA74	4.8	3.170	19.2
NA76	5.0	3.506	21.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA71	Number of Equivalent Loads		1	5	10	16	21 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.511 0.778	0.795 1.137	1.156 1.520	1.593 1.940	1.959 2.271
NA72	Number of Equivalent Loads		1	10	20	29	39 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.463 0.656	0.765 1.005	1.101 1.338	1.403 1.620	1.739 1.919
NA73	Number of Equivalent Loads		1	14	28	43	57 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.462 0.701	0.754 1.034	1.055 1.334	1.377 1.641	1.682 1.921
NA74	Number of Equivalent Loads		1	19	38	56	75 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.488 0.759	0.773 1.125	1.062 1.406	1.353 1.666	1.678 1.941
NA76	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.491 0.755	0.795 1.186	1.101 1.520	1.402 1.800	1.701 2.051

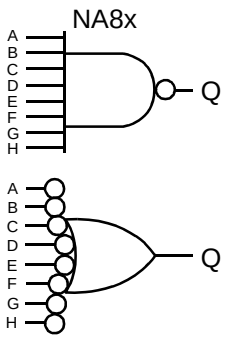
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA8x is a family of 8-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA8x *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: NA8x port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads				
	NA81	NA82	NA83	NA84	NA86
A	1.0	1.9	1.9	1.9	1.9
B	1.0	1.8	1.9	1.9	1.9
C	1.0	1.8	1.9	1.9	1.9
D	1.0	1.9	1.9	1.9	1.9
E	1.0	1.9	2.0	2.0	1.9
F	1.0	1.8	1.9	1.9	1.9
G	1.0	2.0	1.9	1.9	2.0
H	1.0	1.9	1.9	1.9	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA81	3.8	1.469	8.1
NA82	4.8	3.068	17.5
NA83	4.8	3.222	18.8
NA84	4.8	3.381	19.9
NA86	5.0	3.719	22.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA81	Number of Equivalent Loads		1	5	10	16	21 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.600 0.763	0.912 1.069	1.279 1.433	1.704 1.858	2.050 2.205
NA82	Number of Equivalent Loads		1	10	20	29	39 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.447 0.656	0.764 1.023	1.104 1.356	1.406 1.629	1.737 1.916
NA83	Number of Equivalent Loads		1	14	28	43	57 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.466 0.676	0.751 1.018	1.059 1.332	1.391 1.643	1.700 1.916
NA84	Number of Equivalent Loads		1	19	38	56	75 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.468 0.719	0.769 1.128	1.085 1.425	1.383 1.675	1.699 1.927
NA86	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.494 0.767	0.812 1.232	1.115 1.528	1.415 1.787	1.724 2.031

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

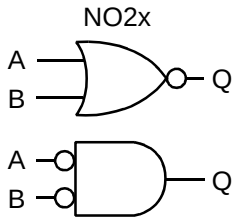
NO2x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NO2x is a family of 2-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

HDL Syntax

Verilog ..... NO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NO21	NO22	NO23	NO24	NO26
A	0.9	1.9	3.7	1.8	1.8
B	0.9	2.0	3.6	1.8	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO21	1.0	0.383	0.9
NO22	1.5	0.720	1.4
NO23	1.8	1.385	3.1
NO24	2.5	1.807	9.6
NO26	2.8	2.154	11.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.272 0.260	0.500 0.441	0.820 0.671	1.033 0.822	1.357 1.060
NO22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.173 0.180	0.409 0.346	0.683 0.505	1.021 0.686	1.307 0.839
NO23	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.127 0.135	0.396 0.311	0.676 0.469	0.928 0.600	1.207 0.733
NO24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.389 0.412	0.696 0.681	1.012 0.941	1.318 1.216	1.650 1.510
NO26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.430 0.395	0.762 0.715	1.073 1.005	1.378 1.279	1.687 1.545

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

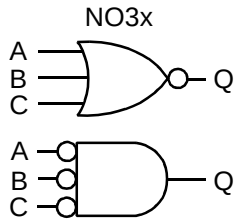
NO3x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NO3x is a family of 3-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

HDL Syntax

Verilog ..... NO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NO31	NO32	NO33	NO34	NO36
A	1.0	1.9	1.9	1.9	1.9
B	1.0	1.9	1.9	1.9	1.9
C	0.9	1.8	1.8	1.8	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO31	1.2	0.539	1.5
NO32	1.2	1.004	2.4
NO33	2.2	1.574	7.1
NO34	2.8	2.108	10.6
NO36	2.8	2.448	12.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.323 0.250	0.500 0.359	0.846 0.546	1.184 0.713	1.515 0.873
NO32	**Number of Equivalent Loads**		**1**	**4**	**8**	**11**	**15 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.226 0.191	0.461 0.318	0.770 0.461	1.000 0.567	1.304 0.717
NO33	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.527 0.445	0.831 0.749	1.173 1.066	1.482 1.343	1.827 1.645
NO34	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.533 0.422	0.811 0.716	1.129 1.009	1.442 1.278	1.780 1.557
NO36	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.541 0.451	0.841 0.765	1.155 1.054	1.471 1.326	1.801 1.587

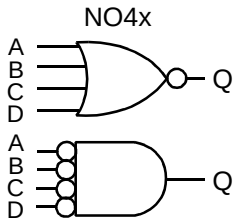
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NO4x is a family of 4-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... NO4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NO4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NO41	NO42	NO43	NO44	NO46
A	1.0	1.0	1.8	1.9	1.8
B	1.0	1.0	1.8	1.8	1.8
C	1.0	1.0	1.8	1.8	1.8
D	1.0	1.0	1.9	1.8	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO41	1.8	0.664	1.8
NO42	2.8	1.154	6.3
NO43	2.5	1.793	7.4
NO44	2.8	2.328	11.4
NO46	3.0	2.671	13.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.402 0.306	0.607 0.415	1.008 0.600	1.208 0.685	1.610 0.845
NO42	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.562 0.585	0.858 0.885	1.225 1.242	1.655 1.656	2.004 1.994
NO43	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.585 0.467	0.868 0.776	1.205 1.093	1.518 1.368	1.873 1.666
NO44	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.567 0.392	0.874 0.698	1.188 0.987	1.480 1.244	1.786 1.502
NO46	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.539 0.446	0.882 0.773	1.210 1.047	1.530 1.301	1.853 1.556

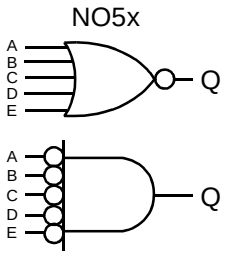
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NO5x is a family of 5-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

HDL Syntax

Verilog ..... NO5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NO5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NO51	NO52	NO53	NO54	NO56
A	1.0	1.0	1.9	1.9	1.8
B	1.1	1.0	1.9	1.8	1.8
C	1.0	1.0	1.9	1.9	1.9
D	1.0	1.0	1.9	1.9	1.8
E	1.0	1.0	1.8	1.8	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
NO51	2.0	0.788	2.1
NO52	3.0	1.310	6.8
NO53	3.0	2.271	10.0
NO54	3.5	2.816	14.1
NO56	3.5	3.169	16.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO51	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.440 0.354	0.686 0.456	0.928 0.546	1.170 0.634	1.658 0.823
NO52	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.570 0.591	0.876 0.895	1.238 1.252	1.660 1.665	2.004 2.003
NO53	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.497 0.509	0.796 0.833	1.146 1.155	1.460 1.432	1.800 1.730
NO54	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.435 0.396	0.747 0.731	1.069 1.019	1.367 1.275	1.677 1.538
NO56	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.479 0.460	0.779 0.784	1.092 1.080	1.405 1.354	1.717 1.614

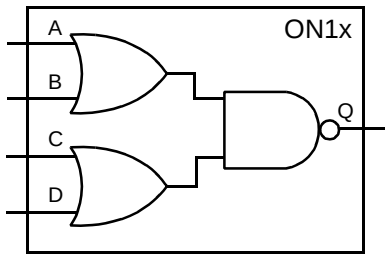
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON1x is a family of OR-NAND circuits consisting of two 2-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON11	ON12	ON14	ON16
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.8
C	1.0	1.0	1.0	1.9
D	1.0	1.0	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON11	1.5	0.485	2.3
ON12	2.8	1.285	6.8
ON14	2.5	1.448	7.6
ON16	3.2	2.790	13.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON11	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.351 0.362	0.646 0.598	1.061 0.907	1.336 1.106	1.758 1.410
ON12	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.577 0.616	0.864 0.930	1.223 1.292	1.655 1.708	2.016 2.045
ON14	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.553 0.589	0.843 0.933	1.184 1.262	1.499 1.538	1.854 1.833
ON16	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.438 0.464	0.730 0.829	1.041 1.111	1.331 1.373	1.634 1.650

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

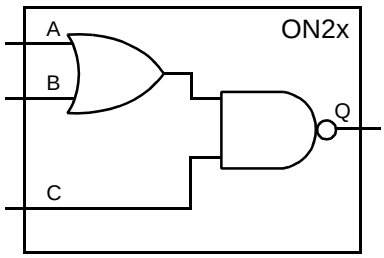
ON2X

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON2x is a family of OR-NAND circuits consisting of one 2-input OR and a direct input into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	Q
L	L	X	H
X	X	L	H
All other combinations			L

HDL Syntax

Verilog ..... ON2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: ON2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	ON21	ON22	ON24	ON26
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.9
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON21	1.2	0.399	1.8
ON22	2.5	1.122	6.0
ON24	2.5	1.296	7.2
ON26	3.0	2.309	13.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.331 0.312	0.641 0.541	1.074 0.853	1.358 1.053	1.794 1.346
ON22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.539 0.601	0.828 0.916	1.191 1.268	1.627 1.679	1.991 2.025
ON24	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.547 0.594	0.851 0.940	1.190 1.269	1.494 1.546	1.833 1.839
ON26	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.435 0.466	0.738 0.822	1.049 1.108	1.340 1.371	1.646 1.645

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

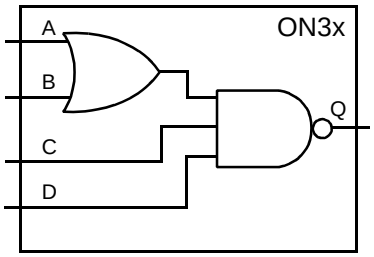
ON3x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON3x is a family of OR-NAND circuits consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON31	ON32	ON34	ON36
A	0.9	1.1	1.0	1.9
B	1.0	1.0	1.0	1.8
C	1.0	1.0	1.0	1.9
D	1.0	1.0	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON31	1.5	0.524	2.1
ON32	2.8	1.154	6.7
ON34	2.8	1.328	7.6
ON36	3.2	2.533	14.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.374 0.366	0.549 0.510	0.881 0.781	1.203 1.048	1.522 1.317
ON32	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.563 0.618	0.850 0.930	1.208 1.293	1.637 1.712	1.995 2.053
ON34	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.565 0.590	0.861 0.947	1.194 1.284	1.495 1.566	1.830 1.864
ON36	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.440 0.472	0.755 0.818	1.051 1.116	1.343 1.373	1.657 1.629

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

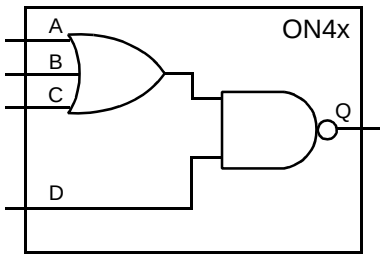
ON4x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON4x is a family of OR-NAND circuits consisting of one 3-input OR gate into and a direct input into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON41	ON42	ON44	ON46
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.9
C	1.0	1.0	1.0	1.8
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON41	1.5	0.433	2.3
ON42	2.8	1.276	6.6
ON44	2.8	1.450	7.8
ON46	3.5	2.612	13.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON41	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.454 0.345	0.647 0.473	1.019 0.710	1.392 0.932	1.776 1.145
ON42	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.703 0.629	0.973 0.947	1.329 1.309	1.770 1.722	2.144 2.054
ON44	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.707 0.630	1.008 0.980	1.353 1.311	1.666 1.589	2.018 1.885
ON46	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.521 0.483	0.825 0.845	1.141 1.130	1.434 1.376	1.743 1.619

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

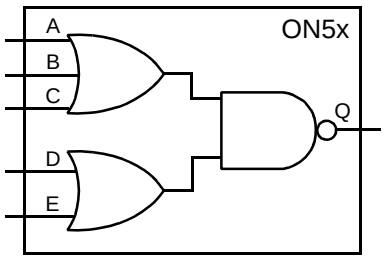
ON5x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON5x is a family of OR-NAND circuits consisting of one 3-input OR gate and one 2-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	L	H
All other combinations					L

HDL Syntax

Verilog ..... ON5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON52	ON54	ON56
A	1.1	1.1	1.9
B	1.1	1.1	1.8
C	1.1	1.1	1.8
D	1.0	1.0	1.9
E	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON52	3.0	1.437	7.0
ON54	3.0	1.611	8.3
ON56	3.5	3.086	14.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

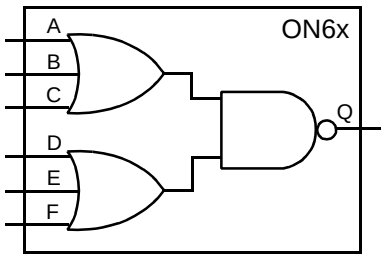
ON52	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.712 0.647	0.988 0.962	1.345 1.320	1.781 1.733	2.149 2.076
ON54	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.717 0.646	1.033 0.980	1.369 1.310	1.667 1.593	1.994 1.897
ON56	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.557 0.504	0.860 0.864	1.176 1.112	1.476 1.381	1.793 1.664

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON6x is a family of OR-NAND circuits consisting of two 3-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	L	H
All other combinations						L

HDL Syntax

Verilog ..... ON6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ON6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ON62	ON64	ON66
A	1.0	1.0	1.9
B	1.1	1.1	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	1.8
F	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON62	3.2	1.591	7.5
ON64	3.2	1.764	8.8
ON66	4.0	3.397	15.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON62	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.726 0.646	1.001 0.966	1.358 1.329	1.795 1.741	2.164 2.072
ON64	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.739 0.643	1.039 0.998	1.374 1.335	1.675 1.619	2.011 1.920
ON66	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.560 0.500	0.853 0.841	1.162 1.137	1.459 1.393	1.777 1.649

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

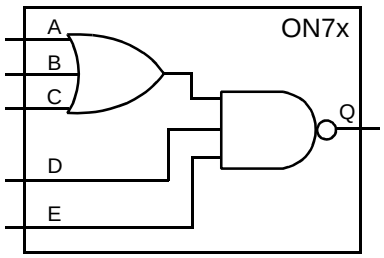
ON7x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON7x is a family of OR-NAND circuits consisting of one 3-input OR gate a two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Core Logic

HDL Syntax

Verilog ..... ON7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON72	ON74	ON76
A	1.0	1.0	1.9
B	1.0	1.0	1.8
C	1.0	1.0	1.8
D	1.0	1.0	1.9
E	1.0	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON72	3.0	1.305	6.9
ON74	3.0	1.480	8.2
ON76	3.5	2.826	14.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON72	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.695 0.631	1.003 0.942	1.366 1.310	1.786 1.731	2.129 2.064
ON74	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.711 0.632	1.018 0.991	1.357 1.324	1.660 1.600	1.997 1.893
ON76	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.550 0.518	0.833 0.866	1.150 1.140	1.459 1.394	1.791 1.659

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

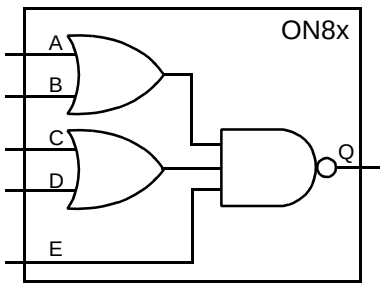
ON8x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON8x is a family of OR-NAND circuits consisting of two 2-input OR gates and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	X	X	X	H
X	X	L	L	X	H
X	X	X	X	L	H
All other combinations					L

HDL Syntax

Verilog ..... ON8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON82	ON84	ON86
A	1.1	1.0	1.9
B	1.1	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.8
E	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON82	3.5	1.633	8.7
ON84	3.5	1.807	10.1
ON86	4.2	3.461	17.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON82	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.605 0.722	0.893 1.067	1.252 1.450	1.680 1.881	2.037 2.225
ON84	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.602 0.752	0.923 1.150	1.261 1.502	1.557 1.788	1.880 2.086
ON86	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.457 0.620	0.740 1.002	1.056 1.329	1.358 1.605	1.672 1.870

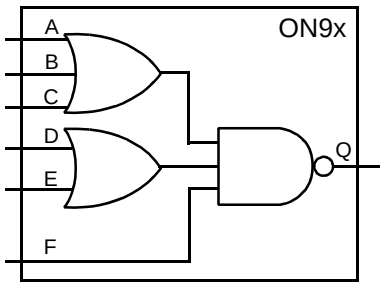
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON9x is a family of OR-NAND circuits consisting of one 3-input OR gate, one 2-input OR gate, and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	X	H
X	X	X	X	X	L	H
All other combinations						L

HDL Syntax

Verilog ..... ON9x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ON9x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ON92	ON94	ON96
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.8
D	1.0	1.0	1.8
E	1.0	1.0	1.8
F	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON92	4.0	1.797	9.0
ON94	4.0	1.970	10.3
ON96	4.5	3.760	18.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON92	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.754 0.766	1.046 1.113	1.405 1.496	1.831 1.925	2.184 2.267
ON94	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.757 0.773	1.077 1.173	1.415 1.527	1.713 1.817	2.039 2.118
ON96	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.619 0.629	0.935 1.034	1.235 1.353	1.525 1.625	1.837 1.894

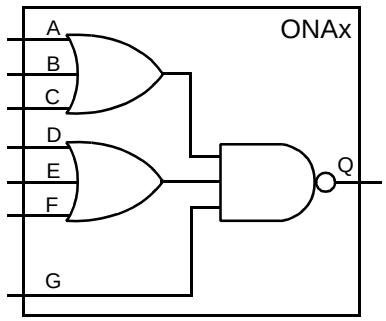
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ONAx

Description

ONAx is a family of OR-NAND circuits consisting of two 3-input OR gates and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	L	X	H
X	X	X	X	X	X	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONAx port map (Q, A, B, C, D, E, F, G;)

Pin Loading

Pin Name	Equivalent Loads		
	ONA2	ONA4	ONA6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.8
D	1.0	1.1	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.8
G	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONA2	4.2	1.951	9.8
ONA4	4.2	2.125	11.0
ONA6	5.0	4.067	19.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONA2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.777 0.729	1.058 1.089	1.406 1.477	1.832 1.901	2.191 2.234
ONA4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.760 0.771	1.062 1.168	1.401 1.524	1.707 1.817	2.048 2.124
ONA6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.602 0.600	0.913 0.994	1.226 1.318	1.516 1.587	1.819 1.844

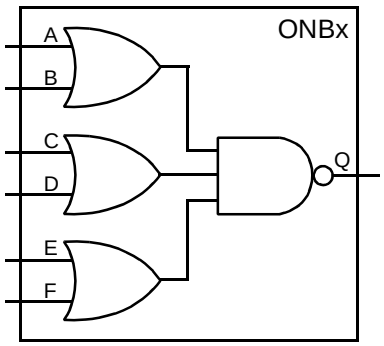
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ONBx

Description

ONBx is a family of OR-NAND circuits consisting of three 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	X	X	X	X	H
X	X	L	L	X	X	H
X	X	X	X	L	L	H
All other combinations						L

HDL Syntax

Verilog ..... ONBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ONBx port map (Q, A, B, C, D, E, F)

Pin Loading

Pin Name	Equivalent Loads		
	ONB2	ONB4	ONB6
A	1.1	1.0	1.9
B	1.0	1.0	1.8
C	1.1	1.0	1.9
D	1.0	1.0	1.8
E	1.1	1.0	1.9
F	1.1	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONB2	3.8	1.793	9.1
ONB4	3.8	1.967	10.1
ONB6	4.5	3.771	18.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONB2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.610 0.726	0.905 1.081	1.264 1.463	1.689 1.885	2.039 2.217
ONB4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.594 0.745	0.893 1.145	1.232 1.494	1.540 1.776	1.884 2.068
ONB6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.460 0.611	0.777 1.024	1.093 1.332	1.389 1.614	1.701 1.892

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

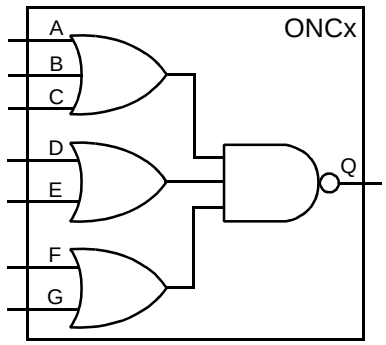
ONCx

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ONCx is a family of OR-NAND circuits consisting of one 3-input OR gate and two 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	X	X	H
X	X	X	X	X	L	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ONC2	ONC4	ONC6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.8
D	1.0	1.0	1.9
E	1.0	1.0	1.8
F	1.0	1.0	1.9
G	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONC2	4.0	1.947	9.4
ONC4	4.0	2.124	10.8
ONC6	4.8	4.070	19.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONC2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.755 0.774	1.034 1.125	1.391 1.493	1.827 1.911	2.193 2.260
ONC4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.748 0.764	1.042 1.164	1.385 1.518	1.701 1.805	2.057 2.104
ONC6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.580 0.632	0.894 1.044	1.181 1.402	1.475 1.691	1.793 1.956

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

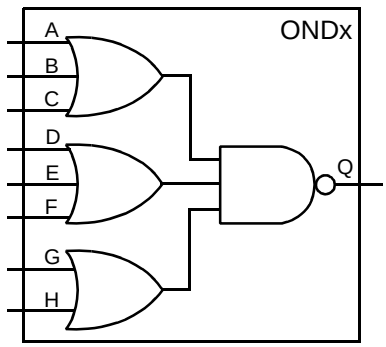
ONDx

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ONDx is a family of OR-NAND circuits consisting of two 3-input OR gates and one 2-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	L	L	X	X	X	X	X	H
X	X	X	L	L	L	X	X	H
X	X	X	X	X	X	L	L	H
All other combinations								L

HDL Syntax

Verilog ..... ONDx *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: ONDx port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads		
	OND2	OND4	OND6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.8
D	1.1	1.1	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.8
G	1.0	1.0	1.9
H	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OND2	4.5	2.111	10.1
OND4	4.5	2.285	11.4
OND6	5.0	4.369	20.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

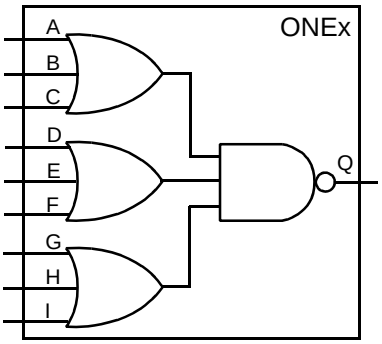
OND2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.763 0.766	1.044 1.119	1.402 1.502	1.836 1.925	2.199 2.260
OND4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.770 0.773	1.080 1.179	1.421 1.535	1.727 1.825	2.066 2.126
OND6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.591 0.637	0.895 1.039	1.219 1.358	1.527 1.630	1.852 1.902

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ONEx is a family of OR-NAND circuits consisting of three 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
L	L	L	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	L	L	L	H
All other combinations									L

HDL Syntax

Verilog ..... ONEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ONEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ONE2	ONE4	ONE6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.8
D	1.1	1.1	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.8
G	1.0	1.0	1.9
H	1.0	1.0	1.9
I	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONE2	4.8	2.265	10.5
ONE4	4.8	2.439	11.7
ONE6	5.5	4.673	21.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

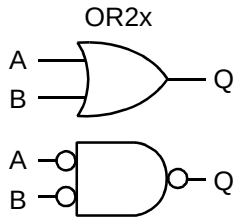
ONE2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.754 0.766	1.051 1.122	1.410 1.504	1.833 1.925	2.180 2.257
ONE4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.766 0.778	1.089 1.187	1.425 1.538	1.718 1.820	2.037 2.111
ONE6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.595 0.740	0.890 1.127	1.200 1.468	1.492 1.755	1.799 2.032

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

OR2x is a family of 2-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

HDL Syntax

Verilog ..... OR2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR21	OR22	OR24	OR26
A	1.0	1.0	1.9	1.9
B	1.0	1.0	1.9	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR21	1.2	0.570	2.4
OR22	1.5	0.747	3.5
OR24	1.8	1.420	6.3
OR26	2.0	1.781	9.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR21	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.330 0.410	0.621 0.729	0.984 1.081	1.418 1.496	1.781 1.857
OR22	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.283 0.402	0.606 0.773	0.952 1.094	1.255 1.360	1.587 1.649
OR24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.237 0.320	0.549 0.662	0.862 0.948	1.154 1.202	1.459 1.464
OR26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.346 0.396	0.635 0.755	0.923 1.045	1.227 1.316	1.561 1.574

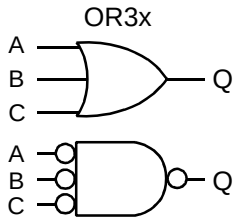
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

OR3x is a family of 3-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

HDL Syntax

Verilog ..... OR3x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR3x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR31	OR32	OR34	OR36
A	1.0	1.0	1.8	3.0
B	1.0	1.0	1.8	3.0
C	1.0	1.0	1.9	2.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR31	1.5	0.724	3.0
OR32	1.5	0.898	4.2
OR34	2.0	1.719	7.6
OR36	3.5	2.595	11.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR31	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.367 0.551	0.661 0.906	1.020 1.287	1.449 1.705	1.806 2.035
OR32	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.367 0.545	0.670 0.964	1.008 1.324	1.315 1.613	1.657 1.913
OR34	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.359 0.429	0.688 0.826	0.996 1.113	1.289 1.368	1.606 1.626
OR36	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.266 0.388	0.576 0.784	0.895 1.084	1.207 1.348	1.514 1.591

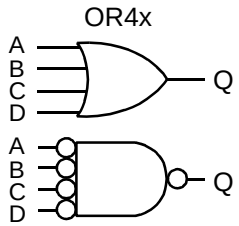
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

OR4x is a family of 4-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

HDL Syntax

Verilog ..... OR4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: OR4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	OR41	OR42	OR44	OR46
A	1.1	1.1	2.9	2.8
B	1.1	1.1	2.8	2.9
C	1.1	1.1	2.9	2.9
D	1.1	1.1	3.0	2.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR41	2.0	0.851	3.4
OR42	2.0	1.025	4.7
OR44	3.2	2.554	9.4
OR46	3.5	2.919	12.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR41	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.408 0.634	0.694 1.026	1.052 1.429	1.484 1.862	1.846 2.198
OR42	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.412 0.647	0.725 1.083	1.058 1.468	1.358 1.781	1.699 2.107
OR44	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.287 0.376	0.604 0.778	0.892 1.092	1.191 1.362	1.505 1.630
OR46	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.251 0.449	0.578 0.890	0.879 1.220	1.174 1.501	1.487 1.762

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

PORB

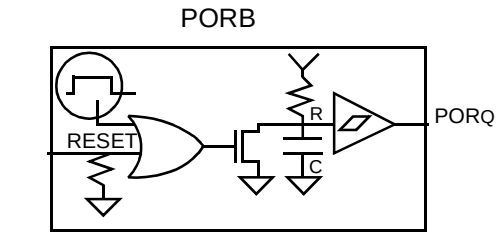
Description

PORB is a power-on-reset.

When power is applied, the PORQ output is asserted low for at least 2 microseconds after the logic circuits become operational. The active high RESET input also drives the PORQ signal to its active low state. Since the PORB is a corner function cell the RESET pin must be driven through the core.

For proper operation, user-designed external circuitry must provide a V_{DD} power slew rate of at least one volt per microsecond. This ensures that the reset pulse will be properly output when V_{DD} falls to zero and immediately returns to its valid range.

Logic Symbol



Truth Table

RESET	PORQ
L	H
H	L

Pin Loading

	Load
RESET	5.9 eql

HDL Syntax

Verilog ..... PORB *inst_name* (RESET, PORQ);

VHDL..... *inst_name*: PORB port map (RESET, PORQ);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	74.806	nA
EQL_{pd}	1664.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

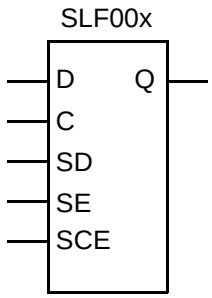
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
RESET	PORQ	t_{PLH}	4242.43				
RESET	PORQ	t_{PHL}	9.55				

Description

SLF00x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low.

Logic Symbol



Truth Table

C	D	SD	SE	SCE	Q
↑	H	X	L	L	H
↑	L	X	L	L	L
↑	X	H	H	L	H
↑	X	L	H	L	L
L	X	X	X	L	NC
L	H	X	L	H	H
L	L	X	L	H	L
L	X	H	H	H	H
L	X	L	H	H	L
H	X	X	X	H	NC

NC = No Change

HDL Syntax

Verilog ..... SLF00x *inst_name* (Q, C, D, SCE, SD, SE);

VHDL..... *inst_name*: SLF00x port map (Q, C, D, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF001	SLF002	SLF004	SLF006
C	1.0	1.1	1.1	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3
SCE	1.0	1.1	1.0	1.1

AMI500MXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF001	7.2	2.592	13.7
SLF002	7.8	2.965	17.1
SLF004	8.2	3.335	19.9
SLF006	8.5	3.679	22.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
SLF001	From: C To: Q	t_{PLH} t_{PHL}	1.28 1.79	1.60 2.14	1.96 2.52	2.39 2.96	2.74 3.30
	From: D To: Q	t_{PLH} t_{PHL}	1.23 1.64	1.56 2.02	1.93 2.40	2.33 2.80	2.66 3.11
	From: SCE To: Q	t_{PLH} t_{PHL}	0.81 0.80	1.12 1.17	1.49 1.55	1.91 1.96	2.26 2.27
	From: SD To: Q	t_{PLH} t_{PHL}	1.22 1.55	1.53 1.87	1.89 2.25	2.32 2.70	2.68 3.07
	From: SE To: Q	t_{PLH} t_{PHL}	1.33 1.79	1.64 2.12	2.01 2.50	2.44 2.94	2.78 3.31
SLF002	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	1.28 1.74	1.60 2.10	1.92 2.42	2.21 2.68	2.52 2.96
	From: D To: Q	t_{PLH} t_{PHL}	1.21 1.56	1.54 1.90	1.86 2.22	2.14 2.49	2.45 2.78
	From: SCE To: Q	t_{PLH} t_{PHL}	0.78 0.64	1.09 1.01	1.43 1.34	1.73 1.61	2.06 1.90
	From: SD To: Q	t_{PLH} t_{PHL}	1.21 1.47	1.52 1.83	1.85 2.15	2.14 2.41	2.45 2.69
	From: SE To: Q	t_{PLH} t_{PHL}	1.32 1.73	1.64 2.08	1.97 2.40	2.25 2.67	2.55 2.95

	Number of Equivalent Loads		1	19	38	56	75 (max)
SLF004	From: C To: Q	t_{PLH} t_{PHL}	1.31 1.78	1.62 2.09	1.93 2.39	2.20 2.67	2.47 2.95
	From: D To: Q	t_{PLH} t_{PHL}	1.26 1.60	1.55 1.99	1.86 2.27	2.16 2.50	2.47 2.73
	From: SCE To: Q	t_{PLH} t_{PHL}	0.82 0.76	1.12 1.05	1.42 1.32	1.71 1.59	2.01 1.88
	From: SD To: Q	t_{PLH} t_{PHL}	1.26 1.49	1.54 1.88	1.86 2.17	2.14 2.42	2.43 2.66
	From: SE To: Q	t_{PLH} t_{PHL}	1.43 1.78	1.76 2.13	2.07 2.41	2.34 2.65	2.62 2.87
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
SLF006	From: C To: Q	t_{PLH} t_{PHL}	1.38 1.85	1.65 2.27	1.96 2.55	2.28 2.78	2.61 2.98
	From: D To: Q	t_{PLH} t_{PHL}	1.33 1.63	1.64 2.08	1.93 2.37	2.22 2.61	2.51 2.83
	From: SCE To: Q	t_{PLH} t_{PHL}	0.84 0.70	1.18 1.13	1.51 1.45	1.81 1.74	2.11 1.99
	From: SD To: Q	t_{PLH} t_{PHL}	1.24 1.60	1.57 1.98	1.89 2.27	2.20 2.53	2.50 2.77
	From: SE To: Q	t_{PLH} t_{PHL}	1.38 1.84	1.67 2.27	2.00 2.54	2.33 2.77	2.67 2.96

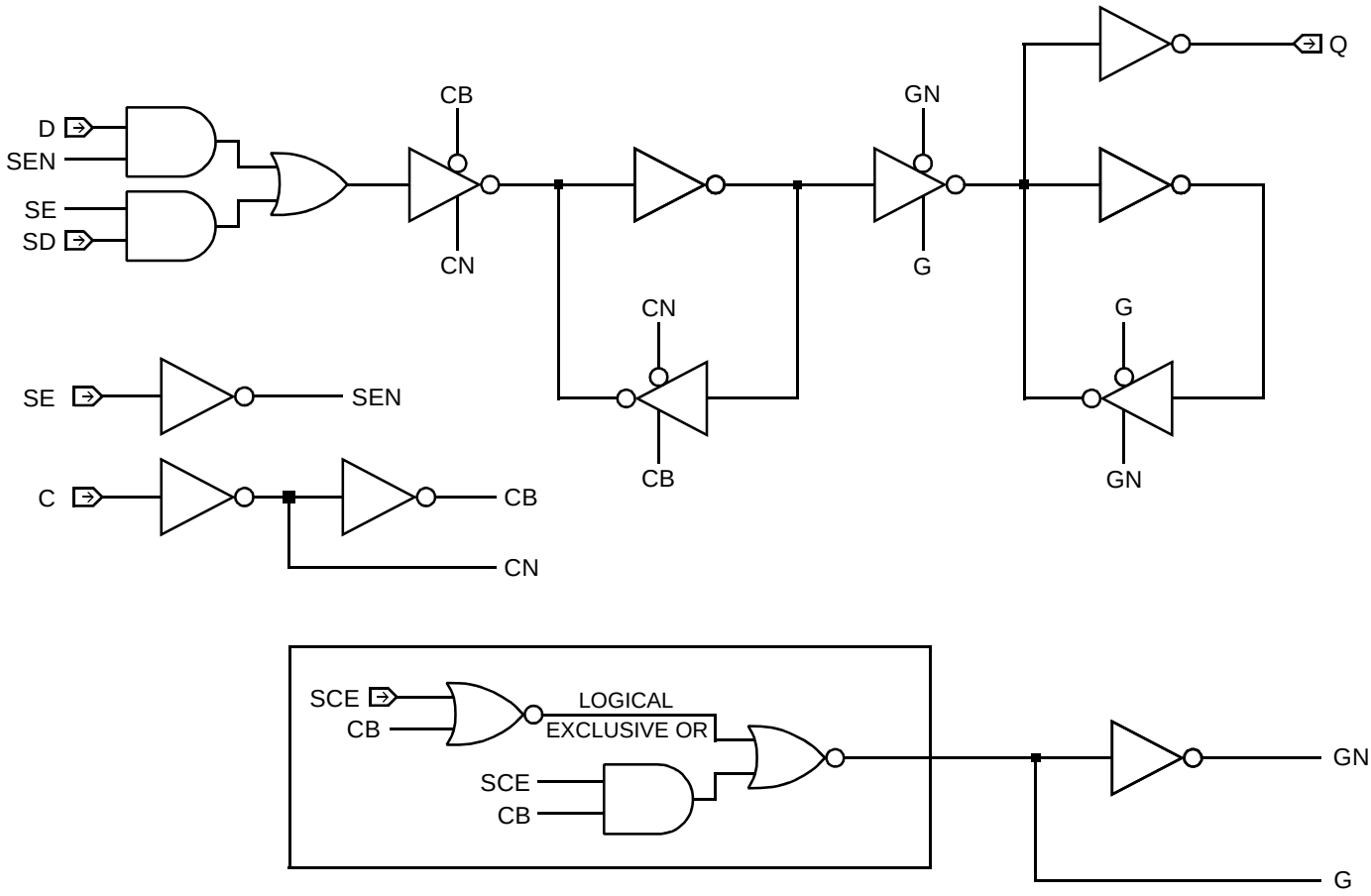
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF001	SLF002	SLF004	SLF006
Min C Width	High	t_w	1.13	1.14	1.21	1.27
Min C Width	Low	t_w	1.19	1.26	1.26	1.26
Min D Setup		t_{su}	0.99	1.07	1.07	1.07
Min D Hold		t_h	0.23	0.23	0.23	0.23
Min SD Setup		t_{su}	0.99	1.07	1.07	1.07
Min SD Hold		t_h	0.23	0.23	0.23	0.23
Min SE Setup		t_{su}	1.18	1.25	1.25	1.25
Min SE Hold		t_h	0.23	0.23	0.23	0.23
Min SCE Setup		t_{su}	0.76	0.77	0.84	0.90
Min SCE Hold		t_h	1.19	1.26	1.26	1.26

Logic Schematic



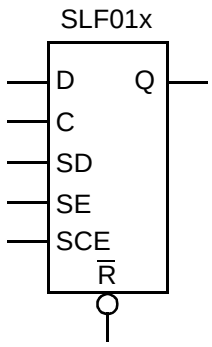
SLF01x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

SLF01x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. RESET is asynchronous and active low.

Logic Symbol



Truth Table

RN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF01x *inst_name* (Q, C, D, RN, SCE, SD, SE);

VHDL..... *inst_name*: SLF01x port map (Q, C, D, RN, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF011	SLF012	SLF014	SLF016
C	1.1	1.1	1.1	1.1
D	1.0	1.0	1.0	1.1
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3
SCE	1.1	1.1	1.1	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF011	8.2	3.276	19.1
SLF012	8.8	3.481	21.1
SLF014	9.0	3.825	23.1
SLF016	9.0	4.515	28.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
SLF011	From: C To: Q	t_{PLH} t_{PHL}	1.56 2.03	1.85 2.38	2.22 2.77	2.66 3.21	3.04 3.56
	From: D To: Q	t_{PLH} t_{PHL}	1.47 1.82	1.80 2.22	2.17 2.60	2.58 2.99	2.92 3.29
	From: RN To: Q	t_{PLH} t_{PHL}	1.12 1.12	1.41 1.47	1.78 1.86	2.22 2.29	2.59 2.64
	From: SCE To: Q	t_{PLH} t_{PHL}	0.88 0.85	1.20 1.21	1.57 1.60	1.99 2.03	2.34 2.37
	From: SD To: Q	t_{PLH} t_{PHL}	1.47 1.70	1.77 2.06	2.14 2.45	2.58 2.89	2.94 3.23
	From: SE To: Q	t_{PLH} t_{PHL}	1.58 1.95	1.87 2.30	2.24 2.69	2.68 3.13	3.05 3.49
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
SLF012	From: C To: Q	t_{PLH} t_{PHL}	1.48 1.83	1.77 2.15	2.10 2.47	2.40 2.76	2.74 3.07
	From: D To: Q	t_{PLH} t_{PHL}	1.42 1.63	1.71 1.99	2.04 2.31	2.34 2.57	2.68 2.84
	From: RN To: Q	t_{PLH} t_{PHL}	1.09 1.87	1.39 2.46	1.72 2.87	2.01 3.17	2.34 3.47
	From: SCE To: Q	t_{PLH} t_{PHL}	0.80 0.66	1.13 1.01	1.48 1.35	1.77 1.64	2.10 1.95
	From: SD To: Q	t_{PLH} t_{PHL}	1.40 1.59	1.70 1.96	2.04 2.28	2.35 2.53	2.70 2.80
	From: SE To: Q	t_{PLH} t_{PHL}	1.52 1.83	1.83 2.12	2.16 2.44	2.45 2.74	2.77 3.06

	Number of Equivalent Loads		1	19	38	56	75 (max)
SLF014	From: C To: Q	t_{PLH} t_{PHL}	1.55 1.86	1.84 2.25	2.13 2.55	2.41 2.79	2.71 3.03
	From: D To: Q	t_{PLH} t_{PHL}	1.47 1.64	1.75 2.08	2.07 2.38	2.37 2.62	2.70 2.86
	From: RN To: Q	t_{PLH} t_{PHL}	1.11 2.15	1.43 2.81	1.74 3.21	2.03 3.51	2.33 3.79
	From: SCE To: Q	t_{PLH} t_{PHL}	0.84 0.67	1.18 1.07	1.49 1.36	1.78 1.63	2.08 1.91
	From: SD To: Q	t_{PLH} t_{PHL}	1.44 1.60	1.80 1.98	2.09 2.27	2.36 2.51	2.65 2.75
	From: SE To: Q	t_{PLH} t_{PHL}	1.57 1.85	1.88 2.23	2.20 2.54	2.49 2.78	2.78 3.01
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
SLF016	From: C To: Q	t_{PLH} t_{PHL}	2.05 2.35	2.37 2.61	2.65 2.86	2.91 3.10	3.17 3.34
	From: D To: Q	t_{PLH} t_{PHL}	1.97 2.09	2.28 2.38	2.59 2.64	2.89 2.89	3.19 3.13
	From: RN To: Q	t_{PLH} t_{PHL}	1.64 0.82	1.89 1.11	2.19 1.36	2.51 1.61	2.85 1.85
	From: SCE To: Q	t_{PLH} t_{PHL}	1.39 1.11	1.70 1.45	2.01 1.70	2.29 1.96	2.57 2.23
	From: SD To: Q	t_{PLH} t_{PHL}	1.99 2.05	2.24 2.27	2.54 2.53	2.86 2.81	3.19 3.10
	From: SE To: Q	t_{PLH} t_{PHL}	2.07 2.25	2.36 2.61	2.65 2.86	2.94 3.08	3.22 3.27

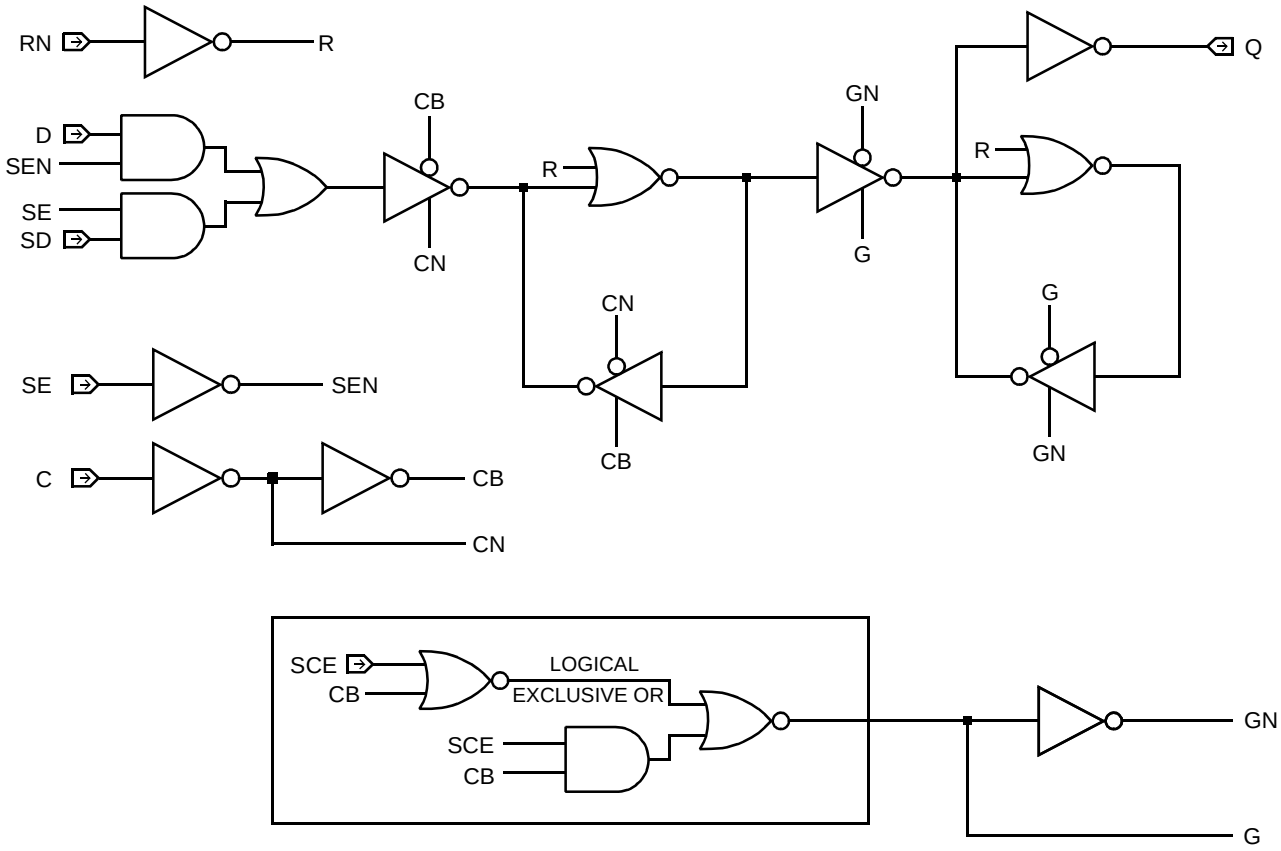
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF011	SLF012	SLF014	SLF016
Min C Width	High	t_w	1.32	1.24	1.31	1.40
Min C Width	Low	t_w	1.37	1.33	1.33	1.37
Min RN Width	Low	t_w	0.78	1.11	1.11	0.78
Min D Setup		t_{su}	1.12	1.14	1.14	1.12
Min D Hold		t_h	0.23	0.23	0.23	0.23
Min SD Setup		t_{su}	1.12	1.14	1.14	1.12
Min SD Hold		t_h	0.23	0.23	0.23	0.23
Min SE Setup		t_{su}	1.30	1.33	1.32	1.30
Min SE Hold		t_h	0.23	0.23	0.23	0.23
Min SCE Setup		t_{su}	0.93	0.87	0.94	1.01
Min SCE Hold		t_h	1.37	1.33	1.33	1.37
Min RN Setup		t_{su}	0.51	0.55	0.55	0.51
Min RN Hold		t_h	0.46	0.64	0.64	0.46

Logic Schematic



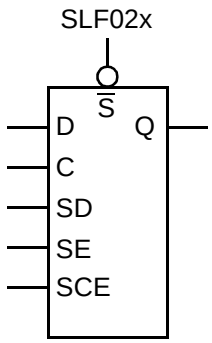
SLF02x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

SLF02x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET is asynchronous and active low.

Logic Symbol



Truth Table

SN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	H

NC = No Change

HDL Syntax

Verilog ..... SLF02x *inst_name* (Q, C, D, SCE, SD, SE, SN);

VHDL..... *inst_name*:SLF02x port map (Q, C, D, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF021	SLF022	SLF024	SLF026
C	1.1	1.1	1.1	1.1
D	1.1	1.1	1.1	1.1
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3
SCE	1.1	1.1	1.1	1.1
SN	2.2	2.2	2.2	2.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF021	7.8	2.912	16.2
SLF022	8.2	3.040	18.2
SLF024	8.5	3.385	20.2
SLF026	8.8	3.914	23.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
SLF021	From: C To: Q	t_{PLH} t_{PHL}	1.37 2.16	1.71 2.51	2.08 2.90	2.48 3.34	2.79 3.70
	From: D To: Q	t_{PLH} t_{PHL}	1.28 1.99	1.59 2.36	1.96 2.75	2.39 3.18	2.74 3.51
	From: SCE To: Q	t_{PLH} t_{PHL}	0.88 0.81	1.19 1.17	1.56 1.56	1.98 2.00	2.33 2.34
	From: SD To: Q	t_{PLH} t_{PHL}	1.28 1.86	1.58 2.18	1.95 2.57	2.39 3.03	2.75 3.41
	From: SE To: Q	t_{PLH} t_{PHL}	1.39 2.12	1.65 2.54	2.01 2.92	2.47 3.30	2.87 3.58
	From: SN To: Q	t_{PLH} t_{PHL}	0.75 1.02	1.07 1.42	1.43 1.88	1.85 2.40	2.19 2.82
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
SLF022	From: C To: Q	t_{PLH} t_{PHL}	1.35 1.84	1.70 2.19	2.02 2.52	2.29 2.79	2.57 3.07
	From: D To: Q	t_{PLH} t_{PHL}	1.30 1.70	1.61 2.06	1.93 2.39	2.22 2.65	2.54 2.92
	From: SCE To: Q	t_{PLH} t_{PHL}	0.81 0.68	1.12 1.03	1.46 1.37	1.75 1.66	2.08 1.97
	From: SD To: Q	t_{PLH} t_{PHL}	1.30 1.61	1.58 1.99	1.91 2.31	2.21 2.56	2.54 2.83
	From: SE To: Q	t_{PLH} t_{PHL}	1.42 1.85	1.70 2.22	2.03 2.55	2.33 2.80	2.66 3.07
	From: SN To: Q	t_{PLH} t_{PHL}	1.25 0.85	1.64 1.24	1.98 1.62	2.26 1.94	2.55 2.29

	Number of Equivalent Loads		1	19	38	56	75 (max)
SLF024	From: C To: Q	t_{PLH} t_{PHL}	1.42 1.88	1.76 2.28	2.06 2.57	2.34 2.82	2.67 3.05
	From: D To: Q	t_{PLH} t_{PHL}	1.39 1.72	1.72 2.11	2.05 2.42	2.34 2.68	2.62 2.94
	From: SCE To: Q	t_{PLH} t_{PHL}	0.86 0.67	1.15 1.08	1.49 1.38	1.81 1.64	2.16 1.93
	From: SD To: Q	t_{PLH} t_{PHL}	1.36 1.63	1.68 2.05	2.01 2.35	2.29 2.59	2.58 2.82
	From: SE To: Q	t_{PLH} t_{PHL}	1.44 1.90	1.77 2.31	2.10 2.60	2.39 2.84	2.68 3.06
	From: SN To: Q	t_{PLH} t_{PHL}	1.56 0.87	1.94 1.30	2.29 1.66	2.59 1.99	2.89 2.33
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
SLF026	From: C To: Q	t_{PLH} t_{PHL}	1.67 2.20	1.94 2.52	2.26 2.78	2.59 3.01	2.93 3.24
	From: D To: Q	t_{PLH} t_{PHL}	1.60 2.06	1.90 2.42	2.21 2.66	2.53 2.87	2.88 3.06
	From: SCE To: Q	t_{PLH} t_{PHL}	1.18 1.13	1.42 1.43	1.73 1.70	2.06 1.96	2.41 2.21
	From: SD To: Q	t_{PLH} t_{PHL}	1.64 1.98	1.90 2.25	2.20 2.51	2.54 2.77	2.90 3.01
	From: SE To: Q	t_{PLH} t_{PHL}	1.69 2.23	1.98 2.52	2.27 2.77	2.61 3.01	2.98 3.23
	From: SN To: Q	t_{PLH} t_{PHL}	0.59 1.21	0.88 1.56	1.18 1.88	1.49 2.19	1.81 2.49

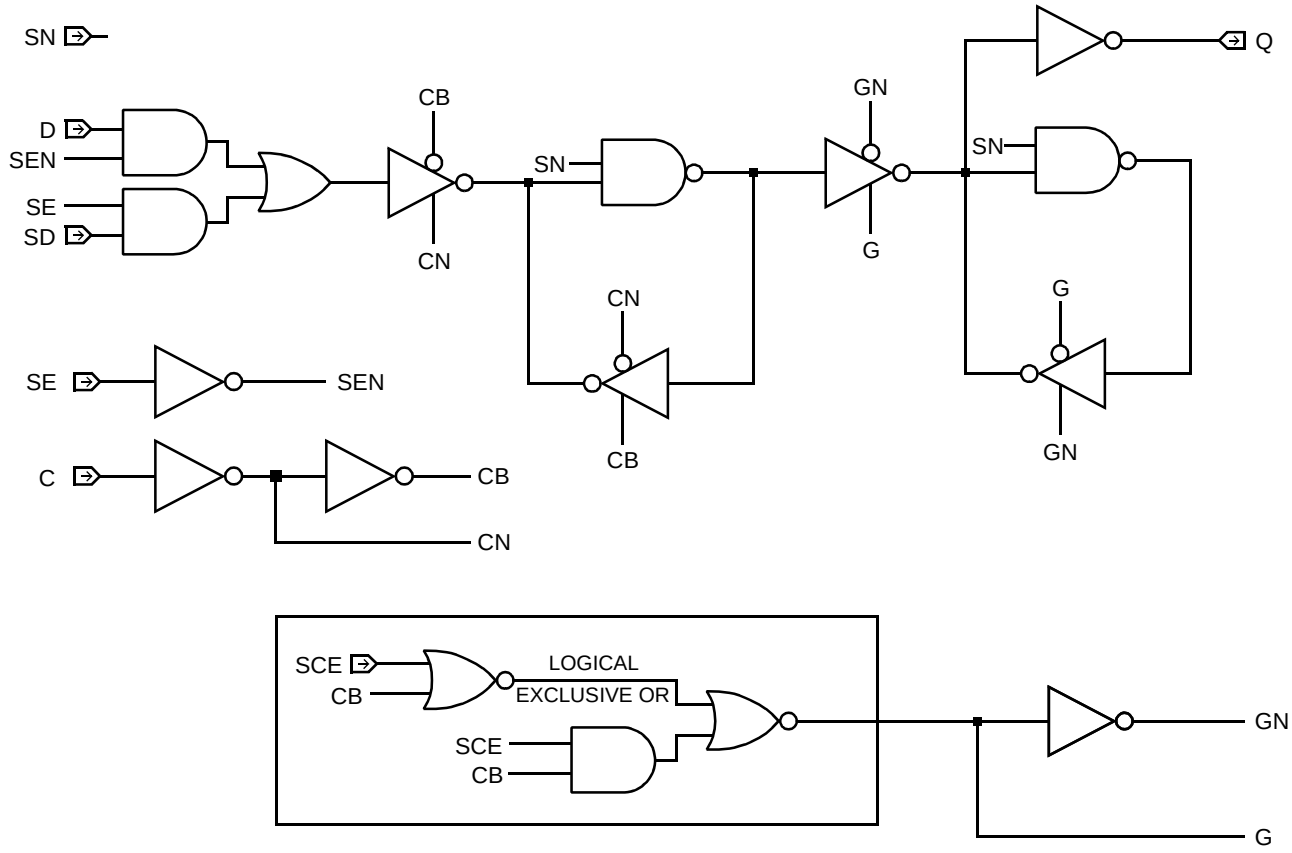
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF021	SLF022	SLF024	SLF026
Min C Width	High	t_w	1.29	1.20	1.26	1.22
Min C Width	Low	t_w	1.52	1.36	1.36	1.29
Min SN Width	Low	t_w	0.55	0.90	0.90	0.82
Min D Setup		t_{su}	1.26	1.17	1.17	1.09
Min D Hold		t_h	0.23	0.23	0.23	0.23
Min SD Setup		t_{su}	1.26	1.17	1.17	1.09
Min SD Hold		t_h	0.23	0.23	0.23	0.23
Min SE Setup		t_{su}	1.45	1.36	1.36	1.28
Min SE Hold		t_h	0.23	0.23	0.23	0.23
Min SCE Setup		t_{su}	0.91	0.83	0.90	0.85
Min SCE Hold		t_h	1.52	1.36	1.36	1.29
Min SN Setup		t_{su}	0.36	0.34	0.34	0.28
Min SN Hold		t_h	0.69	0.87	0.87	0.87

Logic Schematic



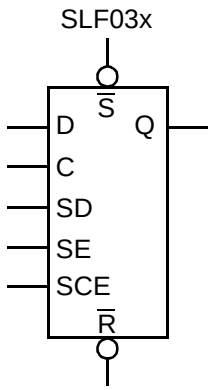
SLF03x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

SLF03x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET and RESET are asynchronous and active low.

Logic Symbol



Truth Table

RN	SN	C	D	SD	SE	SCE	Q
H	H	↑	H	X	L	L	H
H	H	↑	L	X	L	L	L
H	H	↑	X	H	H	L	H
H	H	↑	X	L	H	L	L
H	H	L	X	X	X	L	NC
H	H	L	H	X	L	H	H
H	H	L	L	X	L	H	L
H	H	L	X	H	H	H	H
H	H	L	X	L	H	H	L
H	H	H	X	X	X	H	NC
H	L	X	X	X	X	X	H
L	X	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF03x *inst_name* (Q, C, D, RN, SCE, SD, SE, SN);

VHDL..... *inst_name*: SLF03x port map (Q, C, D, RN, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF031	SLF032	SLF034	SLF036
C	1.1	1.1	1.1	1.1
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.1
SE	2.3	2.3	2.3	2.3
SCE	1.1	1.1	1.1	1.0
SN	2.3	2.2	2.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF031	8.8	2.905	19.2
SLF032	9.5	3.275	22.9
SLF034	9.8	3.608	24.9
SLF036	10.2	3.978	28.2

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	10	20	29	39 (max)
SLF031	From: C To: Q	t_{PLH} t_{PHL}	1.58 1.95	2.25 2.71	2.97 3.44	3.60 4.05	4.31 4.69
	From: D To: Q	t_{PLH} t_{PHL}	1.51 1.79	2.22 2.50	2.94 3.22	3.56 3.86	4.22 4.55
	From: RN To: Q	t_{PLH} t_{PHL}	1.20 1.67	1.85 2.53	2.57 3.32	3.21 3.97	3.93 4.65
	From: SCE To: Q	t_{PLH} t_{PHL}	0.83 0.81	1.53 1.56	2.26 2.29	2.90 2.92	3.61 3.60
	From: SD To: Q	t_{PLH} t_{PHL}	1.50 1.70	2.16 2.45	2.89 3.18	3.55 3.79	4.29 4.44
	From: SE To: Q	t_{PLH} t_{PHL}	1.61 1.96	2.29 2.70	3.01 3.42	3.65 4.04	4.35 4.71
	From: SN To: Q	t_{PLH} t_{PHL}	1.06 1.05	1.74 1.87	2.47 2.71	3.11 3.47	3.82 4.30
SLF032	Number of Equivalent Loads		1	10	20	29	39 (max)
	From: C To: Q	t_{PLH} t_{PHL}	1.64 1.93	2.00 2.23	2.33 2.55	2.59 2.84	2.87 3.16
	From: D To: Q	t_{PLH} t_{PHL}	1.59 1.78	1.88 2.12	2.21 2.45	2.51 2.72	2.85 3.01
	From: RN To: Q	t_{PLH} t_{PHL}	1.26 1.90	1.56 2.40	1.90 2.84	2.19 3.20	2.51 3.59
	From: SCE To: Q	t_{PLH} t_{PHL}	0.81 0.66	1.14 1.02	1.48 1.36	1.77 1.63	2.10 1.93
	From: SD To: Q	t_{PLH} t_{PHL}	1.59 1.68	1.86 2.03	2.19 2.35	2.50 2.62	2.85 2.91
	From: SE To: Q	t_{PLH} t_{PHL}	1.69 1.92	2.02 2.28	2.35 2.61	2.63 2.87	2.93 3.14
	From: SN To: Q	t_{PLH} t_{PHL}	1.29 0.91	1.68 1.33	2.03 1.71	2.31 2.03	2.62 2.36

	Number of Equivalent Loads		1	19	38	56	75 (max)
SLF034	From: C To: Q	t_{PLH} t_{PHL}	1.70 1.95	1.97 2.37	2.26 2.65	2.55 2.90	2.87 3.18
	From: D To: Q	t_{PLH} t_{PHL}	1.65 1.80	1.94 2.22	2.24 2.51	2.51 2.75	2.80 2.98
	From: RN To: Q	t_{PLH} t_{PHL}	1.26 2.16	1.59 2.77	1.91 3.22	2.21 3.59	2.54 3.95
	From: SCE To: Q	t_{PLH} t_{PHL}	0.86 0.71	1.17 1.11	1.49 1.41	1.78 1.66	2.09 1.91
	From: SD To: Q	t_{PLH} t_{PHL}	1.59 1.70	1.97 2.13	2.29 2.41	2.56 2.64	2.83 2.85
	From: SE To: Q	t_{PLH} t_{PHL}	1.74 1.96	2.01 2.32	2.33 2.61	2.64 2.86	2.97 3.12
	From: SN To: Q	t_{PLH} t_{PHL}	1.55 0.91	1.92 1.36	2.28 1.73	2.58 2.03	2.84 2.32
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
SLF036	From: C To: Q	t_{PLH} t_{PHL}	1.75 2.00	2.09 2.43	2.41 2.74	2.70 3.00	2.98 3.25
	From: D To: Q	t_{PLH} t_{PHL}	1.74 1.88	2.07 2.28	2.38 2.59	2.67 2.86	2.96 3.11
	From: RN To: Q	t_{PLH} t_{PHL}	1.36 2.58	1.73 3.28	2.05 3.73	2.33 4.11	2.60 4.44
	From: SCE To: Q	t_{PLH} t_{PHL}	0.90 0.70	1.21 1.14	1.52 1.47	1.82 1.77	2.11 2.04
	From: SD To: Q	t_{PLH} t_{PHL}	1.72 1.82	2.08 2.24	2.38 2.54	2.67 2.81	2.95 3.06
	From: SE To: Q	t_{PLH} t_{PHL}	1.83 2.05	2.10 2.40	2.41 2.74	2.75 3.07	3.10 3.37
	From: SN To: Q	t_{PLH} t_{PHL}	1.86 1.03	2.34 1.52	2.66 1.88	2.92 2.21	3.15 2.52

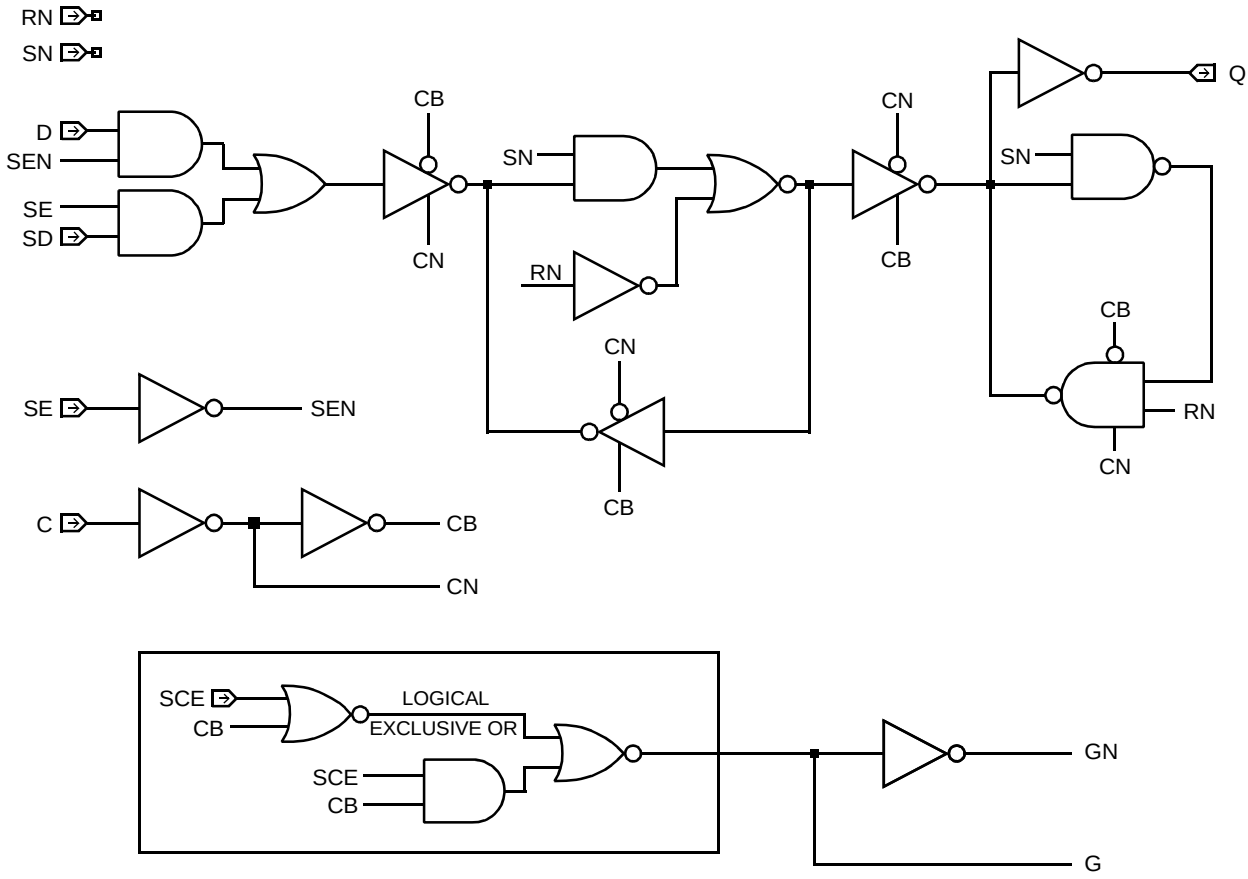
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF031	SLF032	SLF034	SLF036
Min C Width	High	t_w	1.29	1.29	1.36	1.41
Min C Width	Low	t_w	1.30	1.42	1.41	1.42
Min RN Width	Low	t_w	1.11	1.20	1.19	1.21
Min SN Width	Low	t_w	0.82	0.92	0.90	0.92
Min D Setup		t_{su}	1.11	1.23	1.22	1.24
Min D Hold		t_h	0.23	0.23	0.23	0.23
Min RN Setup		t_{su}	0.56	0.66	0.65	0.68
Min RN Hold		t_h	0.64	0.66	0.65	0.64
Min SCE Setup		t_{su}	0.92	0.92	0.99	1.06
Min SCE Hold		t_h	1.30	1.42	1.41	1.42
Min SD Setup		t_{su}	1.11	1.23	1.22	1.24
Min SD Hold		t_h	0.23	0.23	0.23	0.23
Min SE Setup		t_{su}	1.30	1.41	1.40	1.43
Min SE Hold		t_h	0.23	0.23	0.23	0.23
Min SN Setup		t_{su}	0.33	0.41	0.41	0.42
Min SN Hold		t_h	0.86	0.88	0.87	0.86

Logic Schematic

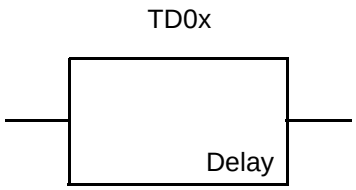


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

TD0x is a family of non-inverting time delays.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... TD0x *inst_name* (Q, A);

VHDL..... *inst_name*: TD0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	TD02	TD03	TD08
A	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
TD02	4.2	1.481	12.1
TD03	6.0	1.740	16.1
TD08	11.8	3.573	40.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

TD02	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	2.208 2.192	2.527 2.511	2.852 2.806	3.134 3.051	3.439 3.309
TD03	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	3.317 3.317	3.963 3.849	4.649 4.445	5.254 4.983	5.918 5.581
TD08	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	8.697 9.078	8.969 9.408	9.294 9.491	9.596 9.532	9.940 9.564

Delay will vary with input conditions. See page 2-15 for interconnect estimates.