0.5 Micron CMOS Core Library
Standard Cell Datasheets
AMI500MXSC 2.5 Volt
Section 3
Revision 1.1

Simple Gates

Complex Gates

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AMI500MXSC 0.5 micron CMOS Standard Cell

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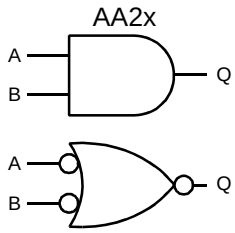
DATASHEETS

Description

AA2x is a family of 2-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... AA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: AA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	AA21	AA22	AA24	AA26
A	1.0	1.0	1.9	1.8
B	1.0	1.0	2.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA21	1.2	0.521	2.4
AA22	1.2	0.682	3.6
AA24	2.0	1.300	6.3
AA26	2.0	1.632	9.2

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

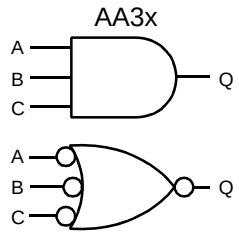
AA21	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.828 0.742	1.514 1.223	2.333 1.759	3.317 2.394	4.148 2.942
AA22	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.786 0.727	1.519 1.197	2.297 1.619	2.985 1.985	3.741 2.404
AA24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.631 0.552	1.377 1.020	2.071 1.381	2.722 1.705	3.419 2.059
AA26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.750 0.622	1.496 1.180	2.206 1.555	2.890 1.882	3.567 2.200

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AA3x is a family of 3-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

HDL Syntax

Verilog ..... AA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AA31	AA32	AA34	AA36
A	1.0	1.0	1.9	2.8
B	1.0	1.0	1.8	2.8
C	1.0	1.0	1.9	2.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA31	1.5	0.638	3.0
AA32	1.8	0.810	4.3
AA34	2.5	1.557	8.0
AA36	3.5	2.340	12.3

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

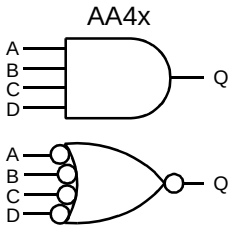
AA31	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.939 0.874	1.676 1.379	2.532 1.929	3.517 2.562	4.317 3.087
AA32	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.897 0.886	1.698 1.420	2.501 1.835	3.192 2.197	3.935 2.641
AA34	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.887 0.719	1.708 1.260	2.422 1.632	3.092 1.979	3.903 2.394
AA36	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.699 0.653	1.460 1.173	2.177 1.567	2.876 1.943	3.588 2.310

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AA4x is a family of 4-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

HDL Syntax

Verilog ..... AA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AA41	AA42	AA44	AA46
A	1.1	1.0	2.9	3.1
B	1.1	1.0	2.9	3.2
C	1.0	1.1	2.8	3.1
D	1.0	1.0	3.0	3.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQLpd (Eq-load)
AA41	2.0	0.741	3.3
AA42	2.0	0.902	4.5
AA44	4.8	2.333	11.8
AA46	5.2	2.654	13.6

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

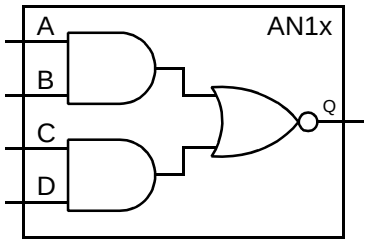
AA41	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.046 0.968	1.773 1.531	2.636 2.139	3.639 2.803	4.457 3.321
AA42	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.056 0.948	1.839 1.478	2.645 1.949	3.347 2.338	4.108 2.748
AA44	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.806 0.621	1.599 1.147	2.316 1.550	3.017 1.914	3.773 2.315
AA46	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.792 0.625	1.592 1.149	2.290 1.459	2.968 1.791	3.644 2.151

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN1x is a family of AND-NOR circuits consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

HDL Syntax

Verilog ..... AN1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN11	AN12	AN14	AN16
A	1.1	1.0	1.1	1.9
B	1.0	1.0	1.0	1.8
C	1.0	1.0	1.1	1.8
D	1.1	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN11	1.5	0.477	2.4
AN12	2.5	1.151	6.3
AN14	3.0	1.332	8.0
AN16	3.2	2.517	13.6

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

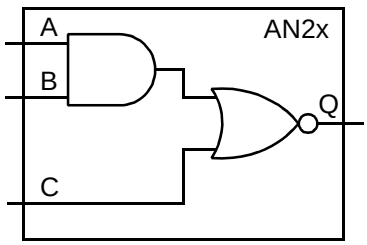
AN11	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.032 0.649	1.783 0.969	2.830 1.420	3.508 1.718	4.520 2.161
AN12	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.168 1.181	1.865 1.658	2.687 2.225	3.670 2.887	4.514 3.429
AN14	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.231 1.250	1.965 1.743	2.757 2.199	3.461 2.577	4.237 2.977
AN16	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.821 0.819	1.522 1.270	2.205 1.643	2.859 1.972	3.585 2.314

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN2x is a family of AND-NOR circuits consisting of one 2-input AND gate and a direct input into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	Q
H	H	X	L
X	X	H	L
All other combinations			H

HDL Syntax

Verilog ..... AN2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AN2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AN21	AN22	AN24	AN26
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.8
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN21	1.2	0.420	1.9
AN22	2.5	1.025	6.2
AN24	2.8	1.196	7.6
AN26	3.2	2.096	13.0

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

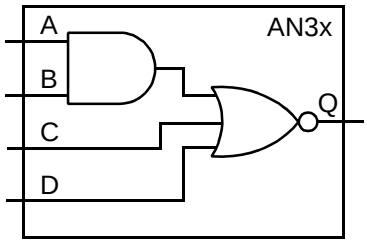
AN21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.588 0.693	1.288 1.176	2.214 1.821	2.798 2.238	3.666 2.870
AN22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.172 1.186	1.861 1.671	2.706 2.239	3.703 2.897	4.523 3.433
AN24	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.191 1.216	1.946 1.708	2.737 2.173	3.430 2.550	4.187 2.931
AN26	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.884 0.867	1.620 1.364	2.272 1.733	2.895 2.051	3.582 2.369

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN3x is a family of AND-NOR circuits consisting of one 2-input AND gate, and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... AN3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN31	AN32	AN34	AN36
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.8
C	1.0	1.0	1.0	1.8
D	1.0	1.1	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN31	1.5	0.577	2.2
AN32	2.8	1.047	6.5
AN34	2.8	1.211	7.6
AN36	3.8	2.321	14.8

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

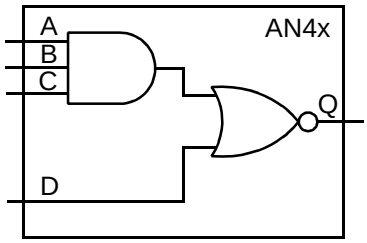
AN31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.953 0.795	1.402 1.080	2.235 1.551	3.037 1.989	3.838 2.446
AN32	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.172 1.209	1.860 1.691	2.703 2.261	3.701 2.925	4.527 3.467
AN34	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.123 1.171	1.846 1.653	2.619 2.100	3.303 2.471	4.054 2.863
AN36	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.873 0.913	1.569 1.380	2.283 1.758	2.952 2.081	3.653 2.400

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN4x is a family of AND-NOR circuits consisting of one 3-input AND gate, and a direct input into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
H	H	H	X	L
X	X	X	H	L
All other combinations				H

HDL Syntax

Verilog ..... AN4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN41	AN42	AN44	AN46
A	1.0	1.1	1.0	1.9
B	1.0	1.1	1.0	1.9
C	1.0	1.1	1.0	1.8
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN41	1.5	0.457	2.5
AN42	2.8	1.142	6.9
AN44	3.0	1.313	8.1
AN46	3.2	2.327	13.6

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

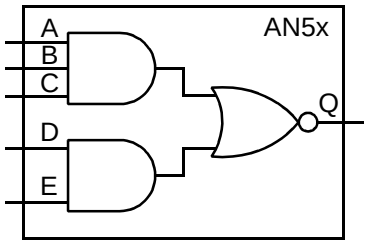
AN41	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.850 0.839	1.163 1.100	1.763 1.597	2.356 2.100	2.932 2.592
AN42	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.345 1.387	2.031 1.873	2.866 2.443	3.861 3.103	4.689 3.641
AN44	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.295 1.390	2.063 1.893	2.865 2.342	3.567 2.713	4.334 3.104
AN46	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.889 0.962	1.651 1.421	2.348 1.793	2.995 2.110	3.721 2.421

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN5x is a family of AND-NOR circuits consisting of one 3-input AND gate and one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN52	AN54	AN56
A	1.1	1.1	1.9
B	1.1	1.1	1.9
C	1.0	1.0	1.8
D	1.1	1.1	1.8
E	1.0	1.1	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN52	3.2	1.288	7.1
AN54	3.2	1.449	8.6
AN56	4.0	2.770	15.5

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

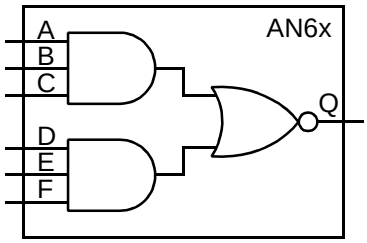
AN52	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.300 1.383	1.992 1.884	2.839 2.418	3.836 3.051	4.655 3.619
AN54	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.355 1.402	2.105 1.927	2.845 2.392	3.511 2.780	4.285 3.195
AN56	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.907 1.022	1.633 1.491	2.356 1.860	3.011 2.187	3.692 2.528

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN6x is a family of AND-NOR circuits consisting of two 3-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN62	AN64	AN66
A	1.1	1.0	1.9
B	1.1	1.0	1.9
C	1.1	1.0	1.9
D	1.0	1.1	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN62	3.2	1.399	7.7
AN64	3.8	1.576	8.8
AN66	4.2	2.975	15.8

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

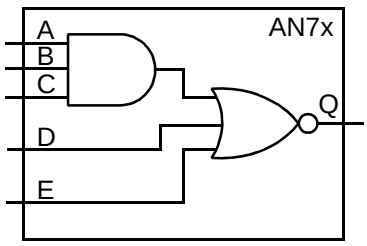
AN62	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.321 1.375	2.003 1.848	2.845 2.418	3.846 3.087	4.675 3.638
AN64	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.317 1.379	2.021 1.899	2.790 2.348	3.477 2.709	4.237 3.083
AN66	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.977 1.084	1.654 1.570	2.335 1.924	3.009 2.238	3.740 2.563

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN7x is a family of AND-NOR circuits consisting of one 3-input AND gate, and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN72	AN74	AN76
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.1	1.0	1.9
E	1.0	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN72	3.0	1.165	7.1
AN74	3.2	1.336	8.5
AN76	3.8	2.518	15.1

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

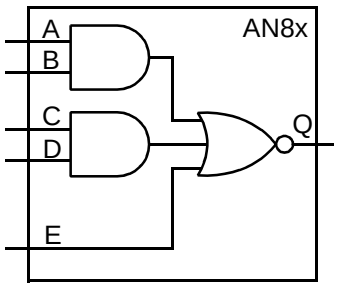
AN72	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.324 1.375	2.028 1.907	2.871 2.477	3.858 3.102	4.669 3.595
AN74	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.327 1.427	2.066 1.945	2.844 2.395	3.519 2.759	4.250 3.136
AN76	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.925 0.978	1.658 1.461	2.373 1.825	3.021 2.138	3.686 2.452

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN8x is a family of AND-NOR circuits consisting of two 2-input AND gates, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	X	X	X	L
X	X	H	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN82	AN84	AN86
A	1.1	1.0	1.9
B	1.0	1.0	1.9
C	1.1	1.0	1.9
D	1.1	1.1	1.9
E	1.0	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN82	3.5	1.462	8.9
AN84	4.0	1.643	10.5
AN86	4.5	3.096	17.8

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

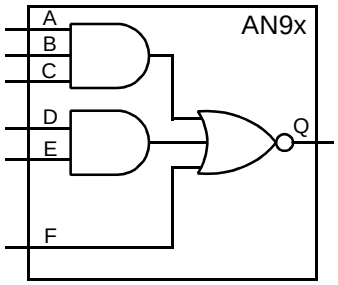
AN82	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.325 1.323	2.053 1.860	2.906 2.454	3.894 3.111	4.698 3.629
AN84	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.352 1.359	2.123 1.914	2.907 2.377	3.585 2.744	4.320 3.121
AN86	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.953 0.962	1.687 1.489	2.409 1.871	3.067 2.192	3.738 2.517

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN9x is a family of AND-NOR circuits consisting of one 3-input AND gate, one 2-input AND gate, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	X	L
X	X	X	X	X	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN9x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN9x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN92	AN94	AN96
A	1.1	1.0	1.8
B	1.1	1.0	1.8
C	1.0	1.1	1.8
D	1.0	1.1	1.9
E	1.0	1.1	1.8
F	0.9	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN92	4.0	1.592	9.5
AN94	4.2	1.760	11.0
AN96	4.8	3.324	18.2

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

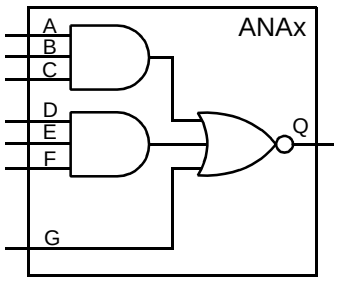
AN92	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.449 1.520	2.140 2.020	2.992 2.602	4.005 3.272	4.846 3.817
AN94	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.490 1.542	2.294 2.057	3.072 2.525	3.732 2.911	4.436 3.316
AN96	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.980 1.026	1.747 1.533	2.474 1.938	3.125 2.270	3.793 2.587

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANAx is a family of AND-NOR circuits consisting of two 3-input AND gates, and a direct input into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	H	X	L
X	X	X	X	X	X	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANAx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANA2	ANA4	ANA6
A	1.0	1.0	1.9
B	1.0	1.1	1.9
C	1.0	1.0	1.9
D	1.1	1.1	2.0
E	1.1	1.1	2.0
F	1.1	1.1	1.9
G	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANA2	4.2	1.706	10.3
ANA4	4.0	1.863	11.4
ANA6	4.8	3.538	19.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

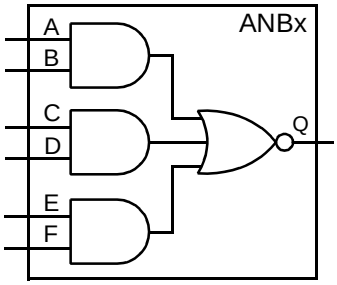
ANA2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.487 1.559	2.182 2.065	3.035 2.650	4.047 3.322	4.884 3.866
ANA4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.461 1.569	2.208 2.061	2.991 2.520	3.678 2.908	4.428 3.323
ANA6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.027 1.139	1.764 1.614	2.474 1.981	3.130 2.307	3.826 2.641

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANBx is a family of AND-NOR circuits consisting of three 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	X	X	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... ANBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ANBx port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ANB2	ANB4	ANB6
A	1.1	1.0	1.8
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.1	1.9
F	0.9	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANB2	3.8	1.599	9.1
ANB4	4.2	1.779	10.8
ANB6	4.8	3.357	18.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

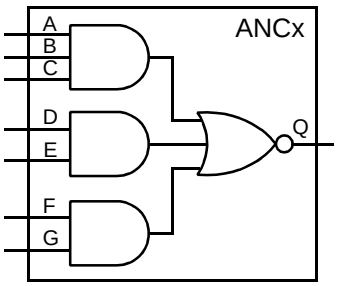
ANB2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.326 1.347	2.042 1.868	2.895 2.448	3.892 3.102	4.708 3.624
ANB4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.368 1.380	2.162 1.890	2.946 2.356	3.616 2.741	4.336 3.146
ANB6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.952 0.995	1.731 1.528	2.453 1.913	3.100 2.241	3.760 2.560

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANCx is a family of AND-NOR circuits consisting of one 3-input AND gate and two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	X	X	L
X	X	X	X	X	H	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANC2	ANC4	ANC6
A	1.0	1.0	1.8
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.9
G	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANC2	4.2	1.726	9.7
ANC4	4.2	1.886	11.1
ANC6	5.0	3.581	19.0

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

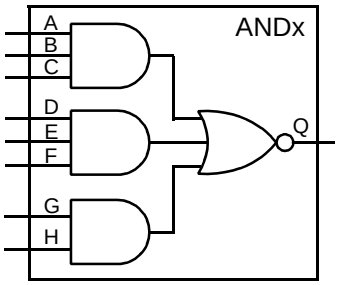
ANC2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.446 1.527	2.173 2.071	3.028 2.651	4.018 3.289	4.824 3.790
ANC4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.526 1.506	2.234 2.018	3.012 2.487	3.714 2.875	4.497 3.283
ANC6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.953 1.042	1.789 1.572	2.493 1.967	3.145 2.297	3.846 2.618

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANDx is a family of AND-NOR circuits consisting of two 3-input AND gates and one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
H	H	H	X	X	X	X	X	L
X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	H	H	L
All other combinations								H

HDL Syntax

Verilog ..... ANDx *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: ANDx port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads		
	AND2	AND4	AND6
A	1.1	1.0	1.8
B	1.1	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.1	2.0
E	1.0	1.1	1.9
F	1.0	1.1	1.9
G	1.0	1.0	2.0
H	1.1	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AND2	4.5	1.842	10.4
AND4	4.5	2.004	11.5
AND6	5.0	3.799	19.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

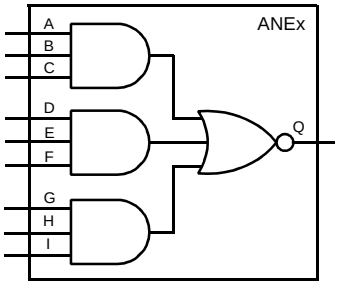
AND2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.461 1.544	2.182 2.093	3.036 2.675	4.032 3.311	4.847 3.810
AND4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.474 1.512	2.223 2.060	3.005 2.521	3.690 2.889	4.438 3.266
AND6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.846 1.051	1.706 1.594	2.395 1.999	3.044 2.340	3.779 2.680

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANEx is a family of AND-NOR circuits consisting of three 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L
All other combinations									H

HDL Syntax

Verilog ..... ANEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ANEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ANE2	ANE4	ANE6
A	1.1	1.0	1.8
B	1.1	1.0	1.8
C	1.0	1.1	1.8
D	1.1	1.1	1.9
E	1.1	1.1	1.9
F	1.1	1.1	1.9
G	1.1	1.1	1.9
H	1.1	1.1	1.9
I	1.0	1.1	1.9

AMI500MXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANE2	5.0	1.971	11.0
ANE4	5.2	2.141	12.6
ANE6	5.8	4.040	20.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

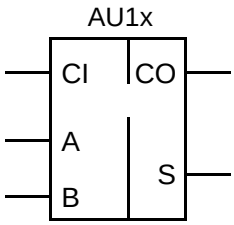
ANE2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.511 1.502	2.193 2.031	3.021 2.614	4.016 3.265	4.847 3.783
ANE4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.621 1.595	2.381 2.145	3.192 2.615	3.916 2.992	4.718 3.380
ANE6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.007 1.048	1.745 1.565	2.476 1.956	3.150 2.280	3.849 2.595

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AU1x is a family of combinational one-bit full adders.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

HDL Syntax

Verilog ..... AU1x *inst_name* (CO, S, A, B, CI);

VHDL..... *inst_name*: AU1x port map (CO, S, A, B, CI);

Pin Loading

Pin Name	Equivalent Loads	
	AU11	AU12
A	4.9	8.4
B	4.8	8.4
CI	3.7	6.5

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AU11	4.8	1.960	10.6
AU12	5.2	3.546	18.2

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

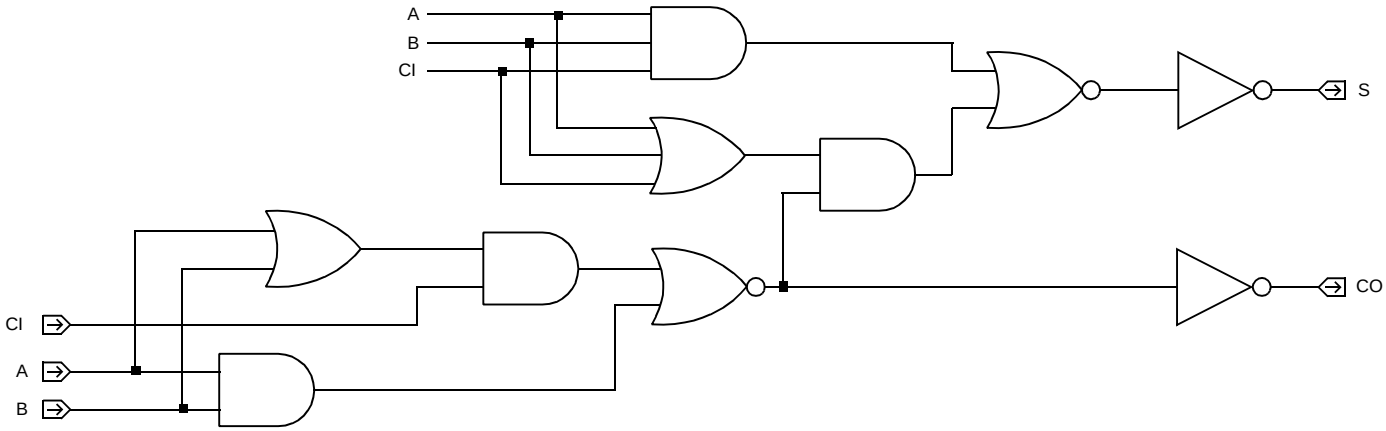
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
AU11	From: A To: S	t_{PLH} t_{PHL}	1.348 2.687	2.093 3.263	2.982 3.905	3.994 4.629	4.795 5.207
	From: B To: S	t_{PLH} t_{PHL}	1.315 2.939	2.038 3.572	2.890 4.216	3.878 4.903	4.684 5.435
	From: CI To: S	t_{PLH} t_{PHL}	1.213 2.898	2.024 3.591	2.926 4.226	3.930 4.865	4.728 5.342
	From: A To: CO	t_{PLH} t_{PHL}	1.180 1.992	1.967 2.704	2.859 3.391	3.862 4.103	4.663 4.645
	From: B To: CO	t_{PLH} t_{PHL}	1.271 1.962	2.003 2.660	2.857 3.336	3.843 4.039	4.645 4.574
	From: CI To: CO	t_{PLH} t_{PHL}	1.246 1.628	1.996 2.308	2.860 2.971	3.851 3.663	4.654 4.190
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
AU12	From: A To: S	t_{PLH} t_{PHL}	0.971 1.974	1.743 2.532	2.520 3.040	3.189 3.458	3.912 3.897
	From: B To: S	t_{PLH} t_{PHL}	0.904 2.113	1.671 2.738	2.449 3.237	3.122 3.626	3.850 4.020
	From: CI To: S	t_{PLH} t_{PHL}	0.918 2.073	1.695 2.716	2.490 3.229	3.179 3.623	3.927 4.017
	From: A To: CO	t_{PLH} t_{PHL}	0.918 1.310	1.681 1.953	2.473 2.480	3.164 2.896	3.917 3.319
	From: B To: CO	t_{PLH} t_{PHL}	0.902 1.329	1.665 1.970	2.458 2.452	3.152 2.833	3.909 3.235
	From: CI To: CO	t_{PLH} t_{PHL}	0.890 0.935	1.619 1.546	2.384 2.042	3.079 2.432	3.860 2.830

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic

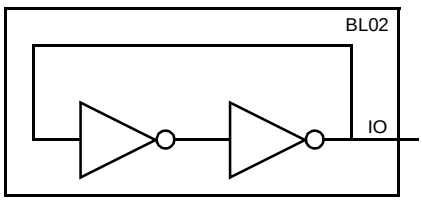


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

BL02 is a tristate bus latch that stores the final binary level on the bus when left undriven.

Logic Symbol



Truth Table

N/A

Pin Loading

	Equivalent Load
IO	1.5

Equivalent Gates 2.5

HDL Syntax

Verilog ..... BL02 *inst_name* (IO);

VHDL..... *inst_name*: BL02 port map (IO);

Size And Power Characteristics

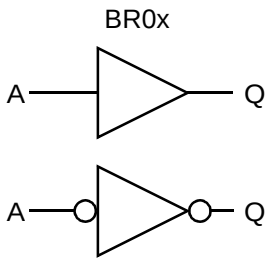
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.415	nA
EQL_{pd}	7.2	Eq-load

See page 2-13 for power equation.

Description

BR0x is a family of non-inverting bus receivers with a single output to be used as the output of tristate busses.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... BR0x *inst_name* (Q, A);

VHDL..... *inst_name*: BR0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	BR02	BR04	BR06
A	1.0	2.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
BR02	1.0	0.585	3.4
BR04	1.5	1.106	5.7
BR06	2.0	1.484	8.8

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

BR02	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.632 0.653	1.351 1.134	2.129 1.537	2.823 1.888	3.591 2.299
BR04	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.418 0.631	1.090 0.962	1.785 1.206	2.449 1.465	3.163 1.811
BR06	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.450 0.564	1.146 1.075	1.764 1.361	2.430 1.621	3.117 1.887

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

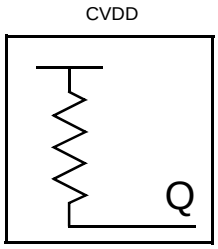
CVDD is the resistive tie-up to the core V_{DD} bus for all cell inputs.

Equivalent Gates 1.0

HDL Syntax

Verilog ..... CVDD *inst_name* (Q);

VHDL..... *inst_name*: CVDD port map (Q);



CVSS

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

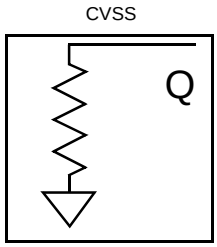
CVSS is the resistive tie-down to the core V_{SS} bus for all cell inputs.

Equivalent Gates 1.0

HDL Syntax

Verilog ..... CVSS *inst_name* (Q);

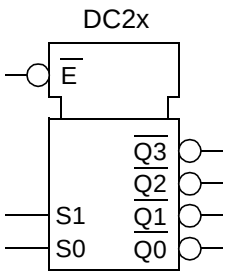
VHDL..... *inst_name*: CVSS port map (Q);



Description

DC2x is a family of two-to-four line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

HDL Syntax

Verilog ..... DC2x *inst_name* (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

VHDL..... *inst_name*: DC2x port map (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

Pin Loading

Pin Name	Equivalent Loads	
	DC21	DC22
S0	3.4	3.5
S1	3.4	3.5
EN	1.0	4.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC21	5.5	2.318	16.3
DC22	7.2	3.252	18.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

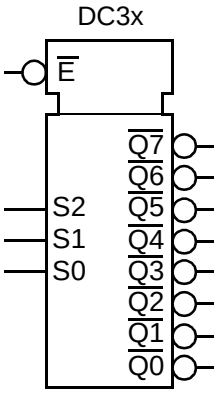
	Number of Equivalent Loads		1	2	4	6	8 (max)
DC21	From: Sx To: QN	t_{PLH} t_{PHL}	0.948 1.035	1.188 1.271	1.644 1.717	2.084 2.143	2.514 2.557
	From: EN To: QN	t_{PLH} t_{PHL}	1.415 1.361	1.653 1.596	2.104 2.050	2.538 2.490	2.961 2.922
	Number of Equivalent Loads		**1**	**5**	**10**	**16**	**21 (max)**
DC22	From: Sx To: QN	t_{PLH} t_{PHL}	0.832 1.405	1.526 2.064	2.366 2.705	3.359 3.375	4.178 3.885
	From: EN To: QN	t_{PLH} t_{PHL}	0.900 1.546	1.575 2.213	2.412 2.859	3.413 3.533	4.244 4.046

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

DC3x is a family of three-to-eight line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... DC3x *inst_name* (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

VHDL..... *inst_name* DC3x port map (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads	
	DC31	DC32
S0	6.1	6.6
S1	6.5	6.7
S2	5.7	5.8
EN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC31	12.3	5.021	40.3
DC32	17.0	7.616	58.5

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

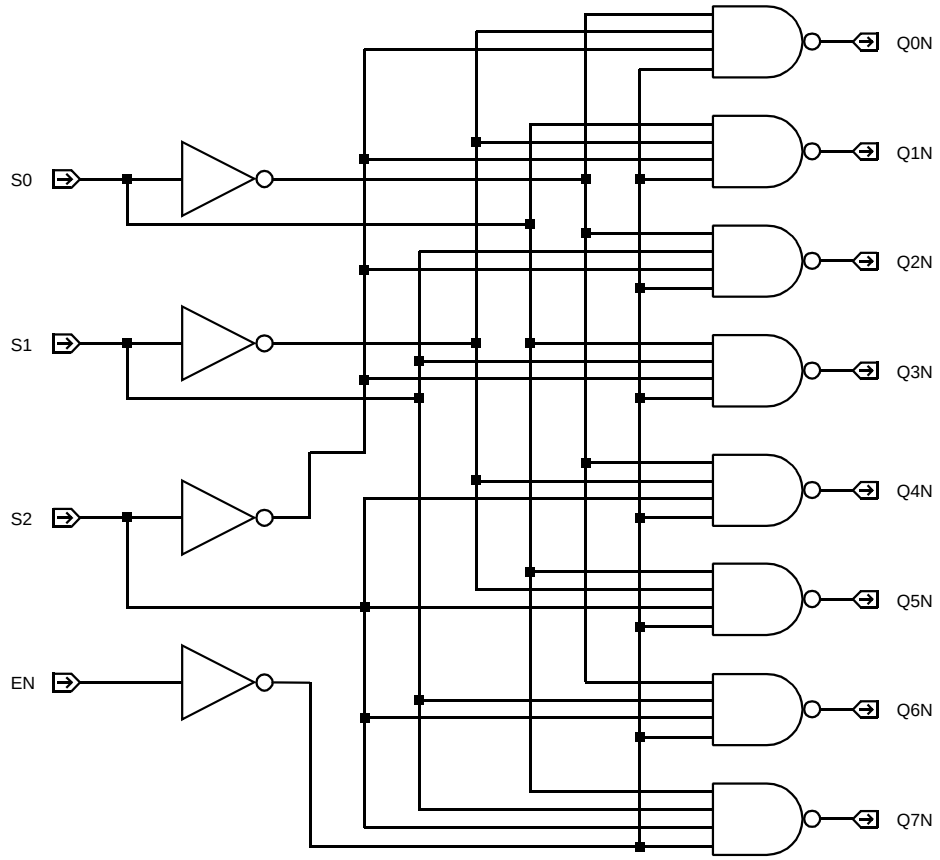
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	4	5	7 (max)
DC31	From: Sx To: QN	t_{PLH} t_{PHL}	1.244 1.462	1.527 1.765	2.047 2.306	2.293 2.559	2.767 3.043
	From: EN To: QN	t_{PLH} t_{PHL}	2.147 2.115	2.427 2.431	2.945 2.992	3.191 3.253	3.669 3.749
	Number of Equivalent Loads		**1**	**5**	**10**	**16**	**21 (max)**
DC32	From: Sx To: QN	t_{PLH} t_{PHL}	0.886 1.596	1.575 2.324	2.412 3.006	3.400 3.702	4.216 4.225
	From: EN To: QN	t_{PLH} t_{PHL}	2.983 3.166	3.689 3.908	4.537 4.587	5.531 5.272	6.347 5.783

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

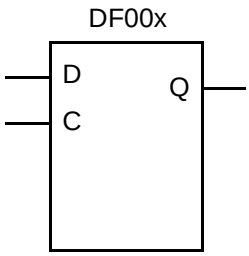
Logic Schematic



Description

DF00x is a family of static, master-slave D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q
H	↑	H
L	↑	L
X	L	NC

NC = No Change

HDL Syntax

Verilog ..... DF00x *inst_name* (Q, C, D);

VHDL..... *inst_name*: DF00x port map (Q, C, D);

Pin Loading

Pin Name	Equivalent Loads	
	DF001	DF002
D	1.1	1.1
C	1.1	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF001	4.0	1.419	8.1
DF002	4.0	1.594	9.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

DF001	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	1.907 1.567	2.597 2.060	3.436 2.646	4.426 3.330	5.242 3.889
DF002	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	1.845 1.554	2.575 2.123	3.346 2.598	4.024 2.975	4.767 3.362

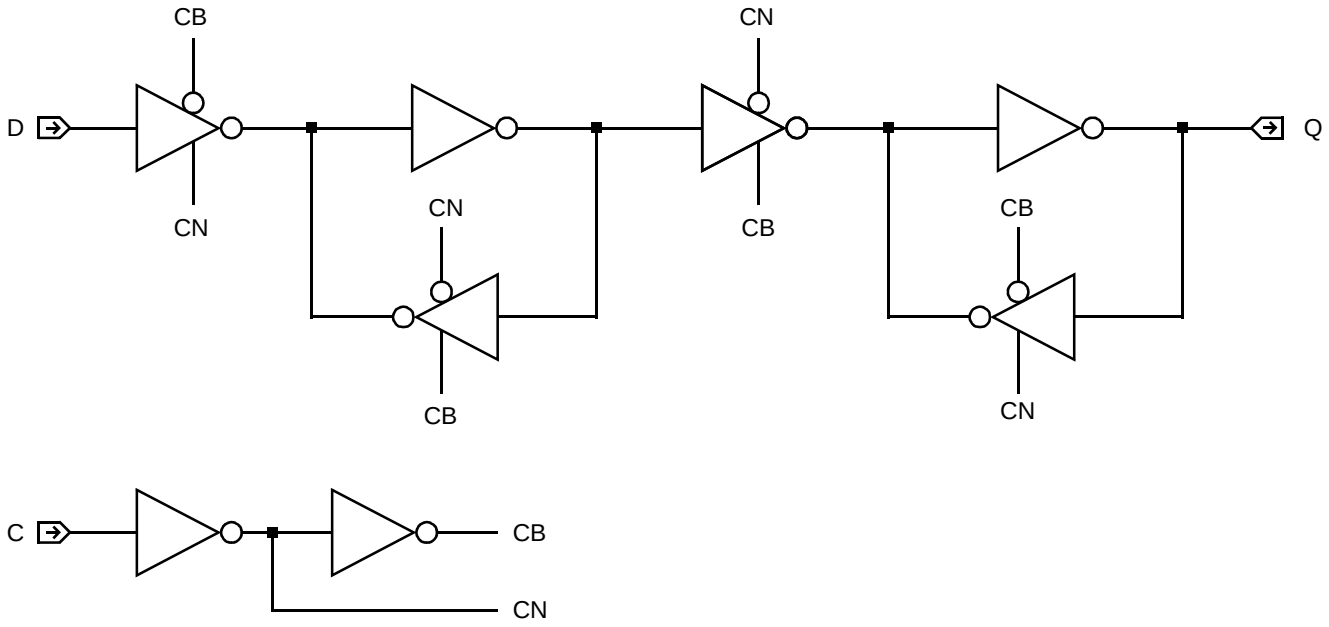
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF001	Cell DF002
Min C Width	High	t_w	1.920	1.894
Min C Width	Low	t_w	2.192	2.104
Min D Setup		t_{su}	1.249	1.265
Min D Hold		t_h	0.537	0.489

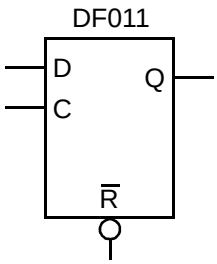
Logic Schematic



Description

DF011 is a static, master-slave D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q
L	X	X	L
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.1
C	1.1
RN	1.1

Equivalent Gates 5.2

HDL Syntax

Verilog ..... DF011 *inst_name* (Q, C, D, RN);

VHDL..... *inst_name*: DF011 port map (Q, C, D, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.028	nA
EQL_{pd}	12.9	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	2.407 1.762	3.012 2.070	3.929 2.480	4.543 2.735	5.468 3.103
RN	Q	t_{PHL}	1.095	1.379	1.747	1.986	2.327

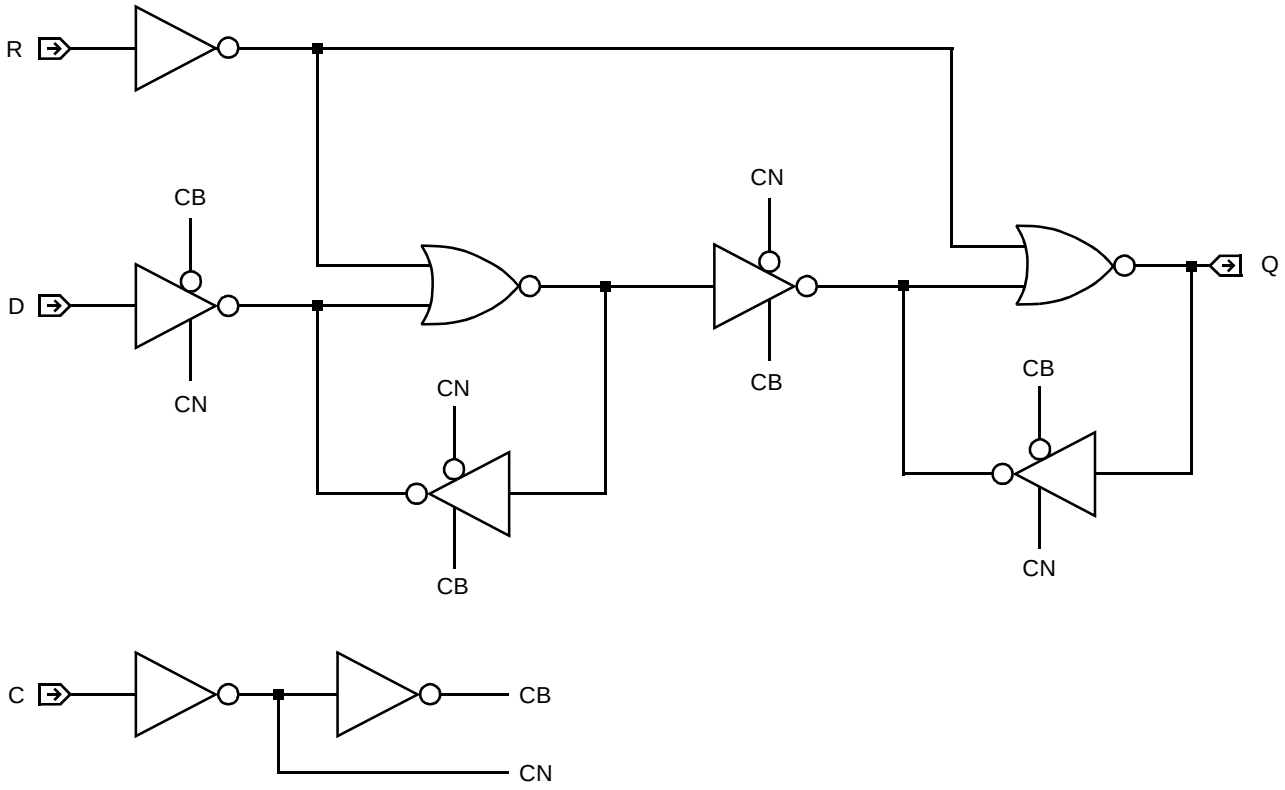
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	2.357
Min C Width	Low	t_w	2.306
Min RN Width	Low	t_w	2.613
Min D Setup		t_{su}	1.373
Min D Hold		t_h	0.522
Min RN Setup		t_{su}	1.118
Min RN Hold		t_h	1.590

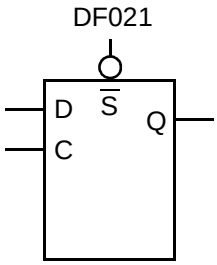
Logic Schematic



Description

DF021 is a static, master-slave D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q
L	X	X	H
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	1.1
SN	2.2

Equivalent Gates 4.8

HDL Syntax

Verilog.....DF021 *inst_name* (Q, C, D, SN);

VHDL..... *inst_name*: DF021 port map (Q, C, D, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.723	nA
EQL_{pd}	9.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	2.145 1.738	2.590 2.120	3.178 2.648	3.543 2.984	4.067 3.473
SN	Q	t_{PLH}	0.742	1.094	1.608	2.011	2.637

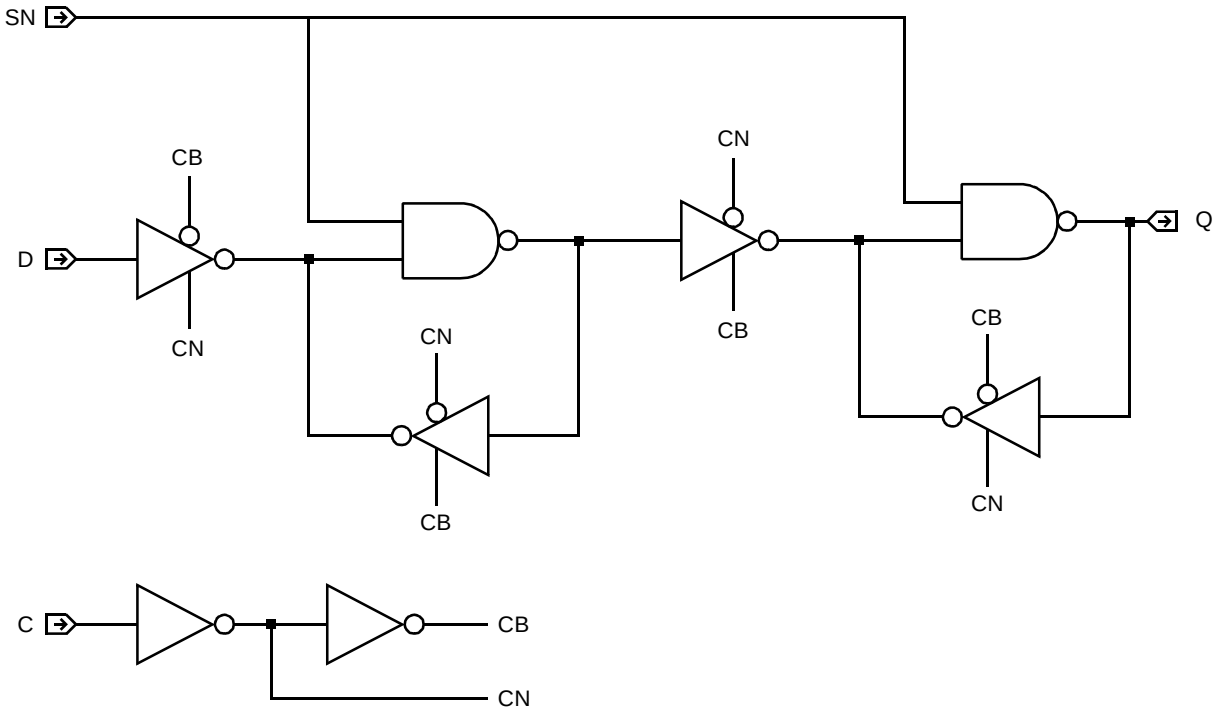
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	2.134
Min C Width	Low	t_w	2.232
Min SN Width	Low	t_w	1.758
Min D Setup		t_{su}	1.312
Min D Hold		t_h	0.510
Min SN Setup		t_{su}	0.521
Min SN Hold		t_h	1.893

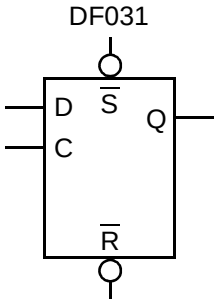
Logic Schematic



Description

DF031 is a static, master-slave D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	L	↑	L
H	H	H	↑	H
H	H	X	L	NC

NC = No Change
IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
C	1.1
SN	2.2
RN	1.0

Equivalent Gates 6.0

HDL Syntax

Verilog ..... DF031 *inst_name* (Q, D, RN, SN);

VHDL..... *inst_name*: DF031 port map (Q, D, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.937	nA
EQL_{pd}	13.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	2.365 1.755	3.102 2.114	4.220 2.689	4.969 3.086	6.098 3.695
RN	Q	t_{PHL}	1.160	1.566	2.117	2.473	3.004
SN	Q	t_{PLH}	0.657	1.024	1.500	1.799	2.245

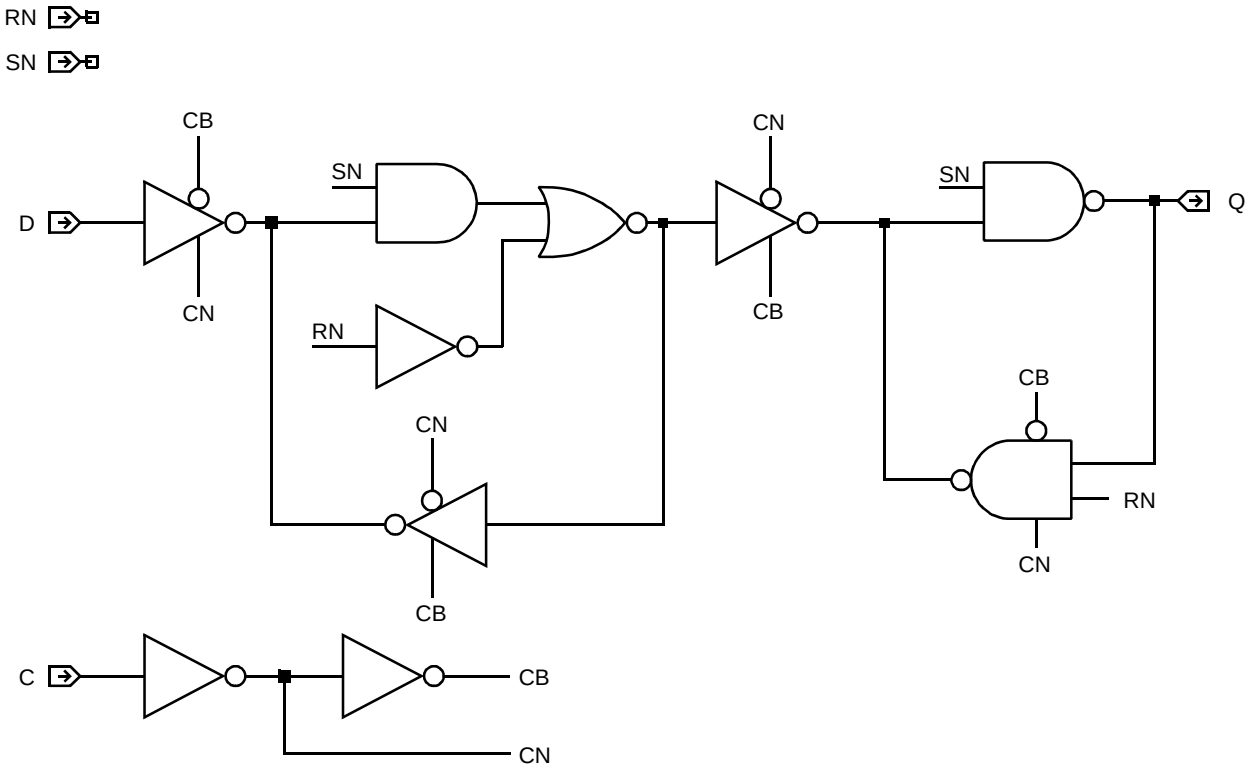
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	2.413
Min C Width	Low	t_w	2.370
Min RN Width	Low	t_w	2.661
Min SN Width	Low	t_w	1.832
Min D Setup		t_{su}	1.434
Min D Hold		t_h	0.529
Min RN Setup		t_{su}	1.282
Min RN Hold		t_h	1.548
Min SN Setup		t_{su}	0.634
Min SN Hold		t_h	1.943

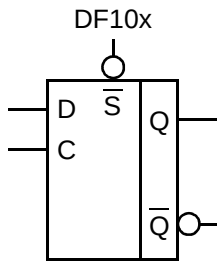
Logic Schematic



Description

DF10x is a family of static, master-slave D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF10x *inst_name* (Q, QN, C, D, SN);

VHDL.....*inst_name*: DF10x port map (Q, QN, C, D, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF101	DF102	DF104	DF106
D	1.0	1.0	1.1	1.0
C	1.1	1.1	1.1	1.1
SN	2.4	2.2	3.5	3.4

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
DF101	5.8	2.005	12.6
DF102	5.5	2.317	14.5
DF104	7.0	3.561	24.5
DF106	7.8	4.226	29.4

a. See page 2-13 for power equation.

Core Logic

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF101	From: C To: Q	t_{PLH} t_{PHL}	2.062 1.808	2.787 2.476	3.594 3.103	4.563 3.743	5.427 4.224
	From: C To: QN	t_{PLH} t_{PHL}	2.405 2.571	3.049 3.064	3.881 3.643	4.900 4.315	5.759 4.862
	From: SN To: Q	t_{PLH}	2.733	3.506	4.386	5.387	6.194
	From: SN To: QN	t_{PHL}	1.043	1.571	2.124	2.780	3.283
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF102	From: C To: Q	t_{PLH} t_{PHL}	2.017 1.735	2.778 2.405	3.559 2.922	4.238 3.319	4.975 3.717
	From: C To: QN	t_{PLH} t_{PHL}	2.622 2.648	3.242 3.218	3.988 3.650	4.683 3.981	5.473 4.311
	From: SN To: Q	t_{PLH}	3.004	3.763	4.567	5.277	6.055
	From: SN To: QN	t_{PHL}	0.963	1.503	1.943	2.331	2.746
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF104	From: C To: Q	t_{PLH} t_{PHL}	2.315 1.622	2.961 2.301	3.638 2.778	4.274 3.140	4.922 3.459
	From: C To: QN	t_{PLH} t_{PHL}	2.273 2.678	2.974 3.158	3.707 3.490	4.402 3.754	5.129 4.004
	From: SN To: Q	t_{PLH}	2.270	2.982	3.707	4.395	5.121
	From: SN To: QN	t_{PHL}	0.666	1.183	1.542	1.872	2.196
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF106	From: C To: Q	t_{PLH} t_{PHL}	2.131 1.730	3.038 2.542	3.709 2.970	4.349 3.338	4.999 3.691
	From: C To: QN	t_{PLH} t_{PHL}	2.716 2.811	3.260 3.325	3.914 3.706	4.637 4.046	5.419 4.366
	From: SN To: Q	t_{PLH}	2.542	3.429	4.180	4.878	5.546
	From: SN To: QN	t_{PHL}	0.825	1.300	1.628	1.965	2.296

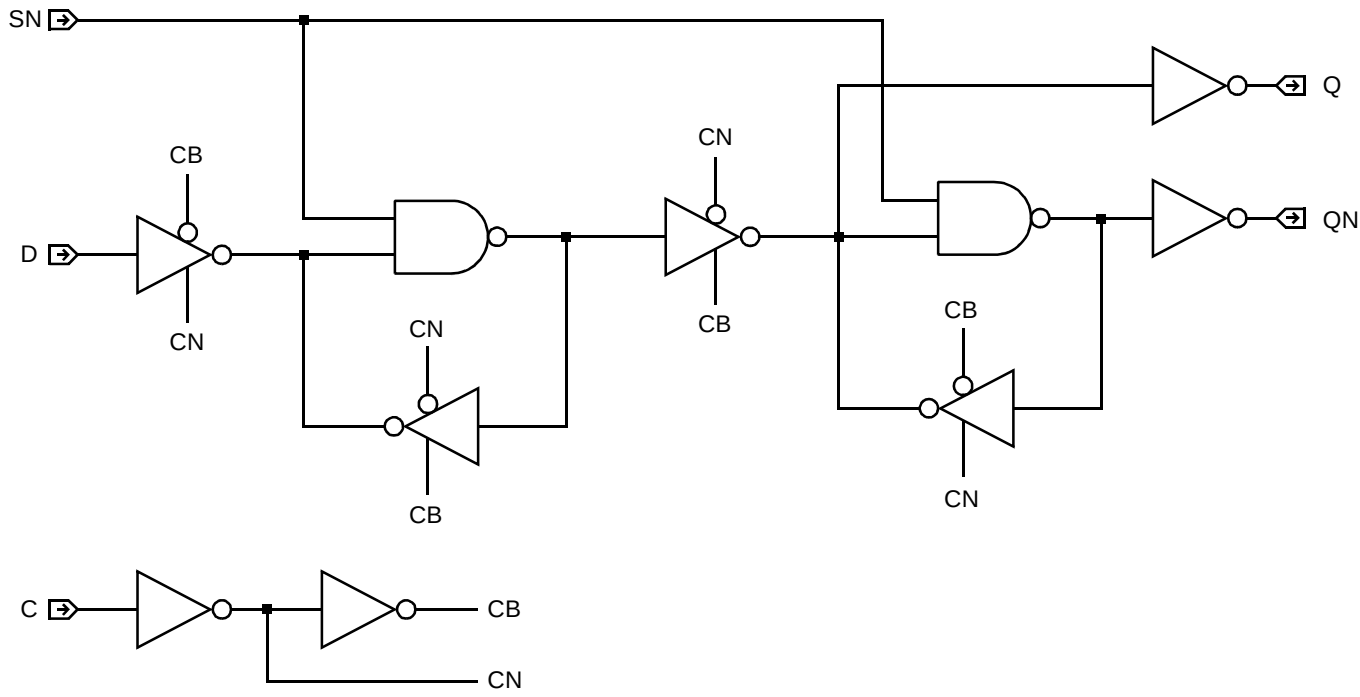
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF101	DF102	DF104	DF106
Min C Width	High	t_w	2.127	2.315	2.424	2.649
Min C Width	Low	t_w	2.268	2.201	2.556	2.526
Min SN Width		t_w	2.123	2.439	2.049	2.152
Min D Setup		t_{su}	1.358	1.311	1.490	1.466
Min D Hold		t_h	0.528	0.507	0.555	0.554
Min SN Setup		t_{su}	0.553	0.521	0.649	0.654
Min SN Hold		t_h	1.860	1.859	2.087	2.042

Logic Schematic

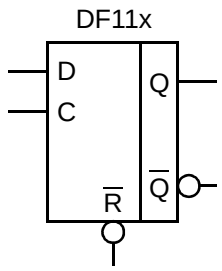


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DF11x is a family of static, master-slave D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF11x *inst_name* (Q, QN, C, D, RN);

VHDL.....inst_DF11x : DF11x port map (Q, QN, C, D, RN);

Pin Loading

Pin Name	Equivalent Loads			
	DF111	DF112	DF114	DF116
D	1.0	1.0	1.0	1.0
C	1.0	1.1	1.0	1.0
RN	1.0	1.1	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF111	6.2	2.335	15.0
DF112	6.0	2.676	17.8
DF114	7.8	3.991	27.1
DF116	8.5	4.720	32.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF111	From: C To: Q	t_{PLH} t_{PHL}	1.982 1.821	2.749 2.484	3.603 3.118	4.565 3.773	5.333 4.268
	From: C To: QN	t_{PLH} t_{PHL}	2.337 2.731	2.939 3.248	3.758 3.859	4.788 4.571	5.674 5.152
	From: RN To: Q	t_{PHL}	3.999	4.904	5.651	6.362	6.873
	From: RN To: QN	t_{PLH}	1.349	2.034	2.875	3.859	4.685
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF112	From: C To: Q	t_{PLH} t_{PHL}	2.009 1.745	2.765 2.450	3.545 2.964	4.225 3.351	4.964 3.734
	From: C To: QN	t_{PLH} t_{PHL}	2.632 2.901	3.302 3.532	4.038 4.012	4.698 4.378	5.430 4.745
	From: RN To: Q	t_{PHL}	4.148	5.172	5.808	6.257	6.682
	From: RN To: QN	t_{PLH}	1.344	2.058	2.822	3.495	4.246
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF114	From: C To: Q	t_{PLH} t_{PHL}	2.040 1.650	2.815 2.386	3.549 2.832	4.223 3.173	4.925 3.484
	From: C To: QN	t_{PLH} t_{PHL}	2.163 2.787	2.774 3.175	3.436 3.589	4.082 3.971	4.777 4.342
	From: RN To: Q	t_{PHL}	3.146	4.050	4.504	4.909	5.366
	From: RN To: QN	t_{PLH}	1.192	1.899	2.601	3.246	3.920
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF116	From: C To: Q	t_{PLH} t_{PHL}	2.167 1.739	2.890 2.483	3.589 2.944	4.289 3.316	4.993 3.636
	From: C To: QN	t_{PLH} t_{PHL}	2.592 3.057	3.113 3.601	3.759 3.898	4.455 4.214	5.185 4.558
	From: RN To: Q	t_{PHL}	3.499	4.336	4.927	5.431	5.885
	From: RN To: QN	t_{PLH}	1.319	1.940	2.603	3.284	3.981

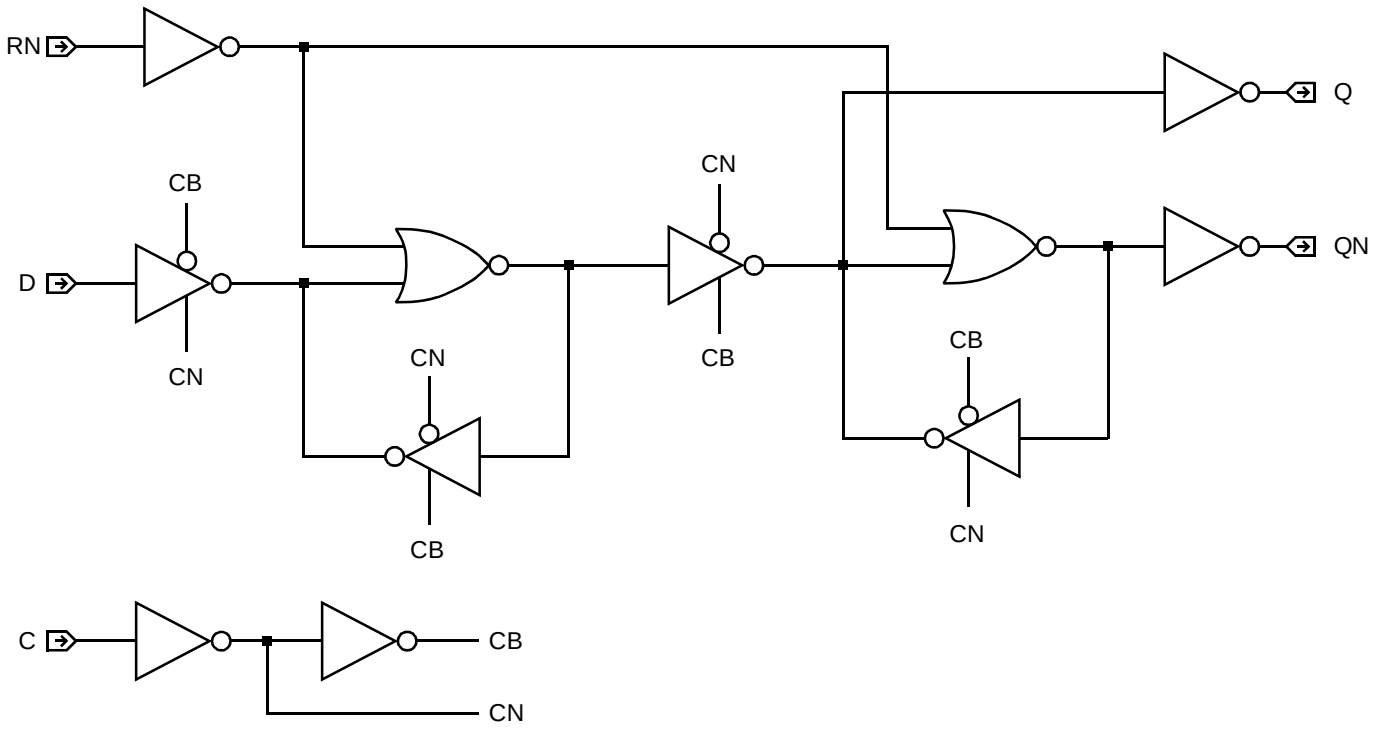
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF111	DF112	DF114	DF116
Min C Width	High	t_w	2.195	2.481	2.508	2.791
Min C Width	Low	t_w	2.158	2.179	2.456	2.458
Min RN Width		t_w	2.481	2.489	2.773	2.767
Min D Setup		t_{su}	1.327	1.320	1.423	1.423
Min D Hold		t_h	0.493	0.505	0.543	0.543
Min RN Setup		t_{su}	1.093	1.103	1.351	1.351
Min RN Hold		t_h	1.456	1.463	1.526	1.526

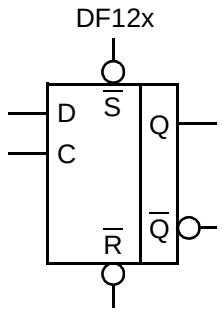
Logic Schematic



Description

DF12x is a family of static, master-slave D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DF12x *inst_name* (Q, QN, C, D, RN, SN);

VHDL..... *inst_name*: DF12x port map (Q, QN, C, D, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF121	DF122	DF124	DF126
D	1.0	1.0	1.0	1.0
C	1.1	1.1	1.1	1.1
SN	2.2	2.3	2.4	2.2
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF121	7.0	2.305	16.5
DF122	7.0	2.630	19.0
DF124	8.0	3.613	26.9
DF126	9.0	4.304	32.3

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF121	From: C To: Q	t_{PLH} t_{PHL}	2.049 1.809	2.766 2.446	3.609 3.113	4.607 3.808	5.444 4.320
	From: C To: QN	t_{PLH} t_{PHL}	2.545 3.049	3.132 3.676	3.956 4.310	5.013 4.985	5.934 5.505
	From: SN To: Q	t_{PLH}	2.713	3.423	4.309	5.368	6.250
	From: SN To: QN	t_{PHL}	1.021	1.540	2.106	2.752	3.286
	From: RN To: Q	t_{PHL}	4.033	4.856	5.641	6.451	7.063
	From: RN To: QN	t_{PLH}	1.487	2.224	3.084	4.074	4.897
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF122	From: C To: Q	t_{PLH} t_{PHL}	2.059 1.790	2.820 2.493	3.604 3.026	4.288 3.434	5.031 3.841
	From: C To: QN	t_{PLH} t_{PHL}	2.756 3.187	3.457 3.876	4.215 4.387	4.890 4.774	5.634 5.158
	From: SN To: Q	t_{PLH}	3.108	3.943	4.757	5.448	6.189
	From: SN To: QN	t_{PHL}	0.941	1.498	1.931	2.296	2.722
	From: RN To: Q	t_{PHL}	4.360	5.335	6.027	6.542	7.048
	From: RN To: QN	t_{PLH}	1.480	2.240	3.030	3.721	4.474

DF124	Number of Equivalent Loads		1	19	38	56	75 (max)
	From: C To: Q	t_{PLH} t_{PHL}	3.528 2.972	4.089 3.415	4.772 3.798	5.450 4.168	6.181 4.577
	From: C To: QN	t_{PLH} t_{PHL}	2.265 2.454	3.047 2.966	3.747 3.391	4.364 3.756	4.985 4.115
	From: SN To: Q	t_{PLH}	1.384	2.075	2.779	3.425	4.142
	From: SN To: QN	t_{PHL}	3.226	3.816	4.207	4.514	4.802
	From: RN To: Q	t_{PHL}	1.890	2.438	2.862	3.195	3.532
	From: RN To: QN	t_{PLH}	4.818	5.479	6.150	6.766	7.407
DF126	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: C To: Q	t_{PLH} t_{PHL}	3.680 3.147	4.374 3.639	5.064 4.042	5.743 4.409	6.414 4.754
	From: C To: QN	t_{PLH} t_{PHL}	2.447 2.735	3.226 3.324	3.872 3.717	4.506 4.048	5.152 4.343
	From: SN To: Q	t_{PLH}	1.513	2.177	2.861	3.548	4.246
	From: SN To: QN	t_{PHL}	3.520	4.188	4.537	4.808	5.039
	From: RN To: Q	t_{PHL}	2.185	2.709	3.093	3.393	3.715
	From: RN To: QN	t_{PLH}	5.151	5.793	6.376	6.977	7.589

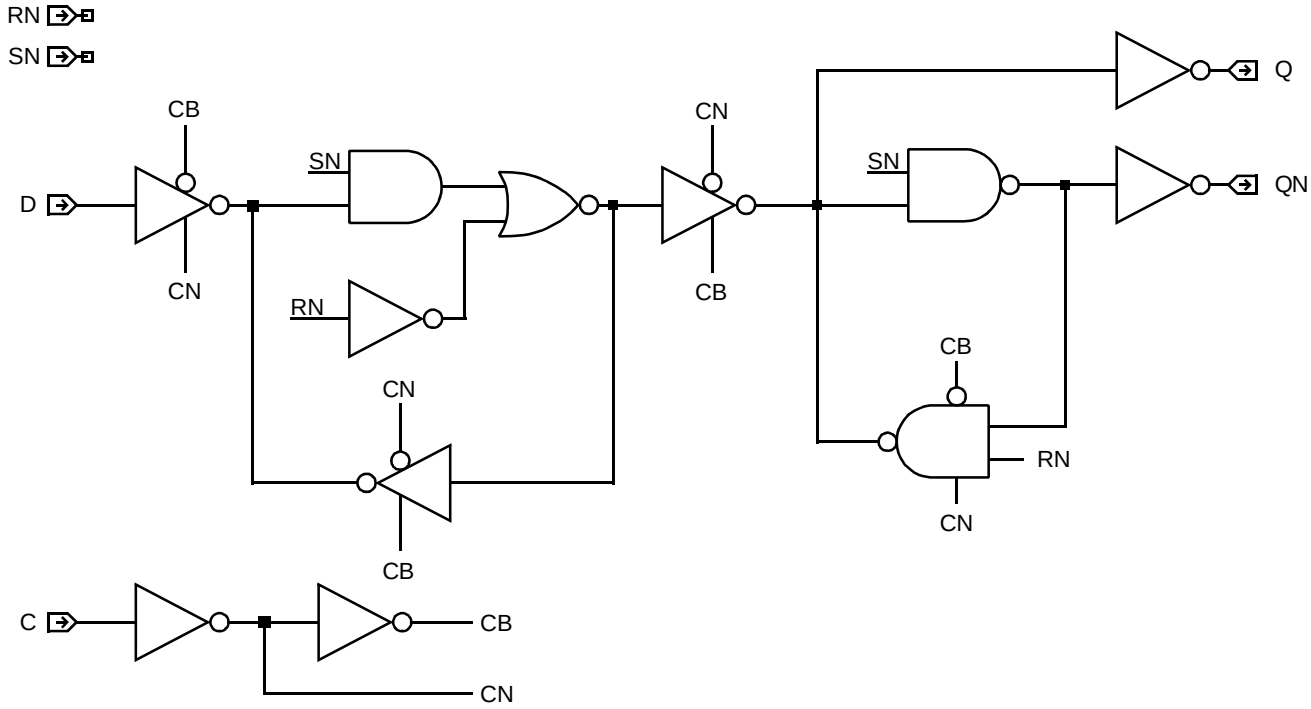
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF121	DF122	DF124	DF126
Min C Width	High	t_w	2.428	2.708	2.437	2.504
Min C Width	Low	t_w	2.304	2.314	2.294	2.327
Min RN Width	Low	t_w	2.570	2.573	2.587	2.608
Min SN Width	Low	t_w	2.124	2.527	2.185	2.204
Min D Setup		t_{su}	1.384	1.385	1.405	1.394
Min D Hold		t_h	0.528	0.529	0.516	0.532
Min RN Setup		t_{su}	1.245	1.254	1.323	1.267
Min RN Hold		t_h	1.499	1.496	1.451	1.513
Min SN Setup		t_{su}	0.622	0.625	0.664	0.625
Min SN Hold		t_h	1.885	1.895	1.834	1.904

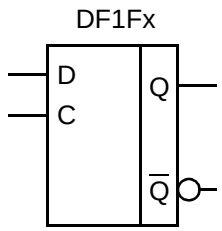
Logic Schematic



Description

DF1Fx is a family of static, master-slave D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
X	X	L	H
L	↑	L	H
H	↑	H	L
X	L	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF1Fx *inst_name* (Q, QN, C, D);

VHDL..... *inst_name*: DF1Fx port map (Q, QN, C, D)

Pin Loading

Pin Name	Equivalent Loads			
	DF1F1	DF1F2	DF1F4	DF1F6
D	1.1	1.1	1.0	1.0
C	1.1	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF1F1	5.2	1.823	11.9
DF1F2	5.0	2.161	13.7
DF1F4	6.0	3.215	20.9
DF1F6	6.8	4.131	28.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF1F1	From: C To: Q	t_{PLH} t_{PHL}	2.012 1.846	2.721 2.459	3.574 3.101	4.576 3.798	5.399 4.343
	From: C To: QN	t_{PLH} t_{PHL}	2.244 2.436	2.960 2.996	3.790 3.556	4.743 4.149	5.516 4.605
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF1F2	From: C To: Q	t_{PLH} t_{PHL}	1.947 1.717	2.677 2.377	3.467 2.896	4.170 3.299	4.945 3.705
	From: C To: QN	t_{PLH} t_{PHL}	2.430 2.441	3.088 2.945	3.833 3.382	4.509 3.734	5.264 4.098
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF1F4	From: C To: Q	t_{PLH} t_{PHL}	2.742 2.426	3.411 2.961	4.125 3.321	4.779 3.628	5.449 3.958
	From: C To: QN	t_{PLH} t_{PHL}	1.840 2.153	2.574 2.602	3.260 2.953	3.894 3.291	4.553 3.690
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF1F6	From: C To: Q	t_{PLH} t_{PHL}	2.819 2.497	3.411 2.877	4.069 3.199	4.747 3.545	5.437 3.912
	From: C To: QN	t_{PLH} t_{PHL}	2.059 1.943	2.695 2.599	3.317 3.032	3.973 3.370	4.696 3.649

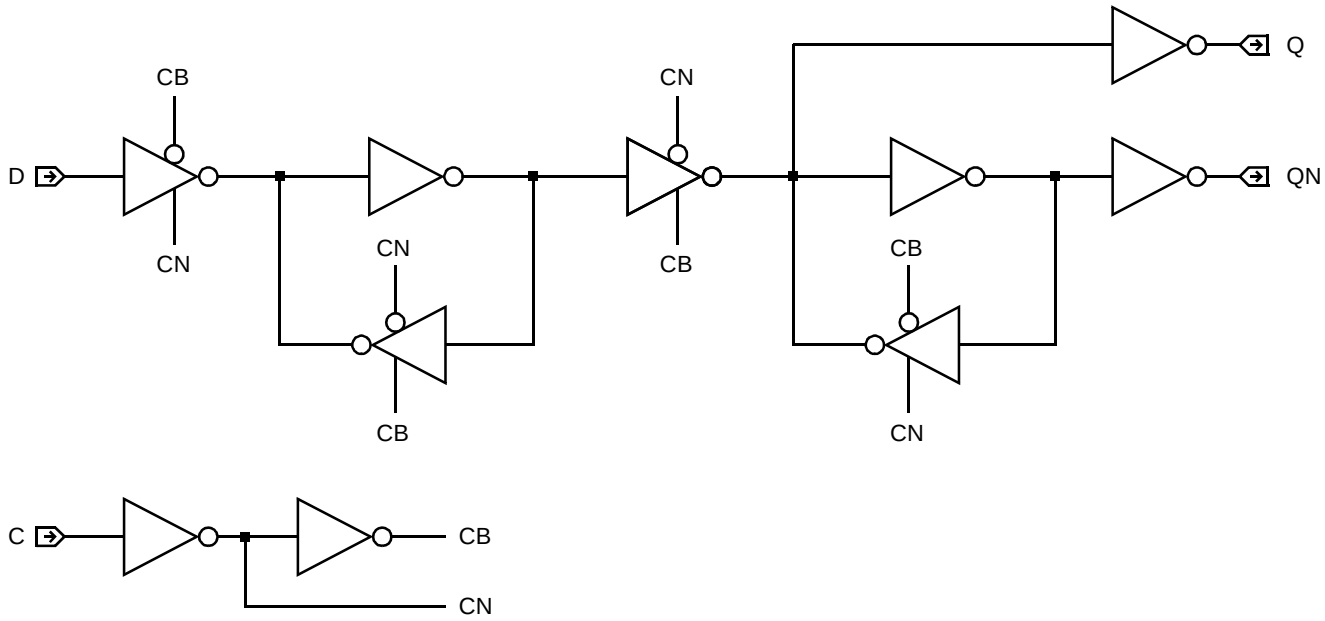
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF1F1	DF1F2	DF1F4	DF1F6
Min C Width	High	t_w	2.026	2.140	1.937	2.065
Min C Width	Low	t_w	2.129	2.065	2.076	2.046
Min D Setup		t_{su}	1.264	1.237	1.265	1.258
Min D Hold		t_h	0.504	0.497	0.491	0.489

Logic Schematic

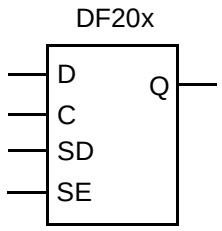


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DF20x is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q
↑	H	X	L	H
↑	L	X	L	L
↑	X	H	H	H
↑	X	L	H	L
L	X	X	X	NC

NC = No Change

HDL Syntax

Verilog ..... DF20x *inst_name* (Q, C, D, SD, SE);

VHDL..... *inst_name*: DF20x port map (Q, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads	
	DF201	DF202
C	1.0	1.0
D	1.0	1.0
SD	1.0	1.0
SE	2.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF201	5.2	2.000	13.4
DF202	5.2	2.010	13.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

DF201	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	2.078 1.660	2.753 2.219	3.591 2.802	4.593 3.432	5.427 3.925
DF202	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	1.883 1.551	2.564 2.100	3.346 2.582	4.060 2.973	4.862 3.379

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

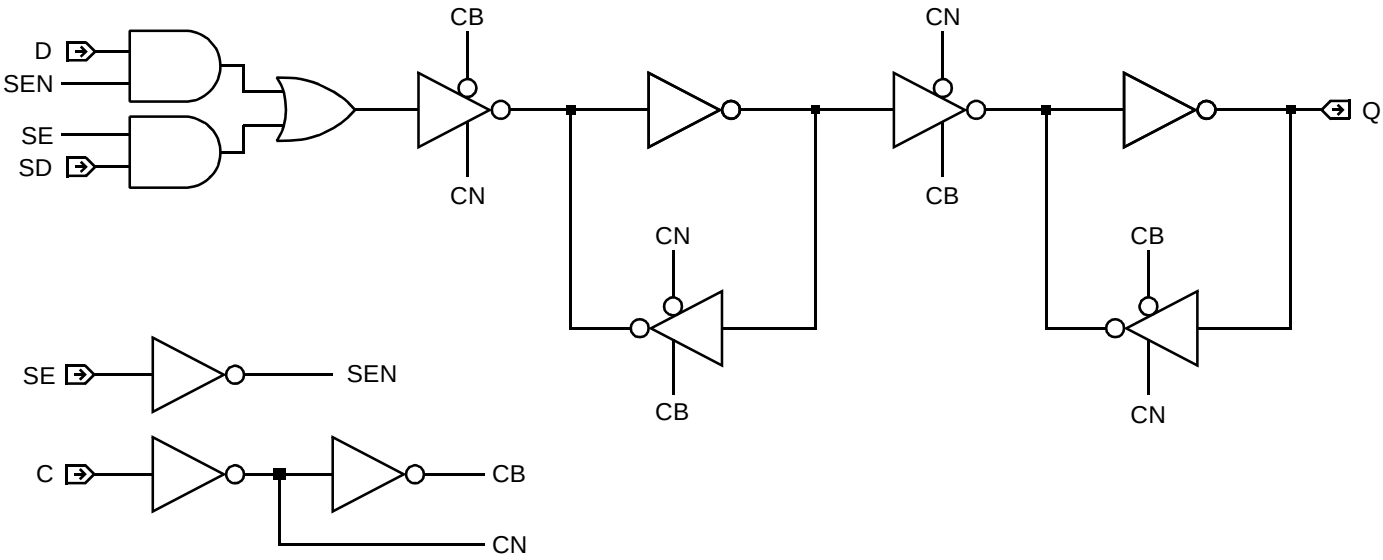
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			DF201	**DF202**
Min C Width	High	t_w	2.060	1.876
Min C Width	Low	t_w	3.157	2.892
Min D Setup		t_{su}	2.464	2.358
Min D Hold		t_h	0.534	0.518
Min SD Setup		t_{su}	2.464	2.358
Min SD Hold		t_h	0.534	0.518
Min SE Setup		t_{su}	2.809	2.700
Min SE Hold		t_h	0.534	0.518

AMI500MXSC 0.5 micron CMOS Standard Cell

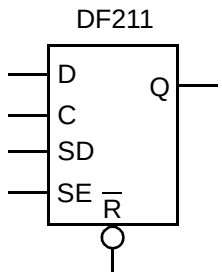
Logic Schematic



Description

DF211 is a static, master-slave, multiplexed scan D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q
↑	H	H	X	L	H
↑	L	H	X	L	L
↑	X	H	H	H	H
↑	X	H	L	H	L
X	X	L	X	X	L
L	X	H	X	X	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.1
D	1.0
RN	1.1
SD	1.0
SE	2.3

Equivalent Gates 6.2

HDL Syntax

Verilog ..... DF211 *inst_name* (Q, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF211 port map (Q, C, D, RN, SD, SE);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.517	nA
EQL_{pd}	17.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	2.399 1.778	3.042 2.077	3.958 2.484	4.552 2.741	5.426 3.114
RN	Q	t_{PHL}	1.112	1.389	1.760	2.007	2.363

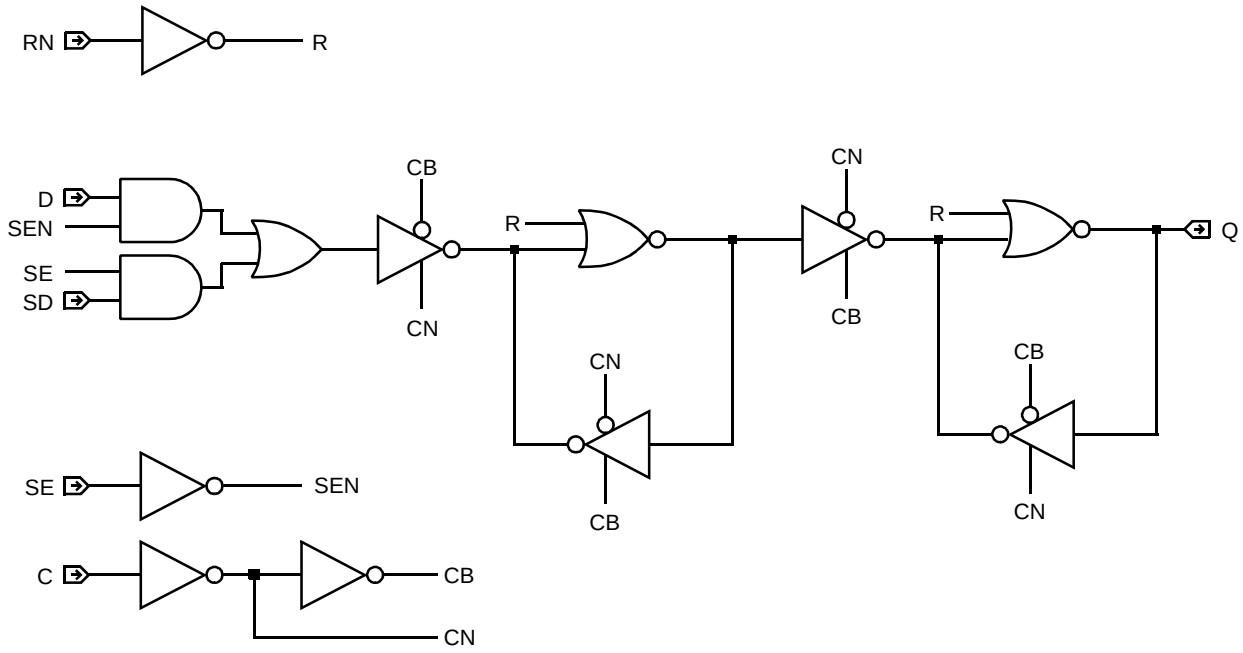
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	2.394
Min C Width	Low	t_w	3.257
Min RN Width	Low	t_w	1.885
Min D Setup		t_{su}	2.577
Min D Hold		t_h	0.532
Min SD Setup		t_{su}	2.577
Min SD Hold		t_h	0.532
Min SE Setup		t_{su}	2.920
Min SE Hold		t_h	0.532
Min RN Setup		t_{su}	1.194
Min RN Hold		t_h	1.108

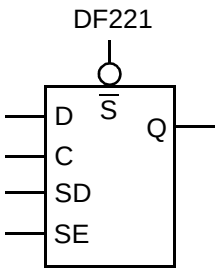
Logic Schematic



Description

DF221 is a static, master-slave, multiplexed scan D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q
↑	H	X	L	H	H
↑	L	X	L	H	L
↑	X	H	H	H	H
↑	X	L	H	H	L
X	X	X	X	L	H
L	X	X	X	H	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.0
D	1.0
SD	1.0
SE	2.3
SN	2.2

Equivalent Gates 5.8

HDL Syntax

Verilog ..... DF221 *inst_name* (Q, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF221 port map (Q, C, D, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.205	nA
EQL_{pd}	14.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
Delay (ns)			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	2.183 1.805	2.566 2.186	3.158 2.713	3.559 3.048	4.167 3.537
SN	Q	t_{PLH}	0.825	1.159	1.596	1.954	2.509

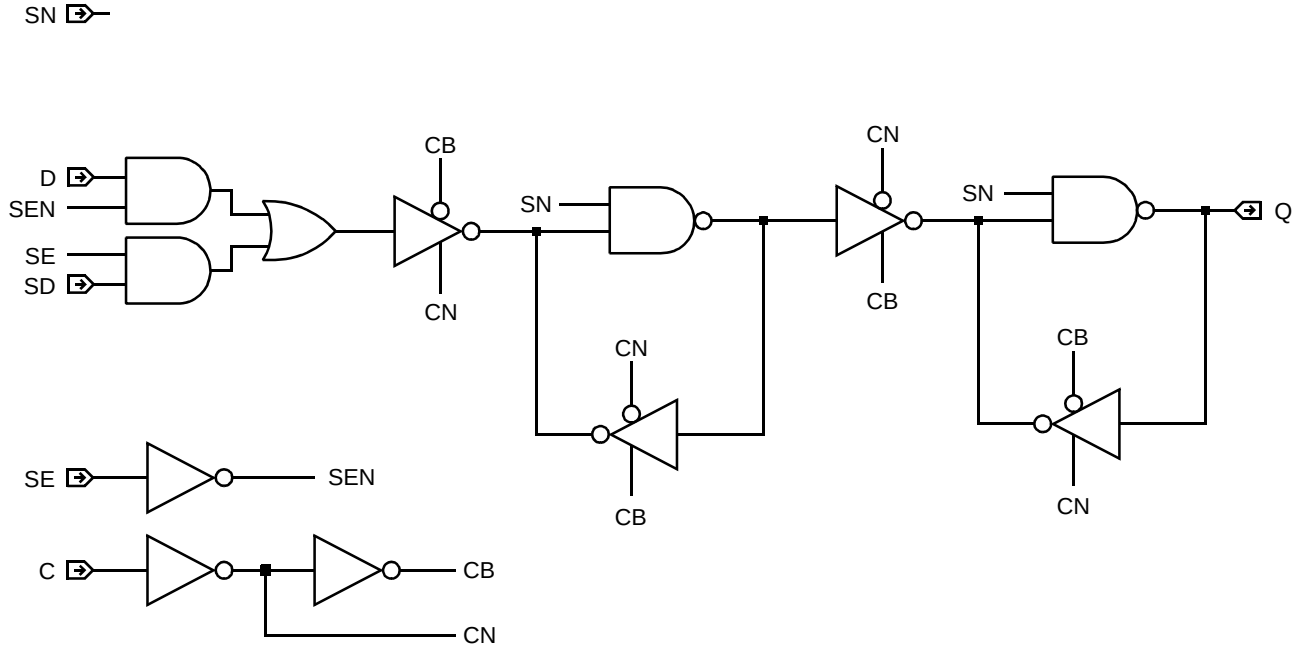
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	2.182
Min C Width	Low	t_w	3.257
Min SN Width	Low	t_w	1.460
Min D Setup		t_{su}	2.579
Min D Hold		t_h	0.531
Min SD Setup		t_{su}	2.579
Min SD Hold		t_h	0.531
Min SE Setup		t_{su}	2.923
Min SE Hold		t_h	0.531
Min SN Setup		t_{su}	0.577
Min SN Hold		t_h	1.562

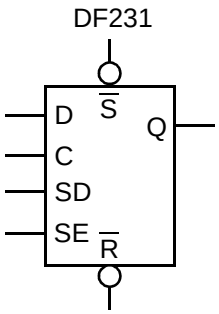
Logic Schematic



Description

DF231 is a static, master-slave, multiplexed scan D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q
↑	H	H	X	L	H	H
↑	L	H	X	L	H	L
↑	X	H	H	H	H	H
↑	X	H	L	H	H	L
X	X	L	X	X	H	L
X	X	H	X	X	L	H
X	X	L	X	X	L	IL
L	X	H	X	X	H	NC

NC = No Change

IL = Illegal Condition

Pin Loading

	Equivalent Load
C	1.1
D	1.0
RN	1.0
SD	1.0
SE	2.3
SN	2.4

Equivalent Gates 7.2

HDL Syntax

Verilog ..... DF231 *inst_name* (Q, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF231 port map (Q, C, D, RN, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.340	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	2.369 1.732	3.138 2.129	4.255 2.707	4.987 3.086	6.073 3.648
RN	Q	t_{PHL}	1.093	1.518	2.084	2.447	2.973
SN	Q	t_{PLH}	0.598	0.906	1.319	1.583	1.970

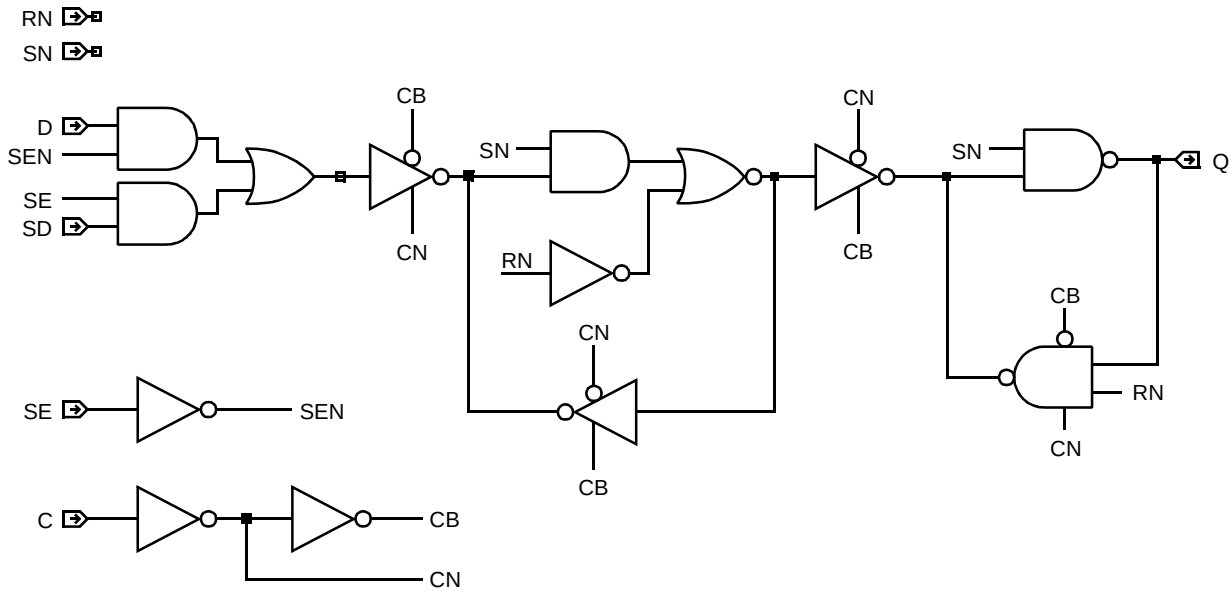
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	2.482
Min C Width	Low	t_w	3.073
Min RN Width	Low	t_w	2.675
Min SN Width	Low	t_w	1.891
Min D Setup		t_{su}	2.524
Min D Hold		t_h	0.527
Min SD Setup		t_{su}	2.524
Min SD Hold		t_h	0.527
Min SE Setup		t_{su}	2.864
Min SE Hold		t_h	0.527
Min RN Setup		t_{su}	1.295
Min RN Hold		t_h	1.590
Min SN Setup		t_{su}	0.659
Min SN Hold		t_h	1.927

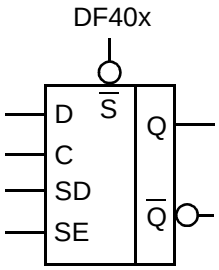
Logic Schematic



Description

DF40x is a family of static, master-slave, multiplexed scan D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q	QN
↑	H	X	L	H	H	L
↑	L	X	L	H	L	H
↑	X	H	H	H	H	L
↑	X	L	H	H	L	H
X	X	X	X	L	H	L
L	X	X	X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF40x *inst_name* (Q, QN, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF40x port map (Q, QN, C, D, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF401	DF402	DF404	DF406
C	1.0	1.1	1.1	1.1
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3
SN	2.1	2.2	3.3	3.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF401	6.8	2.573	17.5
DF402	6.8	2.897	20.0
DF404	8.5	3.954	27.4
DF406	9.2	4.636	32.8

a. See page 2-13 for power equation.

Core Logic

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF401	From: C To: Q	t_{PLH} t_{PHL}	2.171 1.895	2.819 2.535	3.666 3.164	4.709 3.852	5.592 4.383
	From: C To: QN	t_{PLH} t_{PHL}	2.482 2.757	3.218 3.272	4.057 3.855	5.010 4.509	5.816 5.083
	From: SN To: Q	t_{PLH}	1.868	2.608	3.462	4.440	5.239
	From: SN To: QN	t_{PHL}	1.093	1.632	2.218	2.851	3.371
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF402	From: C To: Q	t_{PLH} t_{PHL}	2.183 1.833	2.906 2.494	3.690 3.025	4.380 3.439	5.166 3.860
	From: C To: QN	t_{PLH} t_{PHL}	2.807 2.886	3.464 3.425	4.216 3.879	4.893 4.237	5.670 4.657
	From: SN To: Q	t_{PLH}	2.038	2.792	3.546	4.194	4.895
	From: S To: QN	t_{PHL}	1.043	1.608	2.041	2.411	2.830
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF404	From: C To: Q	t_{PLH} t_{PHL}	2.133 1.714	2.855 2.313	3.599 2.730	4.248 3.118	4.890 3.507
	From: C To: QN	t_{PLH} t_{PHL}	2.361 2.776	2.987 3.173	3.652 3.506	4.282 3.788	4.998 4.074
	From: SN To: Q	t_{PLH}	2.300	3.082	3.766	4.430	5.093
	From: SN To: QN	t_{PHL}	0.711	1.206	1.544	1.866	2.216
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF406	From: C To: Q	t_{PLH} t_{PHL}	2.287 1.778	3.049 2.552	3.755 2.973	4.412 3.316	5.112 3.630
	From: C To: QN	t_{PLH} t_{PHL}	2.714 2.817	3.229 3.273	3.931 3.620	4.610 3.928	5.384 4.214
	From: SN To: Q	t_{PLH}	2.598	3.333	4.043	4.732	5.409
	From: SN To: QN	t_{PHL}	0.847	1.357	1.642	1.968	2.326

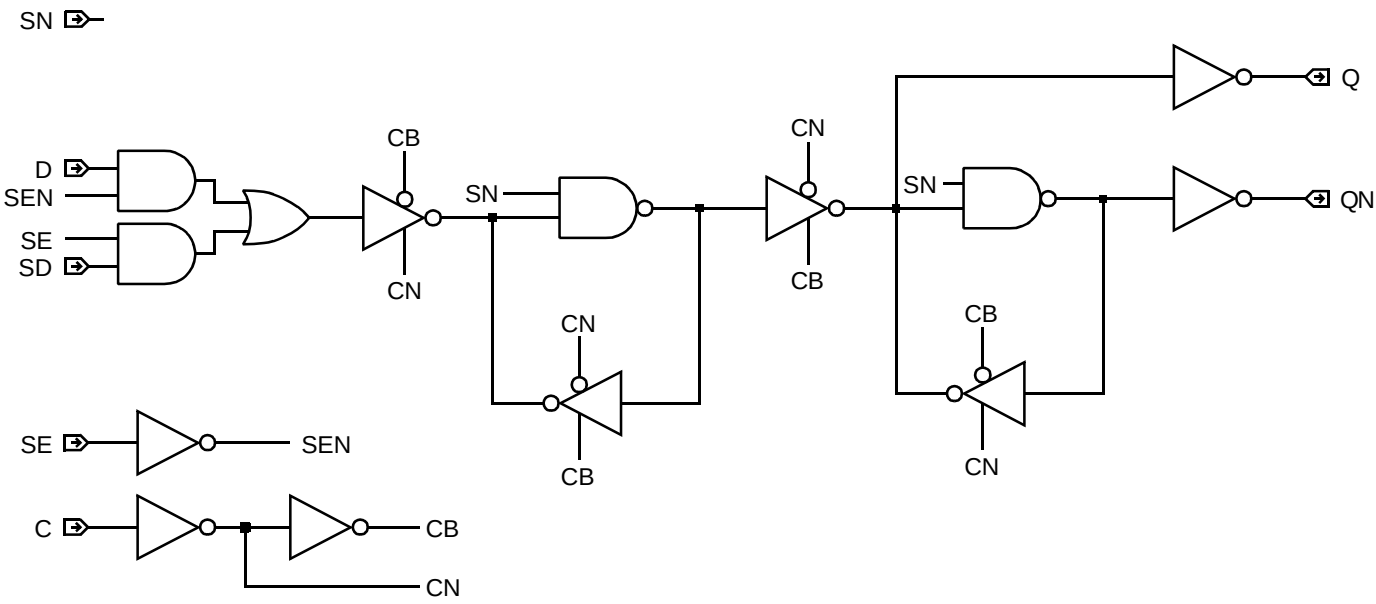
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF401	DF402	DF404	DF406
Min C Width	High	t_w	2.283	2.518	2.437	2.669
Min C Width	Low	t_w	3.255	3.268	3.325	3.324
Min SN Width	Low	t_w	1.482	1.688	2.104	2.140
Min D Setup		t_{su}	2.567	2.569	2.593	2.594
Min D Hold		t_h	0.533	0.535	0.555	0.555
Min SD Setup		t_{su}	2.567	2.569	2.593	2.594
Min SD Hold		t_h	0.533	0.535	0.555	0.555
Min SE Setup		t_{su}	2.913	2.915	2.939	2.937
Min SE Hold		t_h	0.533	0.535	0.555	0.555
Min SN Setup		t_{su}	0.576	0.576	0.656	0.656
Min SN Hold		t_h	1.558	1.572	2.133	2.132

Logic Schematic

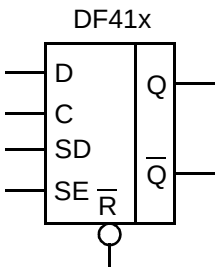


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DF41x is a family of static, master-slave, multiplexed scan D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q	QN
↑	H	H	X	L	H	L
↑	L	H	X	L	L	H
↑	X	H	H	H	H	L
↑	X	H	L	H	L	H
X	X	L	X	X	L	H
L	X	H	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF41x *inst_name* (Q, QN, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF41x port map (Q, QN, C, D, RN, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF411	DF412	DF414	DF416
C	1.1	1.1	1.1	1.1
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.1
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF411	7.2	2.910	20.5
DF412	7.2	3.257	23.0
DF414	9.0	4.405	31.3
DF416	10.0	5.147	37.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF411	From: C To: Q	t_{PLH} t_{PHL}	2.164 1.943	2.944 2.619	3.798 3.254	4.746 3.904	5.544 4.416
	From: C To: QN	t_{PLH} t_{PHL}	2.496 3.066	3.184 3.685	4.015 4.301	4.994 4.957	5.815 5.504
	From: RN To: Q	t_{PHL}	2.623	3.263	3.894	4.558	5.103
	From: RN To: QN	t_{PLH}	1.413	2.113	2.956	3.944	4.756
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF412	From: C To: Q	t_{PLH} t_{PHL}	2.168 1.889	2.890 2.559	3.675 3.089	4.374 3.502	5.145 3.918
	From: C To: QN	t_{PLH} t_{PHL}	2.794 3.172	3.397 3.755	4.134 4.269	4.824 4.683	5.614 5.142
	From: RN To: Q	t_{PHL}	2.637	3.295	3.811	4.215	4.628
	From: RN To: QN	t_{PLH}	1.371	2.085	2.857	3.536	4.285
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF414	From: C To: Q	t_{PLH} t_{PHL}	2.126 1.611	2.897 2.335	3.604 2.792	4.236 3.139	4.878 3.465
	From: C To: QN	t_{PLH} t_{PHL}	2.362 2.930	2.902 3.448	3.579 3.821	4.266 4.158	5.024 4.502
	From: RN To: Q	t_{PHL}	3.137	4.164	4.661	5.028	5.370
	From: RN To: QN	t_{PLH}	1.166	1.902	2.615	3.262	3.933
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF416	From: C To: Q	t_{PLH} t_{PHL}	2.246 1.753	3.054 2.520	3.764 2.996	4.424 3.363	5.053 3.669
	From: C To: QN	t_{PLH} t_{PHL}	2.720 3.080	3.224 3.608	3.875 4.036	4.528 4.404	5.256 4.720
	From: RN To: Q	t_{PHL}	3.634	4.629	5.046	5.419	5.804
	From: RN To: QN	t_{PLH}	1.287	1.984	2.646	3.313	3.987

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

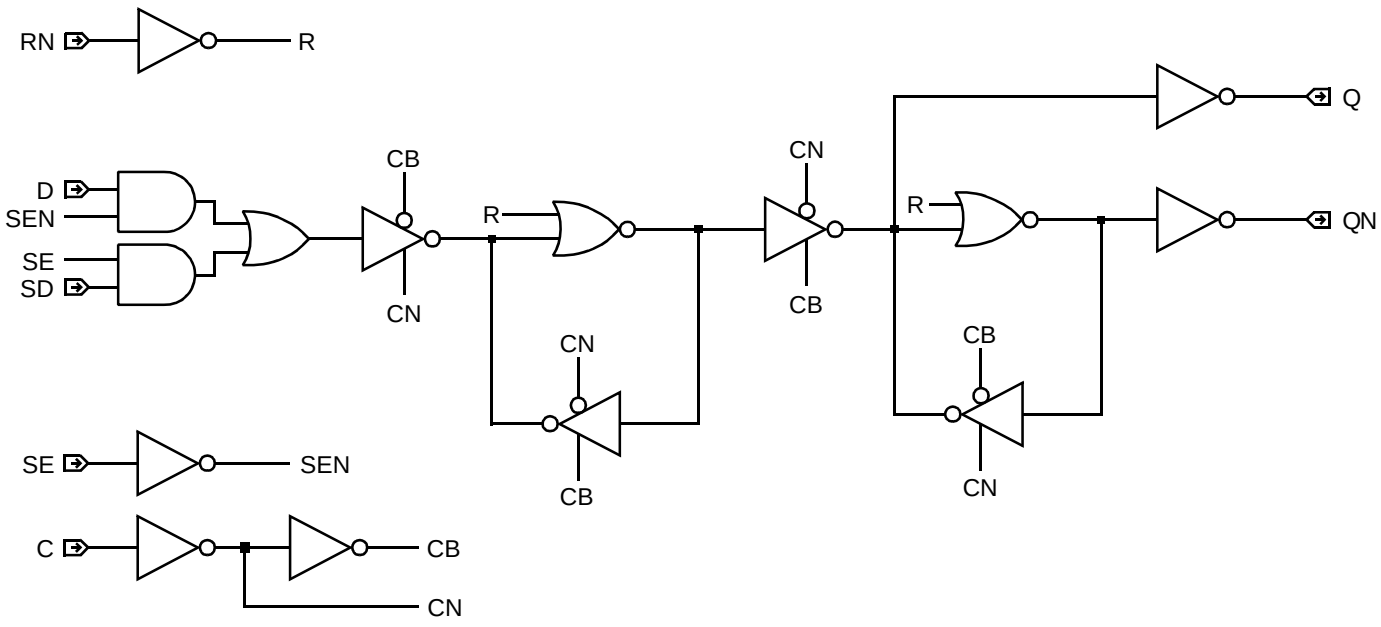
AMI500MXSC 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF411	DF412	DF414	DF416
Min C Width	High	t_w	2.460	2.712	2.572	2.866
Min C Width	Low	t_w	3.298	3.298	3.346	3.346
Min RN Width	Low	t_w	1.884	1.883	2.942	2.941
Min D Setup		t_{su}	2.596	2.596	2.612	2.613
Min D Hold		t_h	0.537	0.537	0.557	0.557
Min SD Setup		t_{su}	2.596	2.596	2.612	2.613
Min SD Hold		t_h	0.537	0.537	0.557	0.557
Min SE Setup		t_{su}	2.941	2.941	2.959	2.959
Min SE Hold		t_h	0.537	0.537	0.557	0.557
Min RN Setup		t_{su}	1.194	1.194	1.416	1.420
Min RN Hold		t_h	1.123	1.123	1.677	1.677

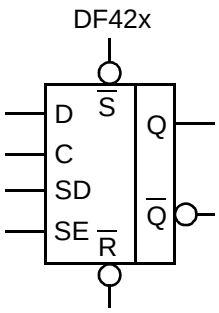
Logic Schematic



Description

DF42x is a family of static, master-slave, multiplexed scan D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	H	H	X	L	H	H	L
↑	L	H	X	L	H	L	H
↑	X	H	H	H	H	H	L
↑	X	H	L	H	H	L	H
X	X	L	X	X	H	L	H
X	X	H	X	X	L	H	L
X	X	L	X	X	L	IL	IL
L	X	H	X	X	H	NC	NC

NC = No Change IL = Illegal Condition

HDL Syntax

Verilog ..... DF421x *inst_name* (Q, QN, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF421x port map (Q, QN, C, D, RN, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF421	DF422	DF424	DF426
C	1.1	1.1	1.1	1.1
D	1.0	1.0	1.0	1.0
RN	1.1	1.1	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3
SN	2.4	2.4	2.4	2.5

AMI500MXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF421	8.2	2.709	20.4
DF422	8.2	3.031	23.0
DF424	9.5	4.027	30.4
DF426	10.2	4.709	36.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF421	From: C To: Q	t_{PLH} t_{PHL}	2.030 1.809	2.791 2.415	3.648 3.058	4.617 3.762	5.441 4.314
	From: C To: QN	t_{PLH} t_{PHL}	2.464 3.051	3.146 3.726	3.985 4.343	4.984 4.964	5.812 5.538
	From: RN To: Q	t_{PHL}	3.948	4.714	5.497	6.336	7.005
	From: RN To: QN	t_{PLH}	1.537	2.262	3.121	4.107	4.936
	From: SN To: Q	t_{PLH}	2.654	3.389	4.274	5.302	6.173
	From: SN To: QN	t_{PHL}	1.036	1.558	2.121	2.775	3.316
DF422	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	2.028 1.815	2.800 2.497	3.586 3.020	4.266 3.420	5.005 3.821
	From: C To: QN	t_{PLH} t_{PHL}	2.786 3.192	3.505 3.905	4.260 4.405	4.905 4.774	5.673 5.150
	From: RN To: Q	t_{PHL}	4.221	5.230	5.868	6.349	6.859
	From: RN To: QN	t_{PLH}	1.501	2.269	3.057	3.740	4.492
	From: SN To: Q	t_{PLH}	3.039	3.889	4.698	5.378	6.110
	From: SN To: QN	t_{PHL}	0.967	1.508	1.942	2.328	2.726

DF424	Number of Equivalent Loads		1	19	38	56	75 (max)
	From: C To: Q	t_{PLH} t_{PHL}	3.527 2.891	4.157 3.368	4.843 3.759	5.530 4.117	6.200 4.477
	From: C To: QN	t_{PLH} t_{PHL}	2.346 2.541	3.042 3.223	3.677 3.630	4.303 3.940	5.102 4.223
	From: RN To: Q	t_{PHL}	1.852	2.446	2.834	3.122	3.390
	From: RN To: QN	t_{PLH}	4.784	5.417	6.049	6.634	7.241
	From: SN To: Q	t_{PLH}	1.358	2.051	2.770	3.401	4.079
	From: SN To: QN	t_{PHL}	3.278	3.712	4.077	4.393	4.706
DF426	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: C To: Q	t_{PLH} t_{PHL}	3.835 3.138	4.539 3.652	5.225 4.041	5.859 4.382	6.500 4.756
	From: C To: QN	t_{PLH} t_{PHL}	2.407 2.643	3.168 3.242	3.874 3.638	4.595 3.984	5.320 4.283
	From: RN To: Q	t_{PHL}	2.137	2.795	3.155	3.450	3.713
	From: RN To: QN	t_{PLH}	5.059	5.564	6.174	6.793	7.507
	From: SN To: Q	t_{PLH}	1.555	2.273	2.945	3.634	4.371
	From: SN To: QN	t_{PHL}	3.498	3.923	4.316	4.689	5.051

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

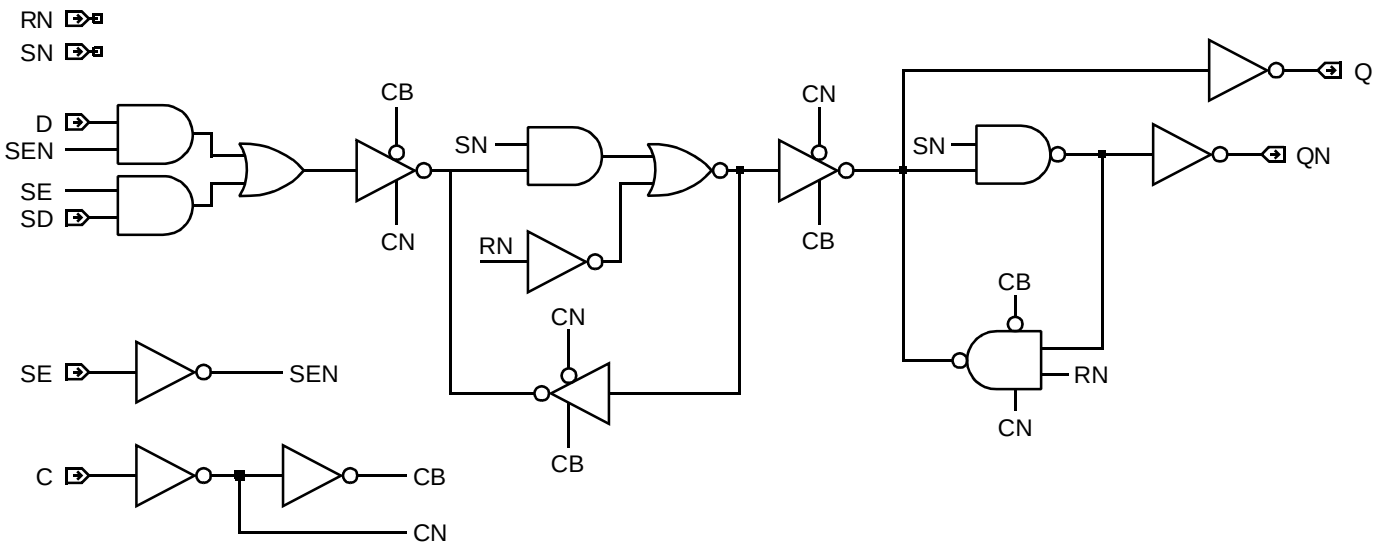
AMI500MXSC 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF421	DF422	DF424	DF426
Min C Width	High	t_w	2.408	2.695	2.449	2.508
Min C Width	Low	t_w	3.077	3.046	3.081	3.073
Min RN Width	Low	t_w	2.715	2.685	2.686	2.686
Min SN Width	Low	t_w	2.076	2.463	2.151	2.184
Min D Setup		t_{su}	2.532	2.511	2.532	2.521
Min D Hold		t_h	0.524	0.523	0.526	0.527
Min SD Setup		t_{su}	2.532	2.511	2.532	2.521
Min SD Hold		t_h	0.524	0.523	0.526	0.527
Min SE Setup		t_{su}	2.872	2.851	2.872	2.861
Min SE Hold		t_h	0.524	0.523	0.526	0.527
Min RN Setup		t_{su}	1.318	1.302	1.304	1.298
Min RN Hold		t_h	1.592	1.574	1.591	1.589
Min SN Setup		t_{su}	0.652	0.645	0.662	0.648
Min SN Hold		t_h	1.939	1.917	1.938	1.941

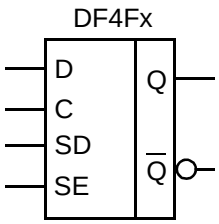
Logic Schematic



Description

DF4Fx is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q	QN
↑	H	X	L	H	L
↑	L	X	L	L	H
↑	X	H	H	H	L
↑	X	L	H	L	H
L	X	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF4Fx *inst_name* (Q, QN, C, D, SD, SE);

VHDL..... *inst_name*: DF4Fx port map (Q, QN, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF4F1	DF4F2	DF4F4	DF4F6
C	1.0	1.1	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.4	2.3	2.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF4F1	6.2	2.395	16.5
DF4F2	6.2	2.740	19.1
DF4F4	7.2	3.631	24.2
DF4F6	8.0	4.545	31.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DF4F1	From: C To: Q	t_{PLH} t_{PHL}	2.115 1.856	2.849 2.540	3.703 3.167	4.678 3.801	5.504 4.319
	From: C To: QN	t_{PLH} t_{PHL}	2.353 2.587	3.026 3.110	3.810 3.682	4.793 4.318	5.613 4.822
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DF4F2	From: C To: Q	t_{PLH} t_{PHL}	2.122 1.828	2.882 2.461	3.653 2.989	4.338 3.416	5.086 3.856
	From: C To: QN	t_{PLH} t_{PHL}	2.581 2.690	3.266 3.166	4.002 3.612	4.639 3.982	5.391 4.393
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DF4F4	From: C To: Q	t_{PLH} t_{PHL}	2.815 2.484	3.401 2.940	4.083 3.317	4.778 3.649	5.553 3.981
	From: C To: QN	t_{PLH} t_{PHL}	1.847 2.147	2.538 2.607	3.248 2.976	3.911 3.288	4.604 3.606
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DF4F6	From: C To: Q	t_{PLH} t_{PHL}	2.836 2.398	3.393 2.887	4.030 3.252	4.705 3.545	5.411 3.886
	From: C To: QN	t_{PLH} t_{PHL}	1.962 2.406	2.699 2.825	3.336 3.187	4.053 3.528	4.707 3.854

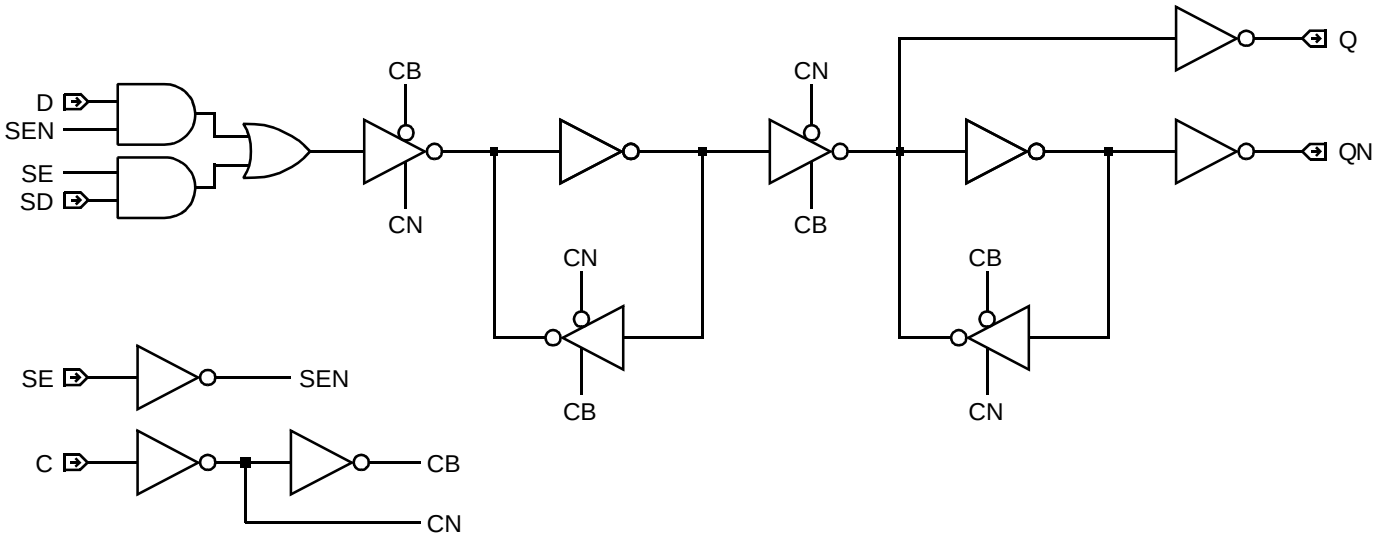
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF4F1	DF4F2	DF4F4	DF4F6
Min C Width	High	t_w	2.152	2.360	1.981	2.106
Min C Width	Low	t_w	3.093	3.156	2.877	2.877
Min D Setup		t_{su}	2.440	2.470	2.358	2.358
Min D Hold		t_h	0.522	0.531	0.512	0.512
Min SD Setup		t_{su}	2.440	2.470	2.358	2.358
Min SD Hold		t_h	0.522	0.531	0.512	0.512
Min SE Setup		t_{su}	2.783	2.814	2.700	2.700
Min SE Hold		t_h	0.522	0.531	0.512	0.512

Logic Schematic

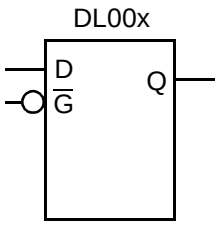


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DL00x is a family of transparent, unbuffered D latch with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

GN	D	Q
L	L	L
L	H	H
H	X	NC

NC = No Change

HDL Syntax

Verilog ..... DL00x *inst_name* (Q, D, GN);

VHDL..... *inst_name*: DL00x port map (Q, D, GN);

Pin Loading

Pin Name	Equivalent Loads	
	DL001	DL002
D	1.0	1.0
GN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL001	2.5	0.998	4.3
DL002	2.5	1.089	4.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DL001	From: D To: Q	t_{PLH} t_{PHL}	1.121 1.394	1.804 1.881	2.636 2.453	3.624 3.118	4.441 3.660
	From: GN To: Q	t_{PLH} t_{PHL}	1.511 1.958	2.165 2.492	2.980 3.078	3.974 3.732	4.813 4.252
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DL002	From: D To: Q	t_{PLH} t_{PHL}	1.044 1.282	1.788 1.860	2.547 2.327	3.236 2.692	4.025 3.064
	From: GN To: Q	t_{PLH} t_{PHL}	1.340 1.783	2.087 2.334	2.867 2.808	3.551 3.189	4.297 3.583

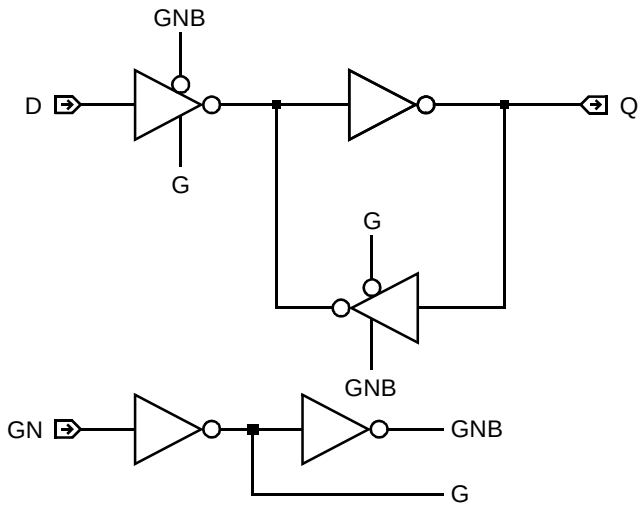
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			DL001	DL002
Min GN Width	Low	t_w	1.969	1.786
Min D Setup		t_{su}	1.375	1.274
Min D Hold		t_h	0.430	0.428

Logic Schematic



Core Logic

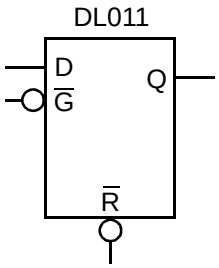
DL011

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DL011 is a transparent, unbuffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q
H	L	L	L
H	H	L	H
H	X	H	NC
L	X	X	L

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
RN	1.0

Equivalent Gates 3.2

HDL Syntax

Verilog ..... DL011 *inst_name* (Q, D, GN, RN);

VHDL..... *inst_name*: DL011 port map (Q, D, GN, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.270	nA
EQL_{pd}	5.5	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
D	Q	t_{PLH} t_{PHL}	1.278 1.343	1.909 1.649	2.828 2.048	3.432 2.295	4.327 2.647
GN	Q	t_{PLH} t_{PHL}	1.619 1.860	2.272 2.169	3.188 2.568	3.777 2.814	4.639 3.163
RN	Q	t_{PLH} t_{PHL}	1.085 0.779	1.701 1.060	2.634 1.442	3.247 1.682	4.149 2.027

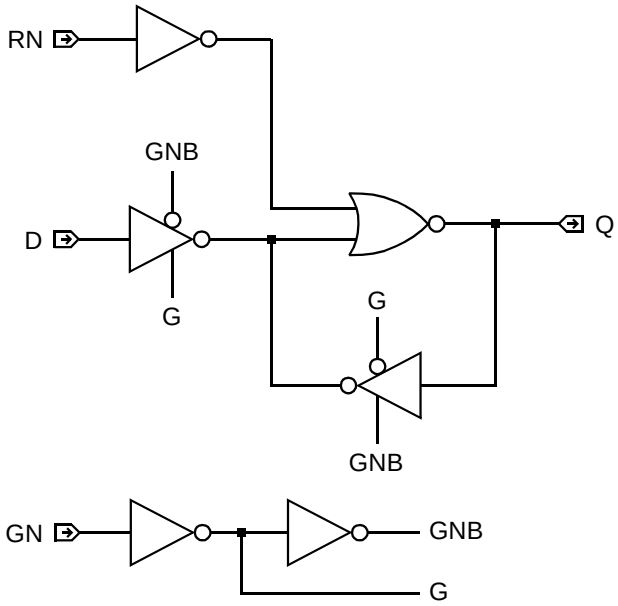
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	1.854
Min RN Width	Low	t_w	2.186
Min D Setup		t_{su}	1.304
Min D Hold		t_h	0.427
Min RN Setup		t_{su}	1.086
Min RN Hold		t_h	0.535

Logic Schematic



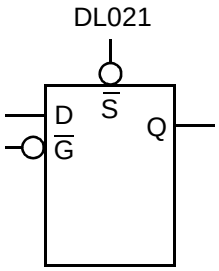
DL021

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DL021 is a transparent, unbuffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q
L	X	X	H
H	H	X	NC
H	L	L	L
H	L	H	H

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
SN	1.0

Equivalent Gates 2.8

HDL Syntax

Verilog ..... DL021 *inst_name* (Q, D, GN, SN);

VHDL..... *inst_name*: DL021 port map (Q, D, GN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.006	nA
EQL_{pd}	3.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
D	Q	t_{PLH} t_{PHL}	1.113 1.374	1.537 1.723	2.138 2.237	2.526 2.576	3.096 3.082
GN	Q	t_{PLH} t_{PHL}	1.436 1.884	1.855 2.253	2.449 2.778	2.834 3.119	3.401 3.620
SN	Q	t_{PLH} t_{PHL}	0.606 0.575	0.983 0.932	1.527 1.386	1.885 1.666	2.414 2.070

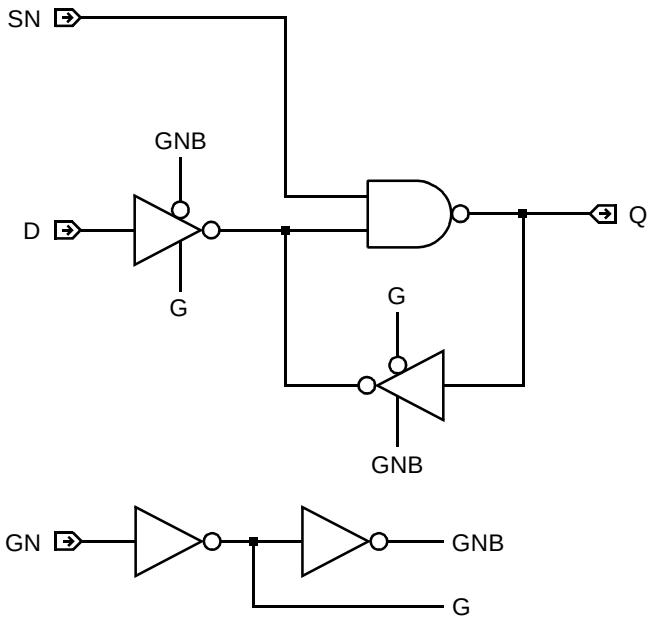
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	1.884
Min SN Width	Low	t_w	1.975
Min D Setup		t_{su}	1.357
Min D Hold		t_h	0.401
Min SN Setup		t_{su}	0.606
Min SN Hold		t_h	1.487

Logic Schematic



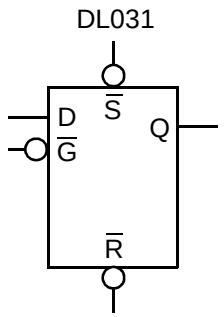
DL031

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DL031 is a transparent, unbuffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	X	H	NC
H	H	L	L	L
H	H	H	L	H

NC = No Change IL = Illegal

Pin Loading

	Equivalent Load
D	1.1
GN	1.1
SN	1.0
RN	1.0

Equivalent Gates 3.5

HDL Syntax

Verilog ..... DL031 *inst_name* (Q, D, GN, RN, SN);

VHDL..... *inst_name*: DL031 port map (Q, D, GN, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.261	nA
EQL_{pd}	4.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
D	Q	t_{PLH} t_{PHL}	1.407 1.711	1.838 2.130	2.451 2.708	2.849 3.064	3.435 3.556
GN	Q	t_{PLH} t_{PHL}	1.715 2.372	2.096 2.772	2.701 3.315	3.116 3.657	3.751 4.152
SN	Q	t_{PLH} t_{PHL}	0.683 0.526	1.074 0.937	1.580 1.485	1.905 1.823	2.394 2.305
RN	Q	t_{PLH} t_{PHL}	1.476 1.347	1.921 1.714	2.538 2.234	2.932 2.571	3.507 3.066

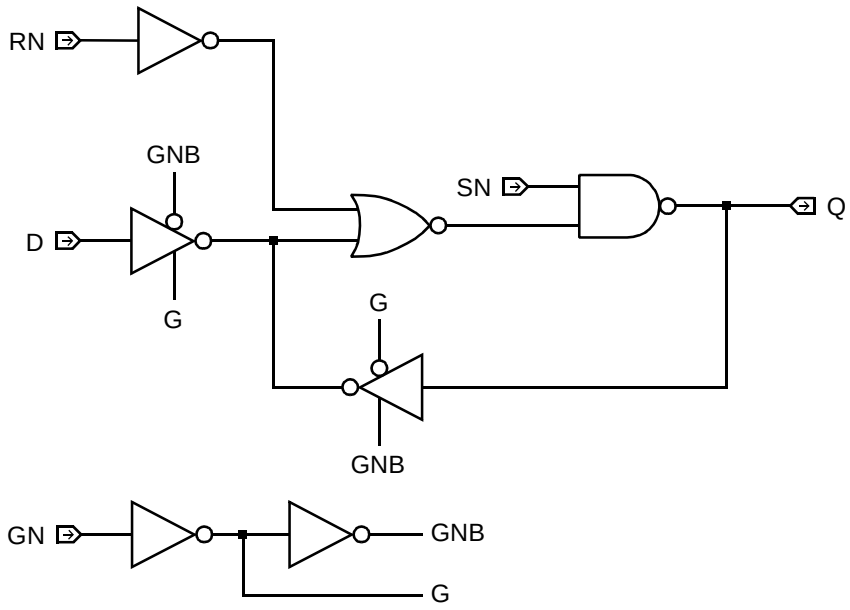
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	2.339
Min RN Width	Low	t_w	0.677
Min SN Width	Low	t_w	1.521
Min D Setup		t_{su}	1.738
Min D Hold		t_h	0.417
Min SN Setup		t_{su}	0.597
Min SN Hold		t_h	1.245
Min RN Setup		t_{su}	1.476
Min RN Hold		t_h	0.533

Logic Schematic



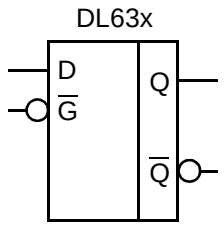
DL63x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

DL63x is a family of transparent, buffered D latches with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

D	GN	Q	QN
L	L	L	H
H	L	H	L
X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DL63x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL63x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL631	DL632	DL634	DL636
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL631	4.0	1.506	8.2
DL632	4.0	1.854	10.8
DL634	4.5	2.710	15.6
DL636	5.2	3.624	22.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DL631	From: D To: Q	t_{PLH} t_{PHL}	1.804 1.958	2.441 2.390	3.268 2.944	4.282 3.620	5.140 4.189
	From: D To: QN	t_{PLH} t_{PHL}	1.731 1.568	2.381 2.063	3.216 2.623	4.234 3.278	5.091 3.816
	From: GN To: Q	t_{PLH} t_{PHL}	2.122 2.501	2.760 2.954	3.587 3.510	4.601 4.172	5.457 4.720
	From: GN To: QN	t_{PLH} t_{PHL}	2.234 1.821	2.966 2.356	3.806 2.941	4.766 3.593	5.541 4.111
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DL632	From: D To: Q	t_{PLH} t_{PHL}	1.941 2.065	2.616 2.474	3.367 2.910	4.042 3.293	4.792 3.714
	From: D To: QN	t_{PLH} t_{PHL}	1.679 1.458	2.418 2.001	3.186 2.473	3.857 2.853	4.589 3.246
	From: GN To: Q	t_{PLH} t_{PHL}	2.258 2.572	2.959 3.047	3.709 3.477	4.373 3.830	5.102 4.201
	From: GN To: QN	t_{PLH} t_{PHL}	2.233 1.770	2.890 2.301	3.657 2.772	4.363 3.156	5.158 3.557
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DL634	From: D To: Q	t_{PLH} t_{PHL}	1.659 2.098	2.500 2.585	3.291 2.976	3.948 3.308	4.574 3.633
	From: D To: QN	t_{PLH} t_{PHL}	1.577 1.252	2.244 1.766	2.903 2.147	3.544 2.456	4.217 2.751
	From: GN To: Q	t_{PLH} t_{PHL}	2.240 2.632	2.882 3.086	3.541 3.452	4.201 3.763	4.939 4.068
	From: GN To: QN	t_{PLH} t_{PHL}	2.047 1.549	2.700 2.086	3.407 2.463	4.051 2.760	4.694 3.035

	Number of Equivalent Loads		1	28	56	84	112 (max)
DL636	From: D To: Q	t_{PLH} t_{PHL}	1.939 2.040	2.582 2.475	3.133 2.821	3.791 3.157	4.550 3.499
	From: D To: QN	t_{PLH} t_{PHL}	1.611 1.278	2.291 1.970	3.078 2.315	3.783 2.655	4.418 2.982
	From: GN To: Q	t_{PLH} t_{PHL}	2.371 2.579	2.953 2.992	3.560 3.356	4.172 3.702	4.795 4.038
	From: GN To: QN	t_{PLH} t_{PHL}	2.174 1.624	2.924 2.294	3.546 2.605	4.211 2.961	4.926 3.367

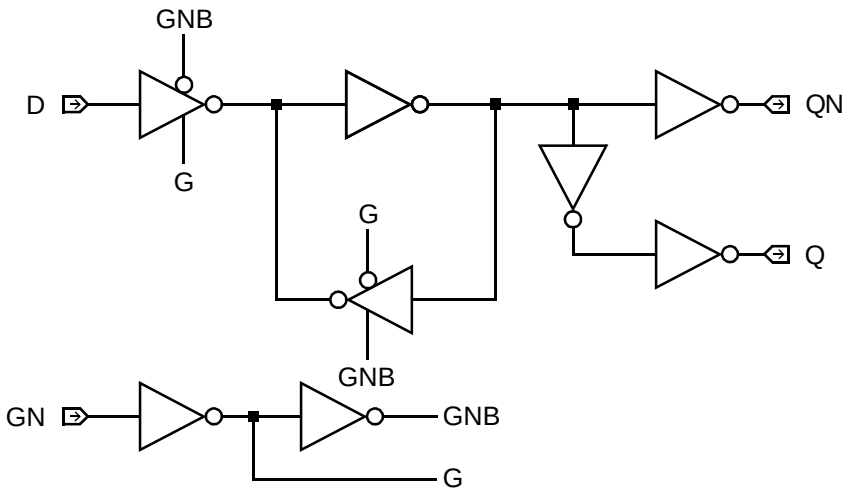
Delay will vary with input conditions. See page 2-Reference for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DL631	DL632	DL634	DL636
Min GN Width	Low	t_w	1.881	1.948	1.917	2.003
Min D Setup		t_{su}	1.332	1.394	1.370	1.468
Min D Hold		t_h	0.429	0.428	0.430	0.424

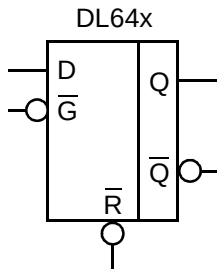
Logic Schematic



Description

DL64x is a family of transparent, buffered D latches with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

HDL Syntax

Verilog ..... DL64x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL64x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL641	DL642	DL644	DL646
D	1.0	1.0	1.0	1.0
GN	1.1	1.1	1.0	1.0
RN	1.0	1.1	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL641	4.0	1.486	8.5
DL642	4.0	1.809	10.9
DL644	5.8	3.441	20.6
DL646	6.2	4.161	26.1

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DL641	From: D To: Q	t_{PLH} t_{PHL}	1.404 1.829	2.204 2.521	3.085 3.179	4.068 3.857	4.851 4.369
	From: D To: QN	t_{PLH} t_{PHL}	2.317 1.870	3.026 2.443	3.855 3.015	4.814 3.620	5.593 4.085
	From: GN To: Q	t_{PLH} t_{PHL}	1.700 2.428	2.494 3.174	3.376 3.817	4.367 4.446	5.158 4.905
	From: GN To: QN	t_{PLH} t_{PHL}	2.901 2.203	3.471 2.676	4.283 3.255	5.334 3.940	6.254 4.506
	From: RN To: Q	t_{PLH} t_{PHL}	1.471 1.286	2.276 1.902	3.159 2.514	4.144 3.158	4.926 3.653
	From: RN To: QN	t_{PLH} t_{PHL}	1.734 1.957	2.379 2.483	3.187 3.064	4.187 3.716	5.041 4.235
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DL642	From: D To: Q	t_{PLH} t_{PHL}	1.395 1.761	2.240 2.517	3.051 3.067	3.736 3.480	4.465 3.888
	From: D To: QN	t_{PLH} t_{PHL}	2.581 2.027	3.260 2.523	3.994 2.978	4.647 3.356	5.368 3.752
	From: GN To: Q	t_{PLH} t_{PHL}	1.706 2.330	2.553 2.994	3.363 3.570	4.045 4.037	4.771 4.520
	From: GN To: QN	t_{PLH} t_{PHL}	3.167 2.341	3.872 2.770	4.611 3.231	5.260 3.640	5.969 4.090
	From: RN To: Q	t_{PLH} t_{PHL}	1.471 1.163	2.328 1.795	3.140 2.292	3.822 2.677	4.545 3.065
	From: RN To: QN	t_{PLH} t_{PHL}	1.894 2.092	2.538 2.556	3.282 3.018	3.964 3.414	4.730 3.841

	Number of Equivalent Loads		1	19	38	56	75 (max)
DL644	From: D To: Q	t_{PLH} t_{PHL}	1.959 1.958	2.699 2.361	3.422 2.738	4.085 3.077	4.770 3.423
	From: D To: QN	t_{PLH} t_{PHL}	2.300 2.341	2.946 2.751	3.622 3.087	4.260 3.392	4.932 3.721
	From: GN To: Q	t_{PLH} t_{PHL}	2.379 2.528	3.036 2.904	3.722 3.281	4.371 3.652	5.058 4.078
	From: GN To: QN	t_{PLH} t_{PHL}	2.882 2.646	3.377 3.147	4.093 3.504	4.818 3.780	5.575 4.028
	From: RN To: Q	t_{PLH} t_{PHL}	1.867 1.402	2.498 1.909	3.165 2.251	3.818 2.561	4.524 2.879
	From: RN To: QN	t_{PLH} t_{PHL}	1.758 2.146	2.433 2.481	3.088 2.871	3.714 3.236	4.420 3.607
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
DL646	From: D To: Q	t_{PLH} t_{PHL}	2.075 1.963	2.502 2.411	2.973 2.670	3.427 2.851	3.911 3.013
	From: D To: QN	t_{PLH} t_{PHL}	2.568 2.528	2.967 2.853	3.378 3.095	3.767 3.299	4.177 3.498
	From: GN To: Q	t_{PLH} t_{PHL}	2.457 2.518	2.800 2.835	3.289 3.096	3.773 3.320	4.256 3.541
	From: GN To: QN	t_{PLH} t_{PHL}	3.121 2.810	3.464 3.129	3.869 3.364	4.272 3.576	4.710 3.808
	From: RN To: Q	t_{PLH} t_{PHL}	1.928 1.458	2.387 1.849	2.866 2.093	3.313 2.282	3.782 2.457
	From: RN To: QN	t_{PLH} t_{PHL}	1.971 2.326	2.321 2.605	2.777 2.819	3.242 2.999	3.755 3.174

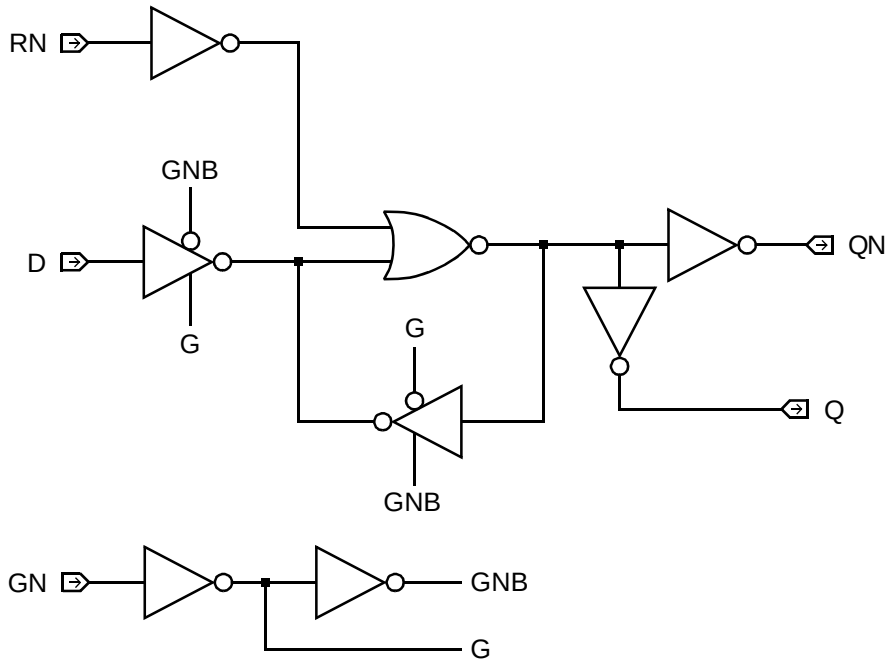
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL641	DL642	DL644	DL646
Min GN Width	Low	t_w	1.886	2.218	1.906	1.905
Min RN Width	Low	t_w	1.331	1.526	2.252	2.252
Min D Setup		t_{su}	1.886	2.218	1.346	1.347
Min D Hold		t_h	0.415	0.416	0.432	0.432
Min RN Setup		t_{su}	0.940	1.037	1.072	1.074
Min RN Hold		t_h	0.527	0.528	1.300	1.300

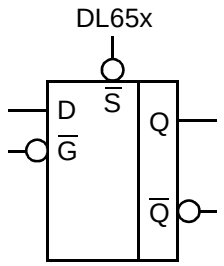
Logic Schematic



Description

DL65x is a family of transparent, buffered D latches with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

HDL Syntax

Verilog ..... DL65x *inst_name* (Q, QN, D, GN, SN);

VHDL..... *inst_name*: DL65x port map (Q, QN, D, GN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL651	DL652	DL654	DL656
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
SN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL651	4.5	1.567	8.6
DL652	4.5	1.904	11.0
DL654	5.2	3.128	19.3
DL656	6.0	3.861	24.7

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DL651	From: D To: Q	t_{PLH} t_{PHL}	1.942 2.119	2.610 2.536	3.443 3.089	4.438 3.776	5.265 4.360
	From: D To: QN	t_{PLH} t_{PHL}	1.849 1.660	2.585 2.217	3.436 2.798	4.414 3.451	5.207 3.993
	From: GN To: Q	t_{PLH} t_{PHL}	2.240 2.629	2.947 3.166	3.780 3.721	4.748 4.319	5.538 4.785
	From: GN To: QN	t_{PLH} t_{PHL}	2.374 1.976	3.089 2.519	3.939 3.118	4.932 3.789	5.744 4.323
	From: SN To: Q	t_{PLH} t_{PHL}	1.461 1.325	2.115 1.769	2.943 2.328	3.944 3.002	4.783 3.564
	From: SN To: QN	t_{PLH} t_{PHL}	1.060 1.169	1.787 1.758	2.641 2.352	3.631 2.984	4.438 3.470
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DL652	From: D To: Q	t_{PLH} t_{PHL}	2.113 2.206	2.733 2.668	3.479 3.100	4.175 3.459	4.966 3.838
	From: D To: QN	t_{PLH} t_{PHL}	1.853 1.583	2.537 2.133	3.313 2.618	4.018 3.013	4.805 3.424
	From: GN To: Q	t_{PLH} t_{PHL}	2.411 2.743	3.112 3.264	3.860 3.681	4.522 4.007	5.250 4.336
	From: GN To: QN	t_{PLH} t_{PHL}	2.381 1.900	3.050 2.437	3.825 2.923	4.535 3.323	5.334 3.742
	From: SN To: Q	t_{PLH} t_{PHL}	1.595 1.449	2.324 1.881	3.078 2.316	3.736 2.692	4.451 3.097
	From: SN To: QN	t_{PLH} t_{PHL}	1.007 1.124	1.802 1.708	2.595 2.143	3.276 2.503	4.009 2.918

	Number of Equivalent Loads		1	19	38	56	75 (max)
DL654	From: D To: Q	t_{PLH} t_{PHL}	1.771 2.053	2.385 2.582	3.103 2.961	3.792 3.280	4.512 3.592
	From: D To: QN	t_{PLH} t_{PHL}	2.435 2.099	3.125 2.549	3.813 2.934	4.450 3.277	5.111 3.630
	From: GN To: Q	t_{PLH} t_{PHL}	2.173 2.594	2.956 3.099	3.627 3.449	4.253 3.739	4.916 4.024
	From: GN To: QN	t_{PLH} t_{PHL}	3.037 2.427	3.744 2.824	4.265 3.109	4.873 3.401	5.679 3.760
	From: SN To: Q	t_{PLH} t_{PHL}	1.223 1.264	1.938 1.767	2.651 2.166	3.319 2.509	4.028 2.857
	From: SN To: QN	t_{PLH} t_{PHL}	1.653 1.607	2.304 2.016	2.975 2.366	3.626 2.695	4.328 3.053
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
DL656	From: D To: Q	t_{PLH} t_{PHL}	1.818 2.132	2.499 2.624	3.166 2.999	3.819 3.331	4.464 3.636
	From: D To: QN	t_{PLH} t_{PHL}	2.614 2.201	3.158 2.691	3.837 3.048	4.567 3.358	5.330 3.641
	From: GN To: Q	t_{PLH} t_{PHL}	2.140 2.627	2.756 3.077	3.409 3.460	4.069 3.813	4.733 4.148
	From: GN To: QN	t_{PLH} t_{PHL}	3.225 2.533	3.850 3.015	4.461 3.385	5.058 3.714	5.646 4.017
	From: SN To: Q	t_{PLH} t_{PHL}	1.367 1.305	2.067 1.832	2.735 2.190	3.408 2.505	4.089 2.792
	From: SN To: QN	t_{PLH} t_{PHL}	1.820 1.723	2.388 2.157	3.088 2.520	3.810 2.855	4.531 3.183

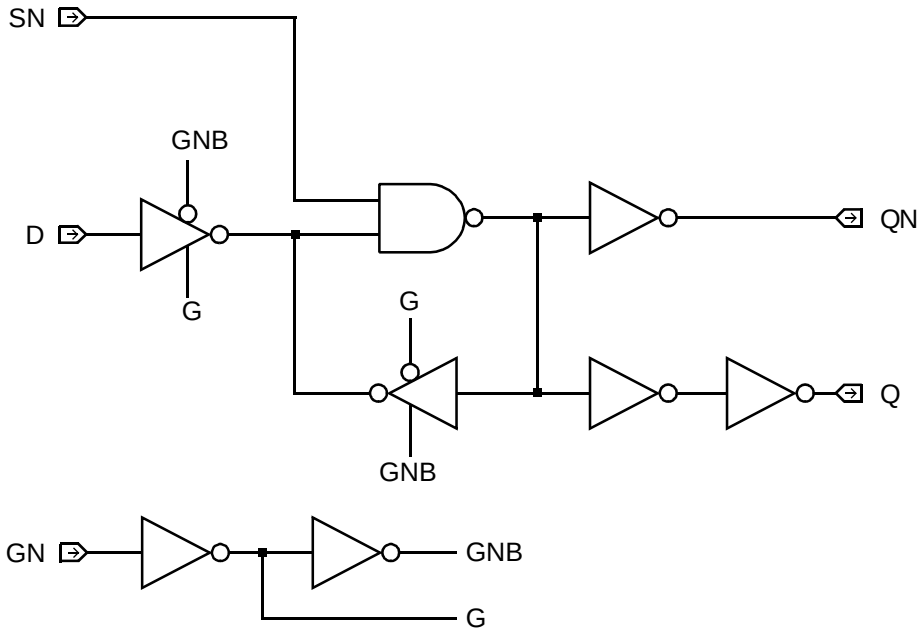
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL651	DL652	DL654	DL656
Min GN Width	Low	t_w	1.969	2.037	1.943	1.944
Min SN Width	Low	t_w	1.923	2.071	1.894	1.890
Min D Setup		t_{su}	1.422	1.490	1.393	1.393
Min D Hold		t_h	0.401	0.401	0.401	0.401
Min SN Setup		t_{su}	0.619	0.690	0.584	0.584
Min SN Hold		t_h	1.489	1.485	1.497	1.497

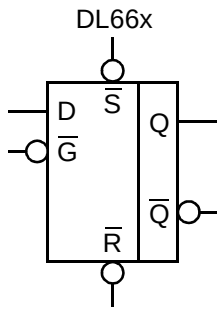
Logic Schematic



Description

DL66x is a family of transparent, buffered D latches with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DL66x *inst_name* (Q, QN, D, GN, RN, SN);

VHDL..... *inst_name*: DL66x port map (Q, QN, D, GN, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL661	DL662	DL664	DL666
D	1.2	1.2	1.0	1.0
GN	1.1	1.1	1.0	1.0
SN	1.0	1.0	2.0	2.0
RN	1.1	1.1	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL661	4.8	1.807	10.3
DL662	4.8	2.131	12.7
DL664	7.2	3.640	25.1
DL666	8.0	4.321	30.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
DL661	From: D To: Q	t_{PLH} t_{PHL}	2.418 2.695	3.107 3.217	3.939 3.776	4.917 4.390	5.722 4.875
	From: D To: QN	t_{PLH} t_{PHL}	2.362 2.076	3.039 2.699	3.893 3.310	4.923 3.951	5.786 4.441
	From: GN To: Q	t_{PLH} t_{PHL}	2.745 3.274	3.320 3.793	4.134 4.352	5.182 4.970	6.096 5.457
	From: GN To: QN	t_{PLH} t_{PHL}	2.965 2.381	3.699 2.945	4.556 3.563	5.547 4.252	6.352 4.799
	From: SN To: Q	t_{PLH} t_{PHL}	1.674 1.463	2.305 1.902	3.094 2.461	4.082 3.139	4.936 3.708
	From: SN To: QN	t_{PLH} t_{PHL}	1.102 1.303	1.855 1.903	2.727 2.484	3.717 3.116	4.513 3.632
	From: R To: Q	t_{PLH} t_{PHL}	2.518 2.237	3.115 2.728	3.934 3.289	4.970 3.929	5.864 4.444
	From: RN To: QN	t_{PLH} t_{PHL}	1.897 2.145	2.610 2.710	3.466 3.332	4.470 4.026	5.294 4.578
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
DL662	From: D To: Q	t_{PLH} t_{PHL}	2.575 2.804	3.248 3.180	3.992 3.618	4.662 4.021	5.405 4.475
	From: D To: QN	t_{PLH} t_{PHL}	2.329 1.980	3.126 2.600	3.912 3.093	4.583 3.477	5.303 3.865
	From: GN To: Q	t_{PLH} t_{PHL}	2.916 3.386	3.473 3.757	4.207 4.196	4.921 4.602	5.755 5.061
	From: GN To: QN	t_{PLH} t_{PHL}	2.940 2.280	3.680 2.927	4.469 3.408	5.166 3.773	5.931 4.134
	From: SN To: Q	t_{PLH} t_{PHL}	1.792 1.536	2.427 1.996	3.163 2.448	3.838 2.833	4.598 3.247
	From: SN To: QN	t_{PLH} t_{PHL}	1.113 1.167	1.874 1.793	2.669 2.270	3.367 2.654	4.129 3.069
	From: RN To: Q	t_{PLH} t_{PHL}	2.633 2.303	3.389 2.786	4.128 3.220	4.757 3.576	5.431 3.947
	From: RN To: QN	t_{PLH} t_{PHL}	1.852 2.047	2.679 2.653	3.461 3.153	4.116 3.548	4.812 3.952

	Number of Equivalent Loads		1	19	38	56	75 (max)
DL664	From: D To: Q	t_{PLH} t_{PHL}	1.968 1.986	2.694 2.500	3.382 2.885	4.086 3.202	4.864 3.508
	From: D To: QN	t_{PLH} t_{PHL}	2.366 2.360	3.037 2.710	3.732 3.079	4.363 3.409	5.006 3.724
	From: GN To: Q	t_{PLH} t_{PHL}	2.378 2.482	3.066 3.014	3.752 3.385	4.387 3.687	5.046 3.976
	From: GN To: QN	t_{PLH} t_{PHL}	2.920 2.682	3.483 3.143	4.194 3.458	4.911 3.732	5.686 4.034
	From: SN To: Q	t_{PLH} t_{PHL}	0.922 0.969	1.619 1.480	2.324 1.891	2.979 2.225	3.663 2.540
	From: SN To: QN	t_{PLH} t_{PHL}	1.447 1.246	2.045 1.633	2.725 2.007	3.393 2.349	4.103 2.702
	From: RN To: Q	t_{PLH} t_{PHL}	1.738 1.396	2.381 1.862	3.055 2.253	3.726 2.591	4.447 2.926
	From: RN To: QN	t_{PLH} t_{PHL}	1.816 2.076	2.461 2.483	3.090 2.844	3.711 3.169	4.458 3.505

	Number of Equivalent Loads		1	28	56	84	112 (max)
DL666	From: D To: Q	t_{PLH} t_{PHL}	2.049 2.072	2.761 2.607	3.461 2.974	4.143 3.293	4.817 3.586
	From: D To: QN	t_{PLH} t_{PHL}	2.531 2.474	3.156 2.958	3.845 3.333	4.522 3.659	5.173 3.961
	From: GN To: Q	t_{PLH} t_{PHL}	2.355 2.546	2.996 3.090	3.666 3.460	4.346 3.773	5.037 4.055
	From: GN To: QN	t_{PLH} t_{PHL}	3.179 2.854	3.704 3.144	4.336 3.475	5.057 3.850	5.872 4.260
	From: SN To: Q	t_{PLH} t_{PHL}	1.041 1.087	1.719 1.561	2.375 1.915	3.055 2.248	3.756 2.571
	From: SN To: QN	t_{PLH} t_{PHL}	1.574 1.351	2.166 1.812	2.833 2.165	3.528 2.503	4.248 2.835
	From: RN To: Q	t_{PLH} t_{PHL}	1.781 1.506	2.511 1.972	3.189 2.368	3.836 2.716	4.464 3.025
	From: RN To: QN	t_{PLH} t_{PHL}	1.926 2.152	2.595 2.613	3.283 3.005	3.967 3.350	4.648 3.670

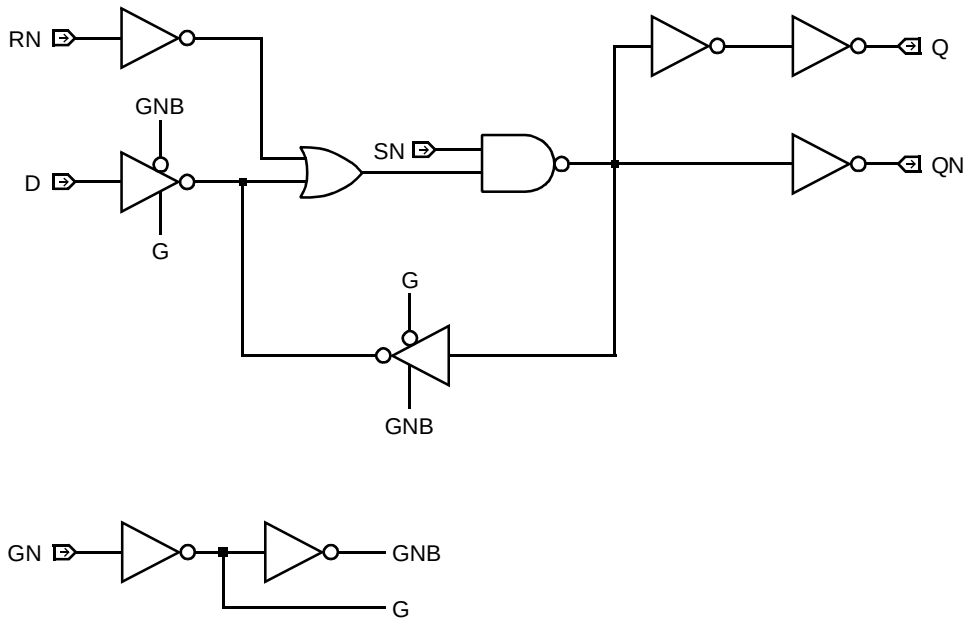
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL661	DL662	DL664	DL666
Min GN Width	Low	t_w	2.510	2.569	1.963	1.962
Min RN Width	Low	t_w	1.491	1.551	0.849	0.847
Min SN Width	Low	t_w	1.644	1.766	1.912	1.909
Min D Setup		t_{su}	1.891	1.949	1.418	1.415
Min D Hold		t_h	0.416	0.416	0.403	0.403
Min SN Setup		t_{su}	0.675	0.741	0.421	0.419
Min SN Hold		t_h	1.263	1.257	1.708	1.708
Min RN Setup		t_{su}	1.588	1.667	1.084	1.080
Min RN Hold		t_h	0.530	0.530	1.717	1.718

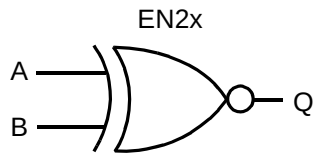
Logic Schematic



Description

EN2x is a family of 2-input gates which perform the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... EN2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EN2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EN21	EN22	EN23	EN24	EN26
A	2.0	3.8	3.9	3.7	3.8
B	2.0	3.8	3.7	3.7	3.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EN21	1.8	0.686	3.5
EN22	2.2	1.334	6.2
EN23	3.0	1.830	10.0
EN24	3.0	2.161	11.6
EN26	3.2	2.527	14.7

a. See page 2-13 for power equation.

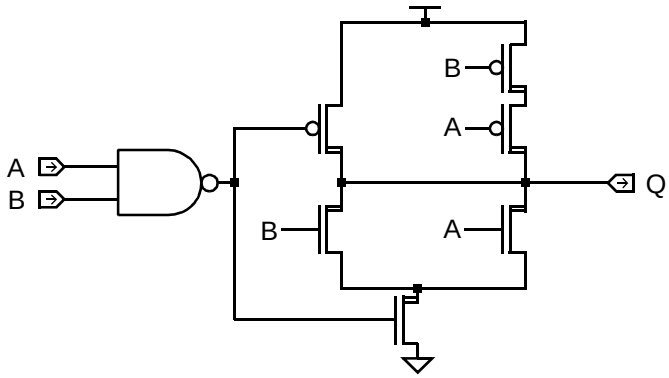
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

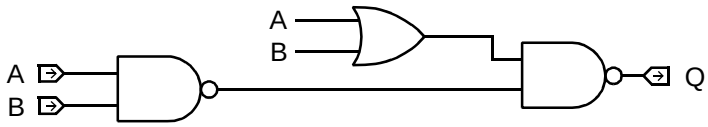
EN21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.073 0.582	1.466 0.946	2.033 1.377	2.411 1.668	2.986 2.163
EN22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.728 0.361	1.008 0.680	1.373 1.000	1.823 1.363	2.204 1.655
EN23	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.741 1.255	1.440 1.783	2.192 2.244	2.876 2.617	3.644 3.004
EN24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.673 1.219	1.421 1.799	2.129 2.207	2.784 2.536	3.468 2.849
EN26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.756 1.430	1.485 2.037	2.164 2.422	2.821 2.761	3.489 3.083

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



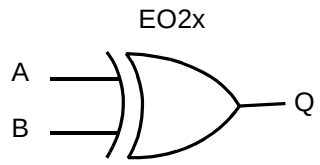
LOGICAL



Description

EO2x is a family of 2-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... EO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EO21	EO22	EO23	EO24	EO26
A	2.1	3.7	3.8	3.8	3.8
B	2.1	3.7	3.8	3.8	3.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO21	2.0	0.817	3.7
EO22	2.0	1.438	6.7
EO23	3.0	1.707	10.2
EO24	3.5	2.053	12.7
EO26	3.8	2.371	15.1

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

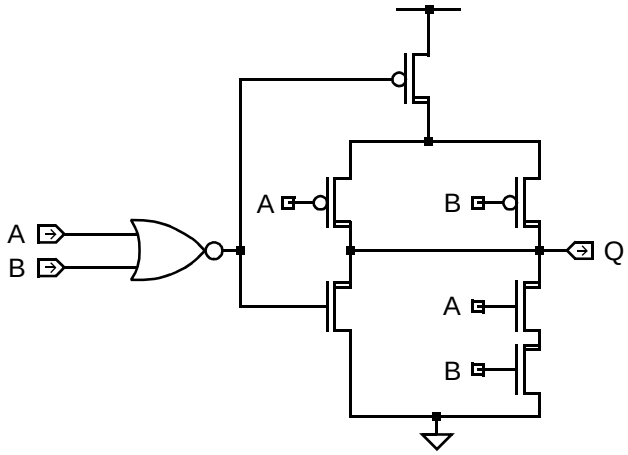
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

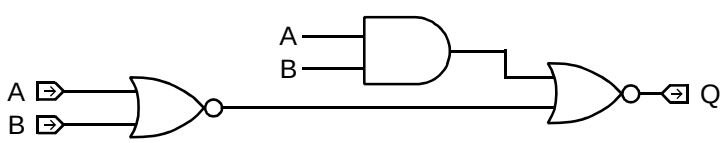
EO21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.254 0.596	1.884 1.021	2.853 1.589	3.510 1.951	4.508 2.486
EO22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.901 0.069	1.447 0.727	2.144 1.186	2.986 1.642	3.687 2.028
EO23	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.653 1.053	1.384 1.524	2.163 1.963	2.852 2.328	3.608 2.714
EO24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.732 1.104	1.447 1.554	2.108 1.898	2.734 2.211	3.441 2.540
EO26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.809 1.067	1.536 1.631	2.172 1.990	2.813 2.333	3.480 2.673

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



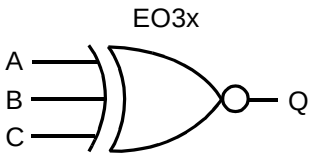
LOGICAL



Description

EO3x is a family of 3-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

HDL Syntax

Verilog ..... EO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: EO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	EO31	EO32	EO33	EO34	EO36
A	2.0	2.1	2.1	2.1	2.1
B	2.0	2.1	2.1	2.1	2.1
C	2.0	3.0	3.0	3.0	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO31	3.5	1.495	9.0
EO32	4.0	1.882	12.9
EO33	4.5	1.824	15.6
EO34	4.8	2.164	18.0
EO36	5.0	2.510	20.5

a. See page 2-13 for power equation.

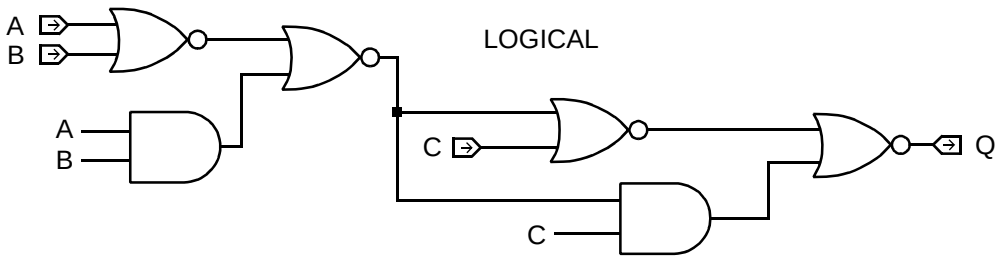
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

EO31	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	2.531 2.002	3.180 2.538	4.076 3.249	4.647 3.692	5.477 4.328
EO32	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	2.831 2.053	3.377 2.535	4.088 3.025	4.960 3.532	5.698 3.916
EO33	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	2.242 3.003	2.992 3.488	3.756 3.923	4.418 4.279	5.135 4.651
EO34	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	2.338 3.123	3.095 3.509	3.817 3.836	4.469 4.132	5.157 4.436
EO36	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	2.406 3.063	3.207 3.679	3.832 4.016	4.437 4.284	5.046 4.526

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

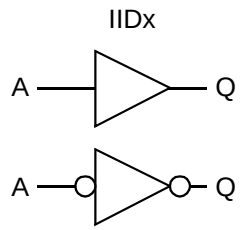
Logic Schematic



Description

IIDx is a family of non-inverting clock drivers with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... IIDx *inst_name* (Q, A);

VHDL..... *inst_name*: IIDx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads				
	IID1	IID2	IID3	IID4	IID6
A	1.0	1.0	1.8	1.8	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IID1	1.0	0.411	2.2
IID2	1.0	0.585	3.4
IID3	1.2	0.933	4.8
IID4	1.8	1.123	5.9
IID6	1.8	1.475	8.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

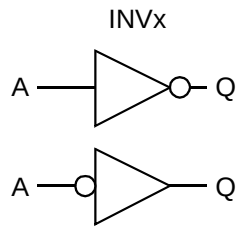
IID1	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.710 0.643	1.385 1.106	2.211 1.666	3.198 2.320	4.019 2.854
IID2	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.659 0.633	1.382 1.108	2.143 1.514	2.824 1.869	3.593 2.276
IID3	**Number of Equivalent Loads**		**1**	**14**	**28**	**43**	**57 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.449 0.435	1.119 0.876	1.803 1.227	2.535 1.590	3.229 1.953
IID4	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.518 0.501	1.170 0.925	1.853 1.246	2.508 1.579	3.193 1.954
IID6	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.526 0.533	1.217 1.018	1.884 1.365	2.560 1.678	3.255 1.974

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

INVx is a family of inverters which perform the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

HDL Syntax

Verilog ..... INVx *inst_name* (Q, A);

VHDL..... *inst_name*: INVx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads					
	INV1	INV2	INV3	INV4	INV5	INV6
A	1.0	1.8	2.9	3.9	4.7	5.4

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
INV1	0.8	0.223	0.6
INV2	1.0	0.408	1.0
INV3	1.0	0.585	1.3
INV4	1.2	0.760	1.6
INV5	1.2	0.932	2.0
INV6	1.5	1.113	2.2

a. See page 2-13 power equation

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

INV1	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.389 0.355	1.156 0.942	1.864 1.493	2.651 2.059	3.341 2.501
INV2	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.322 0.251	1.095 0.784	1.776 1.206	2.398 1.544	3.152 1.903
INV3	**Number of Equivalent Loads**		**1**	**14**	**28**	**43**	**57 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.156 0.212	0.857 0.673	1.446 0.991	2.031 1.300	2.561 1.581
INV4	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.133 0.183	0.839 0.596	1.567 0.992	2.208 1.381	2.859 1.682
INV5	**Number of Equivalent Loads**		**1**	**24**	**47**	**70**	**94 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.202 0.185	0.862 0.677	1.533 1.044	2.199 1.336	2.832 1.591
INV6	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.278 0.119	0.899 0.696	1.600 1.153	2.316 1.535	2.912 1.868

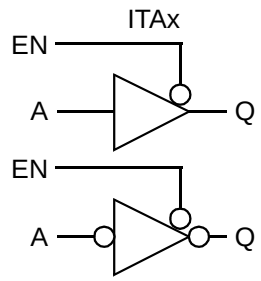
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ITAx is a family of non-inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

HDL Syntax

Verilog ..... ITAx *inst_name* (Q, A, EN);

VHDL..... *inst_name*: ITAx port map (Q, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITA1	ITA2	ITA4	ITA6
A	1.0	1.0	1.0	1.0
EN	1.5	1.9	2.8	3.8
Q	0.6	1.0	1.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITA1	2.0	0.631	3.7
ITA2	2.0	0.807	5.7
ITA4	2.0	1.144	9.5
ITA6	2.8	1.528	14.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITA1	Number of Equivalent Loads		1	18	35	52	70 (max)
	From: A To: Q	t_{PLH} t_{PHL}	1.124 0.867	6.545 4.438	11.935 7.984	17.349 11.537	23.110 15.307
	From: EN To: Q	t_{ZH} t_{ZL}	0.605 0.665	6.153 4.308	11.338 7.866	16.667 11.413	22.605 15.178
ITA2	Number of Equivalent Loads		1	33	66	99	132 (max)
	From: A To: Q	t_{PLH} t_{PHL}	0.959 0.692	5.694 3.233	10.574 5.815	15.454 8.381	20.333 10.938
	From: EN To: Q	t_{ZH} t_{ZL}	0.629 0.535	5.285 3.083	9.908 5.633	14.764 8.189	19.548 10.785
ITA4	Number of Equivalent Loads		1	64	128	191	255 (max)
	From: A To: Q	t_{PLH} t_{PHL}	0.983 0.929	5.669 3.467	10.402 5.949	15.049 8.394	19.763 10.898
	From: EN To: Q	t_{ZH} t_{ZL}	0.222 0.599	4.916 3.110	9.574 5.592	14.191 8.039	18.929 10.541
ITA6	Number of Equivalent Loads		1	94	189	284	378 (max)
	From: A To: Q	t_{PLH} t_{PHL}	1.116 1.137	5.746 3.710	10.419 6.210	15.070 8.687	19.659 11.138
	From: EN To: Q	t_{ZH} t_{ZL}	0.296 0.684	4.832 3.273	9.288 5.728	13.865 8.174	18.527 10.619

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

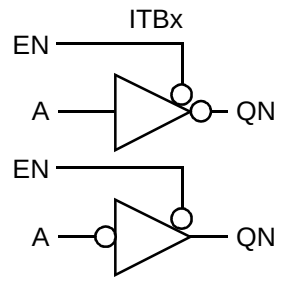
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ITA1	ITA2	ITA4	ITA6
EN	Q	t_{HZ} t_{LZ}	0.218 0.419	0.215 0.479	0.211 0.619	0.205 0.755

Description

ITBx is a family of inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITBx *inst_name* (QN, A, EN);

VHDL..... *inst_name*: ITBx port map (QN, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITB1	ITB2	ITB4	ITB6
A	1.0	1.9	3.7	5.6
EN	1.5	1.9	2.8	3.7
QN	0.6	0.9	1.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITB1	1.2	0.424	2.1
ITB2	1.2	0.591	3.2
ITB4	1.8	0.956	5.3
ITB6	2.2	1.333	8.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITB1	**Number of Equivalent Loads**		**1**	**18**	**35**	**52**	**70 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.876 0.632	6.276 4.222	11.608 7.747	17.038 11.300	22.719 15.097
	From: EN To: QN	t_{ZH} t_{ZL}	0.444 0.675	6.008 4.266	11.411 7.813	16.789 11.372	22.486 15.166
ITB2	**Number of Equivalent Loads**		**1**	**33**	**66**	**99**	**132 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.587 0.427	5.262 3.005	10.055 5.495	14.901 8.025	19.803 10.616
	From: EN To: QN	t_{ZH} t_{ZL}	0.419 0.524	5.082 3.039	9.895 5.623	14.702 8.209	19.490 10.797
ITB4	**Number of Equivalent Loads**		**1**	**64**	**128**	**191**	**255 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.345 0.392	5.137 2.921	9.915 5.241	14.578 7.646	19.288 10.257
	From: EN To: QN	t_{ZH} t_{ZL}	0.368 0.602	4.978 3.097	9.558 5.604	14.231 8.075	19.156 10.589
ITB6	**Number of Equivalent Loads**		**1**	**94**	**189**	**284**	**378 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.278 0.326	4.946 2.975	9.639 5.294	14.296 7.679	18.881 10.167
	From: EN To: QN	t_{ZH} t_{ZL}	0.292 0.658	4.826 3.252	9.438 5.699	14.088 8.154	18.724 10.628

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

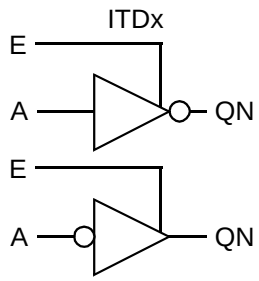
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Cell			
From	**To**		**ITB1**	**ITB2**	**ITB4**	**ITB6**
EN	QN	t_{HZ} t_{LZ}	0.217 0.413	0.215 0.490	0.210 0.616	0.205 0.744

Description

ITD1x is a family of inverting internal tristate buffers with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITDx *inst_name* (QN, A, E);

VHDL..... *inst_name*: ITDx port map (QN, A, E);

Pin Loading

Pin Name	Equivalent Loads			
	ITD1	ITD2	ITD4	ITD6
A	1.0	1.8	3.7	5.6
E	1.5	1.9	2.8	3.8
QN	0.6	0.9	1.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITD1	1.2	0.423	2.1
ITD2	1.5	0.600	3.1
ITD4	1.8	0.955	5.2
ITD6	2.2	1.329	7.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITD1	**Number of Equivalent Loads**		**1**	**18**	**35**	**52**	**70 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.753 0.637	6.258 4.187	11.590 7.670	16.932 11.198	22.683 14.957
	From: E To: QN	t_{ZH} t_{ZL}	0.800 0.519	6.193 4.303	11.592 7.732	17.001 11.183	22.737 14.937
ITD2	**Number of Equivalent Loads**		**1**	**33**	**66**	**99**	**132 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.577 0.422	5.244 2.850	10.078 5.348	14.936 8.043	19.817 10.860
	From: E To: QN	t_{ZH} t_{ZL}	0.584 0.506	5.316 3.125	10.157 5.497	15.017 7.934	19.907 10.504
ITD4	**Number of Equivalent Loads**		**1**	**64**	**128**	**191**	**255 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.381 0.321	5.161 2.876	9.844 5.183	14.454 7.557	19.177 10.136
	From: E To: QN	t_{ZH} t_{ZL}	0.589 0.341	5.258 3.006	9.995 5.330	14.659 7.717	19.410 10.292
ITD6	**Number of Equivalent Loads**		**1**	**94**	**189**	**284**	**378 (max)**
	From: A To: QN	t_{PLH} t_{PHL}	0.334 0.446	5.056 2.775	9.704 5.160	14.339 7.680	18.942 10.284
	From: E To: QN	t_{ZH} t_{ZL}	0.615 0.277	5.165 3.085	9.824 5.412	14.488 7.748	19.106 10.115

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

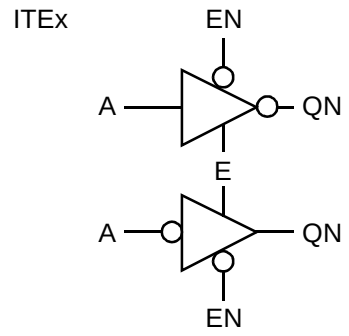
Delay (ns) From	To	Parameter	Cell ITD1	Cell ITD2	Cell ITD4	Cell ITD6
E	QN	t_{HZ} t_{LZ}	0.441 0.055	0.498 0.055	0.674 0.055	0.825 0.054

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ITEx is a family of two-phase enable inverting internal tristate buffers.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

IL = Illegal

HDL Syntax

Verilog ..... ITEx *inst_name* (QN, A, E, EN);

VHDL..... *inst_name*: ITEx port map (QN, A, E, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITE1	ITE2	ITE4	ITE6
A	1.0	1.8	3.7	5.6
E	0.5	1.0	1.9	2.8
EN	0.5	0.9	1.8	2.7
QN	0.6	1.0	2.0	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITE1	1.0	0.235	1.0
ITE2	1.0	0.410	1.8
ITE4	1.5	0.784	3.5
ITE6	2.0	1.142	4.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ITE1	Number of Equivalent Loads		1	18	35	52	70 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.871 0.658	6.229 4.273	11.606 7.725	17.030 11.249	22.755 15.094
	From: EN To: QN	t_{ZH}	0.807	6.156	11.513	16.920	22.699
	From: E To: QN	t_{ZL}	0.517	4.368	7.819	11.305	15.141
ITE2	Number of Equivalent Loads		1	33	66	99	132 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.445 0.347	5.224 3.033	10.113 5.530	14.982 8.041	19.842 10.634
	From: EN To: QN	t_{ZH}	0.255	5.286	10.046	14.820	19.701
	From: E To: QN	t_{ZL}	0.631	3.061	5.400	7.910	10.376
ITE4	Number of Equivalent Loads		1	64	128	191	255 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.418 0.354	5.138 2.852	9.843 5.239	14.449 7.653	19.123 10.181
	From: EN To: QN	t_{ZH}	0.466	5.116	9.733	14.308	18.993
	From: E To: QN	t_{ZL}	0.315	3.121	5.391	7.732	10.320
ITE6	Number of Equivalent Loads		1	94	189	284	378 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.343 0.208	5.013 2.855	9.663 5.251	14.294 7.650	18.874 10.074
	From: EN To: QN	t_{ZH}	0.380	5.211	9.612	14.108	18.775
	From: E To: QN	t_{ZL}	0.229	3.042	5.325	7.603	9.925

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

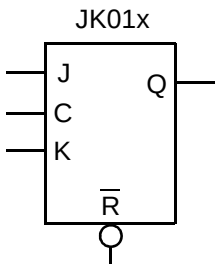
Delay (ns) From	To	Parameter	Cell			
			ITE1	ITE2	ITE4	ITE6
EN	QN	t_{HZ}	0.215	0.215	0.209	0.205
E	QN	t_{LZ}	0.056	0.054	0.054	0.054

JK01x

Description

JK01x is a family of static, master-slave JK flip-flops. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)
L	X	X	X	L
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK01x *inst_name* (Q, C, J, K, RN);

VHDL..... *inst_name*: JK01x port map (Q, C, J, K, RN);

Pin Loading

Pin Name	Equivalent Loads	
	JK011	JK012
J	1.1	1.1
K	1.1	1.1
C	1.0	1.0
RN	1.1	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK011	6.8	2.499	20.2
JK012	7.0	2.749	21.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	8	11 (max)
JK011	From: C To: Q	t_{PLH} t_{PHL}	2.842 2.551	3.504 2.893	4.426 3.368	5.017 3.670	5.880 4.112
	From: RN To: Q	t_{PHL}	1.060	1.358	1.738	1.971	2.310
	Number of Equivalent Loads		**1**	**5**	**10**	**16**	**21 (max)**
JK012	From: C To: Q	t_{PLH} t_{PHL}	2.476 2.234	3.053 2.592	3.771 2.958	4.629 3.350	5.343 3.655
	From: RN To: Q	t_{PHL}	0.947	1.199	1.468	1.754	1.976

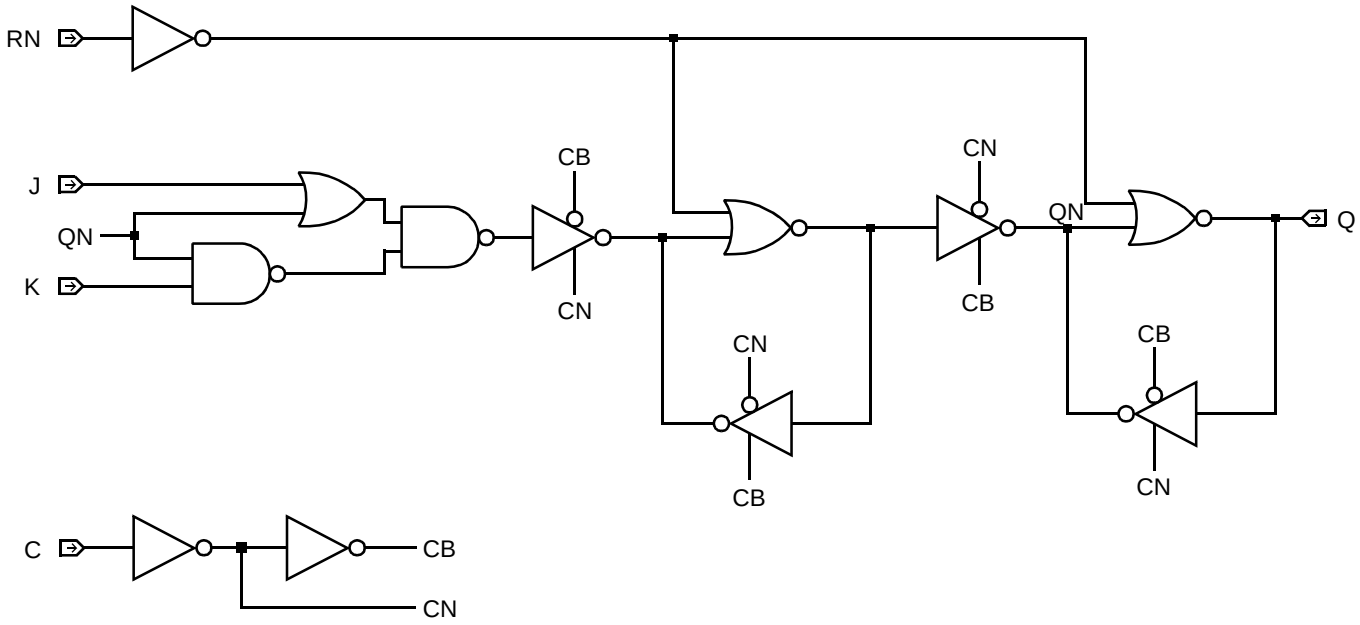
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK011	JK012
Min C Width	High	t_w	2.830	2.481
Min C Width	Low	t_w	2.416	2.390
Min RN Width	Low	t_w	2.546	2.673
Min J Setup		t_{su}	2.341	2.349
Min J Hold		t_h	0.569	0.553
Min K Setup		t_{su}	2.133	2.104
Min K Hold		t_h	0.569	0.553
Min RN Setup		t_{su}	1.135	1.217
Min RN Hold		t_h	1.592	1.561

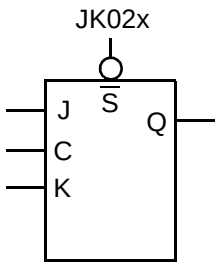
Logic Schematic



Description

JK02x is a family of static, master-slave JK flip-flops. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)
L	X	X	X	H
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK02x *inst_name* (Q, C, J, K, SN);

VHDL..... *inst_name*: JK02x port map (Q, C, J, K, SN);

Pin Loading

Pin Name	Equivalent Loads	
	JK021	JK022
J	1.0	1.0
K	1.0	1.0
C	1.0	1.0
SN	2.2	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK021	6.2	2.382	16.5
JK022	6.2	2.581	17.3

a. See page 2-13 for power equation.

AMI500MXSC 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	8	11 (max)
JK021	From: C To: Q	t_{PLH} t_{PHL}	2.496 2.468	2.950 2.928	3.552 3.499	3.927 3.842	4.466 4.323
	From: SN To: Q	t_{PLH}	0.758	1.170	1.689	2.075	2.627
	Number of Equivalent Loads		**1**	**5**	**10**	**16**	**21 (max)**
JK022	From: C To: Q	t_{PLH} t_{PHL}	2.298 2.142	2.702 2.570	3.181 3.003	3.738 3.463	4.193 3.818
	From: SN To: Q	t_{PLH}	0.476	0.864	1.236	1.690	2.094

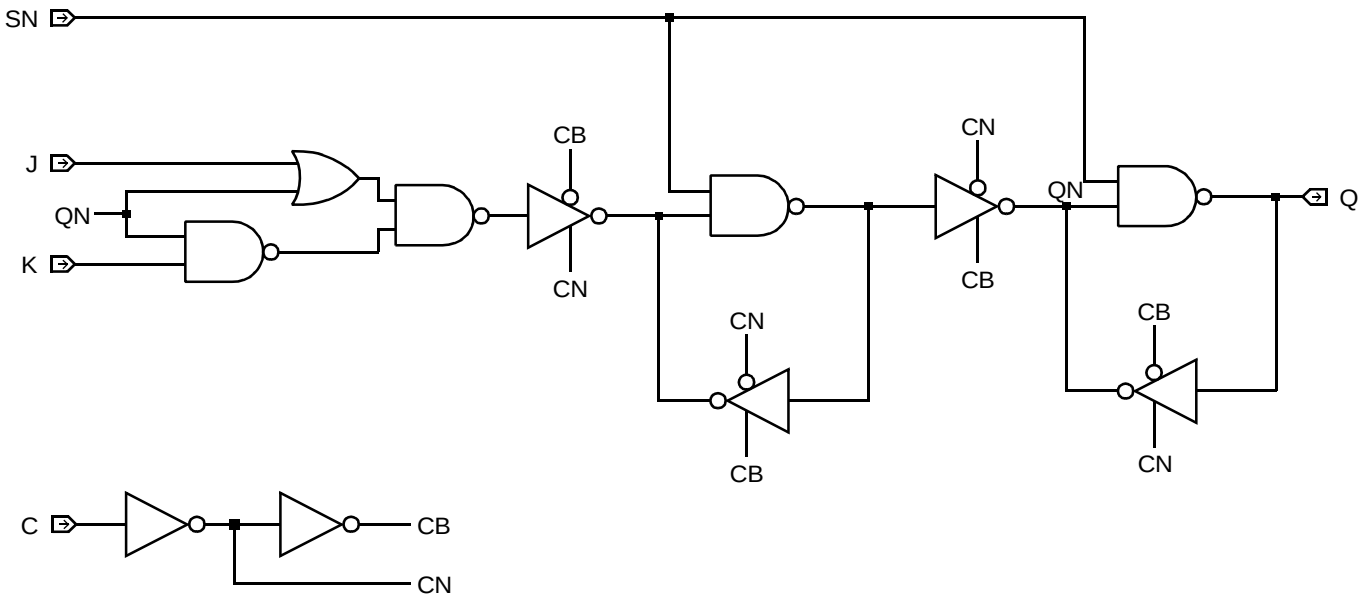
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK021	JK022
Min C Width	High	t_w	2.494	2.318
Min C Width	Low	t_w	2.249	2.299
Min SN Width	Low	t_w	1.758	2.411
Min J Setup		t_{su}	2.249	2.299
Min J Hold		t_h	0.515	0.521
Min K Setup		t_{su}	1.871	1.904
Min K Hold		t_h	0.515	0.521
Min SN Setup		t_{su}	0.526	0.543
Min SN Hold		t_h	1.860	1.909

Logic Schematic



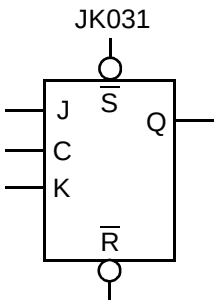
JK031

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

JK031 is a static, master-slave JK flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)
L	L	X	X	X	IL
L	H	X	X	X	L
H	L	X	X	X	H
H	H	L	L	↑	NC
H	H	L	H	↑	L
H	H	H	L	↑	H
H	H	H	H	↑	$\overline{Q(n)}$

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	1.0
SN	2.3
RN	2.3

Equivalent Gates 8.5

HDL Syntax

Verilog ..... JK031 *inst_name* (Q, C, J, K, RN, SN);

VHDL..... *inst_name*: JK031 port map (Q, C, J, K, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.734	nA
EQL_{pd}	21.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	3	6	8	11 (max)
C	Q	t_{PLH} t_{PHL}	2.651 2.598	3.064 3.016	3.669 3.596	4.067 3.968	4.659 4.510
RN	Q	t_{PHL}	3.034	3.400	3.980	4.378	4.987
SN	Q	t_{PLH}	0.797	1.190	1.694	2.014	2.496

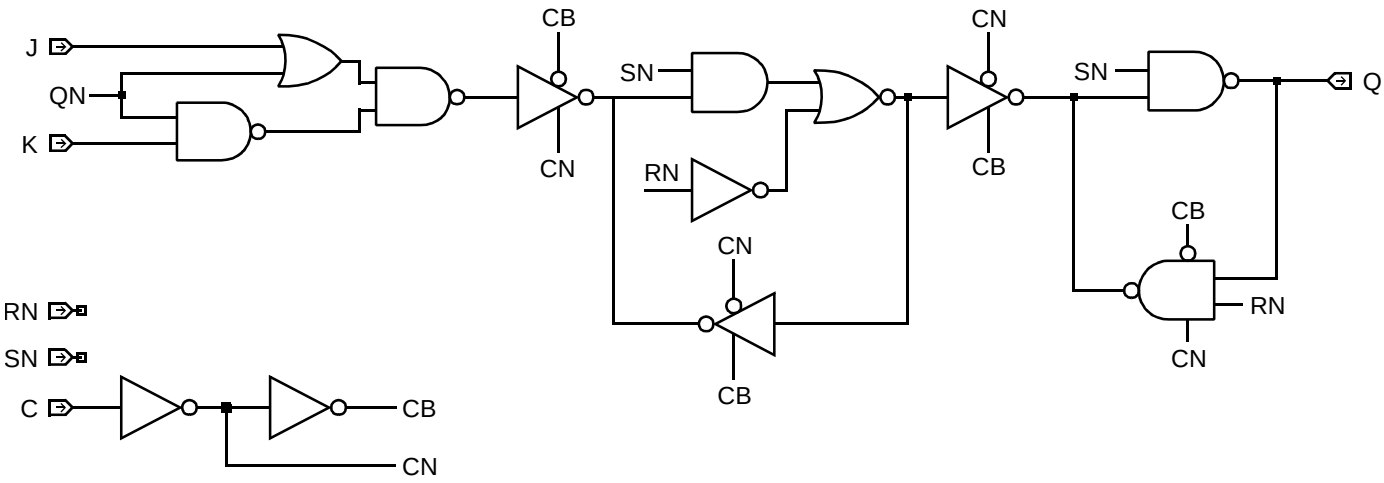
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	2.651
Min C Width	Low	t_w	2.534
Min RN Width	Low	t_w	3.044
Min SN Width	Low	t_w	2.117
Min J Setup		t_{su}	2.475
Min J Hold		t_h	0.542
Min K Setup		t_{su}	2.031
Min K Hold		t_h	0.542
Min RN Setup		t_{su}	1.066
Min RN Hold		t_h	1.510
Min SN Setup		t_{su}	0.709
Min SN Hold		t_h	1.979

Logic Schematic



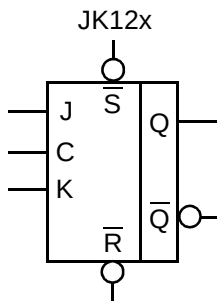
JK12x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

JK12x is a family of static, master-slave JK flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... JK12x *inst_name* (Q, QN, C, J, K, RN, SN);

VHDL..... *inst_name*: JK12x port map (Q, QN, C, J, K, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	JK121	JK122	JK124	JK126
J	1.0	1.0	1.0	1.0
K	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.4	2.2	2.3	2.3
RN	2.2	1.1	1.1	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK121	9.2	3.096	24.5
JK122	9.2	3.670	30.5
JK124	9.8	4.307	34.3
JK126	10.2	5.066	40.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
JK121	From: C To: Q	t_{PLH} t_{PHL}	2.559 2.568	3.306 3.310	4.184 4.033	5.202 4.789	6.032 5.366
	From: C To: QN	t_{PLH} t_{PHL}	3.306 3.251	3.925 3.760	4.759 4.358	5.803 5.052	6.697 5.618
	From: RN To: Q	t_{PHL}	3.051	3.771	4.505	5.290	5.897
	From: RN To: QN	t_{PLH}	3.751	4.372	5.208	6.254	7.150
	From: SN To: Q	t_{PLH}	2.599	3.403	4.288	5.278	6.065
	From: SN To: QN	t_{PHL}	1.158	1.722	2.314	2.976	3.507
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
JK122	From: C To: Q	t_{PLH} t_{PHL}	3.786 3.180	4.593 3.757	5.357 4.235	5.996 4.614	6.674 5.001
	From: C To: QN	t_{PLH} t_{PHL}	2.148 2.349	2.838 2.828	3.597 3.261	4.277 3.616	5.030 3.988
	From: RN To: Q	t_{PHL}	2.279	2.880	3.350	3.713	4.129
	From: RN To: QN	t_{PLH}	4.486	5.277	6.034	6.672	7.351
	From: SN To: Q	t_{PLH}	1.597	2.326	3.093	3.768	4.509
	From: SN To: QN	t_{PHL}	3.049	3.564	3.999	4.347	4.706

AMI500MXSC 0.5 micron CMOS Standard Cell

	Number of Equivalent Loads		1	19	38	56	75 (max)
JK124	From: C To: Q	t_{PLH} t_{PHL}	3.765 3.080	4.509 3.725	5.259 4.194	5.976 4.557	6.747 4.889
	From: C To: QN	t_{PLH} t_{PHL}	2.144 2.504	2.869 3.030	3.577 3.411	4.245 3.750	4.957 4.099
	From: RN To: Q	t_{PHL}	2.240	2.927	3.366	3.740	4.117
	From: RN To: QN	t_{PLH}	4.747	5.468	6.147	6.760	7.386
	From: SN To: Q	t_{PLH}	1.750	2.356	2.986	3.632	4.366
	From: SN To: QN	t_{PHL}	3.169	3.600	4.017	4.399	4.792
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
JK126	From: C To: Q	t_{PLH} t_{PHL}	4.125 3.479	4.701 4.195	5.435 4.605	6.183 4.931	6.910 5.212
	From: C To: QN	t_{PLH} t_{PHL}	2.496 2.711	3.126 3.271	3.776 3.672	4.447 4.026	5.140 4.353
	From: RN To: Q	t_{PHL}	2.559	3.233	3.653	3.999	4.302
	From: RN To: QN	t_{PLH}	3.416	4.113	4.781	5.422	6.035
	From: SN To: Q	t_{PLH}	1.810	2.573	3.278	3.940	4.591
	From: SN To: QN	t_{PHL}	2.449	3.074	3.454	3.747	4.010

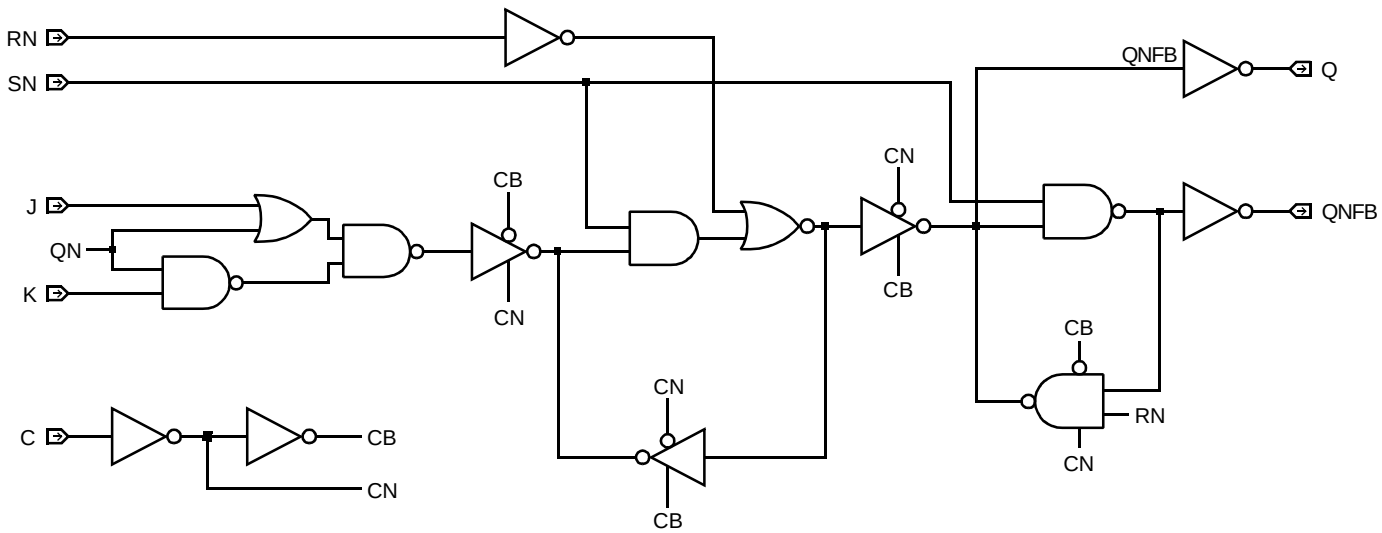
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			JK121	JK122	JK124	JK126
Min C Width	High	t_w	2.781	2.496	2.428	2.605
Min C Width	Low	t_w	2.534	2.403	2.403	2.403
Min RN Width	Low	t_w	3.276	2.690	2.696	2.691
Min SN Width	Low	t_w	2.114	2.177	2.107	1.813
Min J Setup		t_{su}	2.475	2.403	2.403	2.403
Min J Hold		t_h	0.542	0.518	0.517	0.534
Min K Setup		t_{su}	2.031	2.176	2.176	2.176
Min K Hold		t_h	0.542	0.518	0.517	0.534
Min RN Setup		t_{su}	1.066	1.346	1.349	1.347
Min RN Hold		t_h	1.509	1.494	1.494	1.504
Min SN Setup		t_{su}	0.710	0.650	0.651	0.650
Min SN Hold		t_h	1.980	1.887	1.887	1.928

Logic Schematic

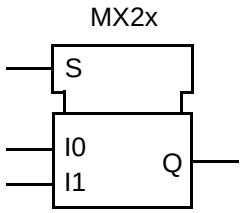


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

MX2x is a family of two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

HDL Syntax

Verilog ..... MX2x *inst_name* (Q, I0, I1, S);

VHDL..... *inst_name*: MX2x port map (Q, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MX21	MX22	MX24	MX26
I0	1.0	1.0	2.0	2.0
I1	1.0	1.0	2.0	2.0
S	1.6	1.6	4.0	4.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX21	2.0	0.714	4.6
MX22	2.0	0.888	5.8
MX24	3.2	1.880	11.2
MX26	3.5	2.242	14.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
MX21	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	1.072 1.252	1.730 1.842	2.547 2.448	3.541 3.098	4.378 3.600
	From: S To: Q	t_{PLH} t_{PHL}	1.532 1.854	2.214 2.372	3.097 2.971	4.119 3.659	4.907 4.215
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
MX22	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.980 1.245	1.762 1.819	2.541 2.308	3.223 2.700	3.984 3.103
	From: S To: Q	t_{PLH} t_{PHL}	1.486 1.917	2.230 2.472	3.006 2.968	3.684 3.375	4.424 3.799
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
MX24	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.904 1.055	1.627 1.697	2.305 2.105	2.964 2.440	3.672 2.771
	From: S To: Q	t_{PLH} t_{PHL}	1.032 1.342	1.750 1.935	2.470 2.380	3.141 2.739	3.844 3.078
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
MX26	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.983 1.176	1.703 1.856	2.389 2.273	3.062 2.615	3.783 2.916
	From: S To: Q	t_{PLH} t_{PHL}	1.091 1.446	1.956 2.088	2.681 2.525	3.357 2.882	4.014 3.185

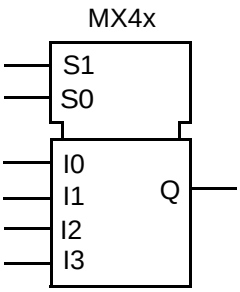
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

MX4x is a family of four-to-one digital multiplexers.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

HDL Syntax

Verilog ..... MX4x *inst_name* (Q, I0, I1, I2, I3, S0, S1);

VHDL..... *inst_name*: MX4x port map (Q, I0, I1, I2, I3, S0, S1);

Pin Loading

Pin Name	Equivalent Loads			
	MX41	MX42	MX44	MX46
I0	1.1	1.1	1.1	1.1
I1	1.1	1.1	1.1	1.1
I2	1.1	1.1	1.1	1.1
I3	1.0	1.0	1.0	1.0
S0	3.5	3.6	3.6	3.7
S1	3.5	2.5	2.4	2.4

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX41	4.5	1.459	12.6
MX42	5.8	2.466	18.0
MX44	6.5	3.084	23.4
MX46	6.8	3.420	26.4

a. See page 2-13 for power equation.

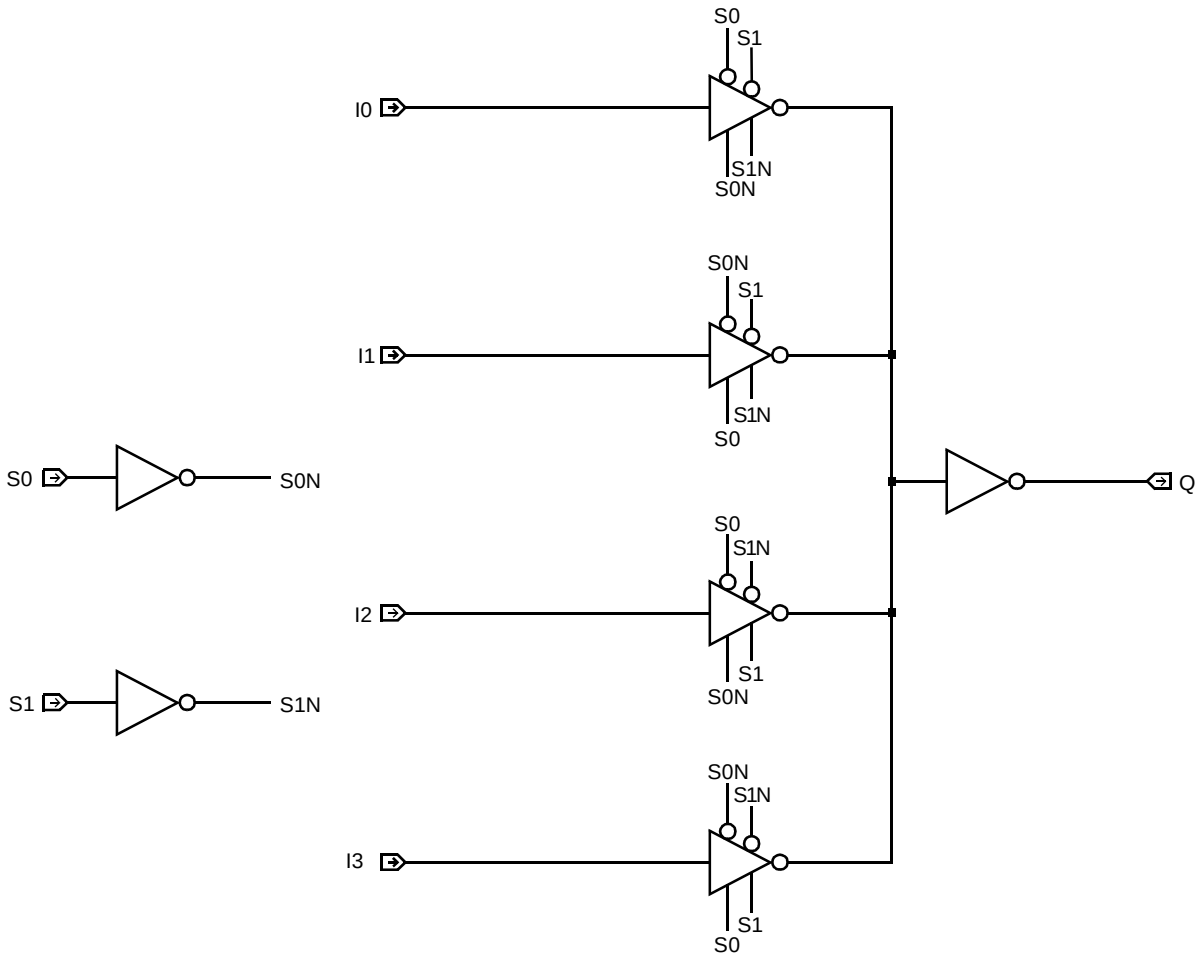
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
MX41	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	1.723 2.936	2.526 3.696	3.415 4.431	4.410 5.195	5.203 5.776
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	2.155 3.535	2.932 4.307	3.812 5.014	4.809 5.725	5.611 6.256
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
MX42	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	1.856 2.097	2.548 2.590	3.318 3.036	4.010 3.403	4.780 3.788
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	2.277 2.674	3.054 3.128	3.823 3.583	4.480 3.974	5.186 4.396
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
MX44	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	1.929 2.036	2.625 2.642	3.266 3.021	3.910 3.324	4.550 3.634
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	2.271 2.788	2.980 3.218	3.614 3.585	4.256 3.904	5.029 4.221
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
MX46	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	2.069 2.063	2.704 2.601	3.370 2.911	4.040 3.125	4.713 3.252
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	2.532 2.794	3.240 3.357	3.958 3.774	4.681 4.114	5.412 4.407

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

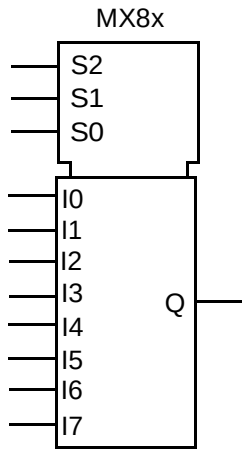
Logic Schematic



Description

MX8x is a family of eight-to-one digital multiplexers.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

HDL Syntax

Verilog ..... MX8x *inst_name* (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

VHDL..... *inst_name*: MX8x port map (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads			
	MX81	MX82	MX84	MX86
I0	1.1	1.1	1.0	1.1
I1	1.1	1.1	1.1	1.1
I2	1.0	1.0	1.1	1.0
I3	1.2	1.2	1.2	1.1
I4	1.0	1.0	1.0	1.0
I5	1.1	1.0	1.1	1.1
I6	1.0	1.0	1.0	1.0
I7	1.1	1.1	1.1	1.1
S0	6.2	6.3	6.3	6.5
S1	3.7	3.8	3.9	4.0
S2	2.4	2.5	3.4	3.4

AMI500MXSC 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX81	9.5	3.555	32.0
MX82	11.0	4.757	41.3
MX84	10.8	4.456	40.8
MX86	12.0	4.869	44.0

a. See page 2-13 for power equation.

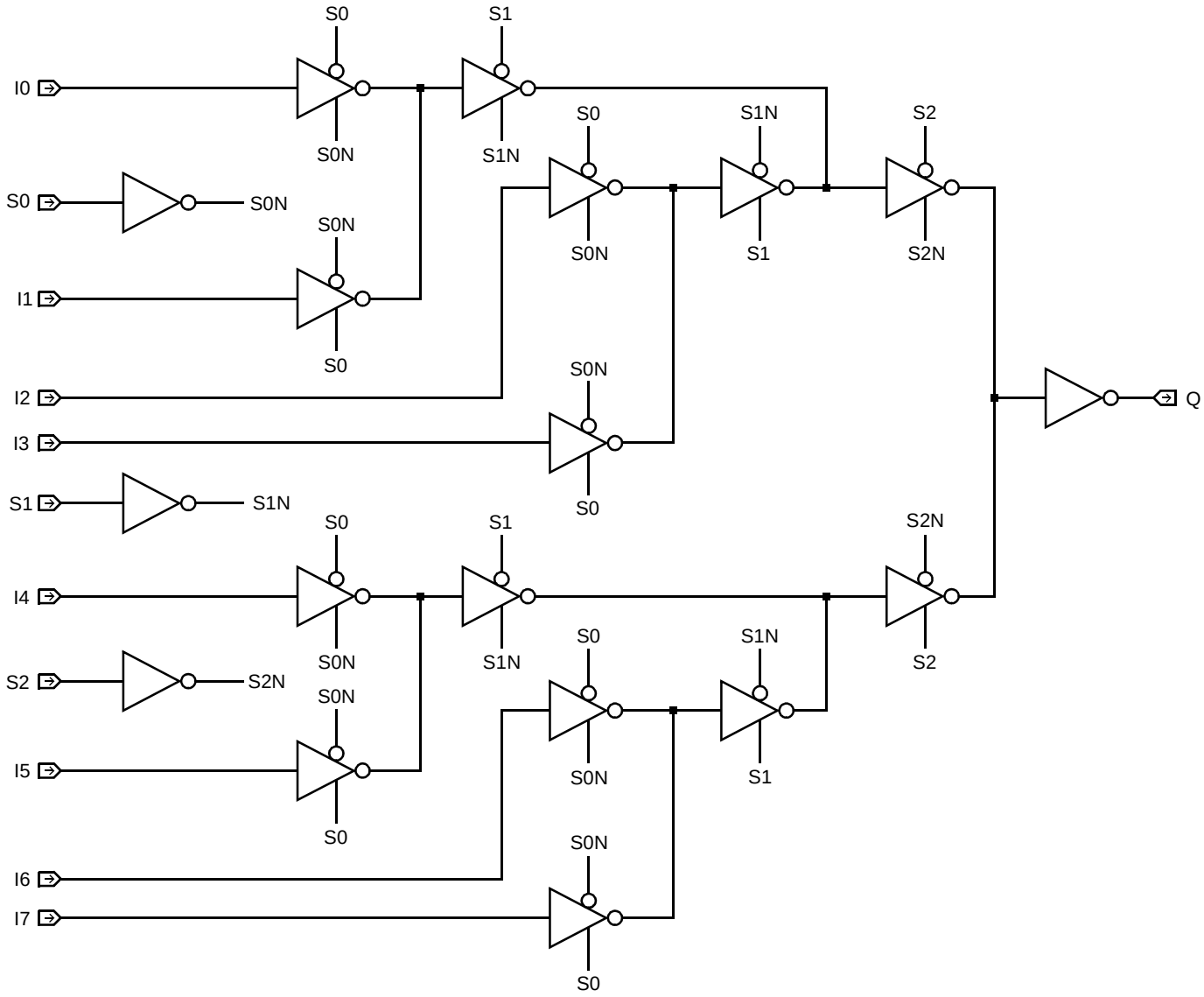
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

MX81	Number of Equivalent Loads		1	5	10	16	21 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	2.738 3.062	3.341 3.686	4.176 4.305	5.239 4.958	6.158 5.458
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	3.624 3.728	4.260 4.287	5.103 4.914	6.148 5.621	7.038 6.187
MX82	Number of Equivalent Loads		1	10	20	29	39 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	2.693 2.797	3.182 3.411	3.633 3.839	4.008 4.154	4.402 4.462
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	3.632 3.551	4.098 4.089	4.551 4.547	4.937 4.915	5.350 5.295
MX84	Number of Equivalent Loads		1	19	38	56	75 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	2.816 3.029	3.702 3.585	4.420 3.934	5.031 4.247	5.632 4.601
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	3.864 3.560	4.499 4.228	5.219 4.679	5.881 5.032	6.521 5.361
MX86	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	2.623 2.872	3.244 3.679	3.915 4.134	4.623 4.495	5.372 4.806
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	3.602 3.673	4.273 4.388	4.977 4.790	5.685 5.173	6.396 5.595

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic

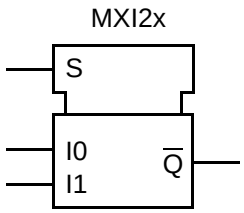


AMI500MXSC 0.5 micron CMOS Standard Cell

Description

MXI2x is a family of inverting two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	QN
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

HDL Syntax

Verilog ..... MXI2x *inst_name* (QN, I0, I1, S);

VHDL..... *inst_name*: MXI2x port map (QN, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MXI21	MXI22	MXI24	MXI26
I0	1.0	1.0	1.1	1.1
I1	1.0	1.0	1.0	1.0
S	1.6	1.6	2.2	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MXI21	2.5	0.910	6.1
MXI22	2.5	1.084	7.3
MXI24	3.2	1.815	11.6
MXI26	3.8	2.440	16.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
MXI21	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	1.519 1.251	2.204 1.737	3.040 2.300	4.030 2.946	4.847 3.470
	From: S To: QN	t_{PLH} t_{PHL}	2.130 1.811	2.777 2.300	3.609 2.860	4.624 3.501	5.478 4.019
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
MXI22	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	1.485 1.210	2.204 1.657	2.968 2.110	3.642 2.500	4.381 2.923
	From: S To: QN	t_{PLH} t_{PHL}	2.159 1.807	2.874 2.270	3.595 2.707	4.260 3.072	5.038 3.460
	Number of Equivalent Loads		**1**	**19**	**38**	**56**	**75 (max)**
MXI24	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	1.590 1.291	2.218 1.870	2.902 2.278	3.550 2.612	4.232 2.934
	From: S To: QN	t_{PLH} t_{PHL}	1.656 1.570	2.467 2.171	3.205 2.575	3.862 2.897	4.530 3.199
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
MXI26	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	1.220 1.195	1.838 1.743	2.495 2.122	3.180 2.431	3.882 2.707
	From: S To: QN	t_{PLH} t_{PHL}	1.589 1.401	2.273 1.915	2.915 2.259	3.558 2.610	4.205 2.970

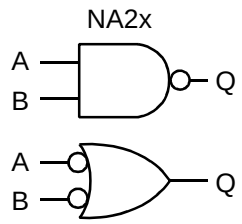
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA2x is a family of 2-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... NA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NA21	NA22	NA23	NA24	NA26
A	1.0	1.8	3.7	1.8	1.8
B	1.0	1.8	3.7	1.8	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA21	1.0	0.346	0.9
NA22	1.2	0.642	1.5
NA23	2.0	1.230	2.7
NA24	2.2	1.643	9.2
NA26	2.5	1.979	11.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.449 0.555	0.819 0.954	1.342 1.445	1.680 1.742	2.171 2.170
NA22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.314 0.290	0.687 0.603	1.097 0.926	1.581 1.268	1.991 1.529
NA23	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.160 0.181	0.630 0.596	1.095 0.926	1.478 1.203	1.878 1.520
NA24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.710 0.762	1.394 1.196	2.101 1.582	2.773 1.912	3.481 2.243
NA26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.846 0.746	1.547 1.325	2.236 1.714	2.902 2.026	3.550 2.294

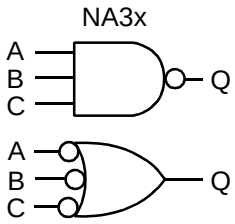
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA3x is a family of 3-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

HDL Syntax

Verilog ..... NA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NA31	NA32	NA33	NA34	NA36
A	1.0	1.9	1.9	1.9	1.9
B	1.0	1.9	1.9	1.9	1.9
C	1.0	1.9	1.9	1.9	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA31	1.2	0.464	1.3
NA32	1.5	0.867	2.4
NA33	2.2	1.387	6.7
NA34	2.8	1.876	10.0
NA36	3.0	2.212	12.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.566 0.694	0.785 0.934	1.209 1.343	1.629 1.716	2.040 2.078
NA32	**Number of Equivalent Loads**		**1**	**4**	**8**	**11**	**15 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.349 0.475	0.708 0.726	1.142 1.009	1.443 1.221	1.820 1.517
NA33	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.914 0.955	1.581 1.415	2.349 1.857	3.053 2.230	3.843 2.626
NA34	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.779 0.895	1.435 1.344	2.185 1.718	2.857 2.038	3.591 2.354
NA36	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.857 0.958	1.547 1.407	2.214 1.774	2.886 2.111	3.561 2.427

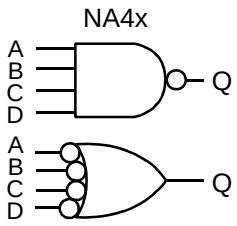
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA4x is a family of 4-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

HDL Syntax

Verilog ..... NA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NA41	NA42	NA43	NA44	NA46
A	1.0	2.0	2.0	2.0	2.0
B	1.0	2.0	2.0	2.0	2.0
C	1.0	2.0	2.0	2.0	2.0
D	1.0	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA41	1.8	0.567	1.7
NA42	2.2	1.056	2.9
NA43	3.0	1.576	7.2
NA44	3.2	2.056	10.5
NA46	3.5	2.392	13.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.647 0.686	0.909 0.952	1.382 1.430	1.608 1.657	2.056 2.102
NA42	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.390 0.510	0.607 0.801	0.910 1.172	1.096 1.403	1.348 1.740
NA43	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.988 1.086	1.676 1.535	2.437 1.971	3.120 2.341	3.878 2.737
NA44	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.904 1.026	1.577 1.464	2.275 1.867	2.930 2.202	3.617 2.511
NA46	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.918 1.073	1.593 1.590	2.264 1.897	2.952 2.222	3.639 2.550

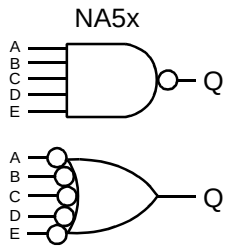
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA5x is a family of 5-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

HDL Syntax

Verilog ..... NA5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NA5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NA51	NA52	NA53	NA54	NA56
A	1.0	1.0	1.9	1.9	1.9
B	1.0	0.9	1.9	1.9	1.9
C	1.0	1.0	2.0	2.0	1.9
D	1.0	1.0	1.9	2.0	1.8
E	1.0	1.0	2.0	2.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA51	2.0	0.666	2.2
NA52	3.0	1.166	6.9
NA53	3.5	2.018	9.8
NA54	3.5	2.511	14.1
NA56	4.0	2.853	16.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA51	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.709 0.838	0.997 1.129	1.268 1.392	1.536 1.646	2.083 2.169
NA52	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.178 1.441	1.881 1.982	2.717 2.570	3.693 3.223	4.491 3.740
NA53	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.920 1.266	1.660 1.831	2.431 2.316	3.107 2.707	3.844 3.111
NA54	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.781 1.085	1.448 1.609	2.162 2.017	2.837 2.356	3.550 2.686
NA56	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.896 1.232	1.603 1.820	2.276 2.225	2.991 2.561	3.750 2.842

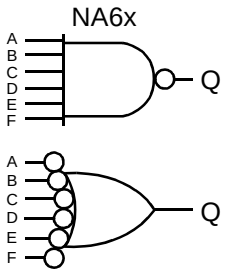
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA6x is a family of 6-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: NA6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads				
	NA61	NA62	NA63	NA64	NA66
A	1.0	1.9	1.9	1.9	1.9
B	1.0	1.9	1.9	1.9	1.9
C	1.0	2.0	2.0	2.0	2.0
D	1.0	2.0	2.0	2.0	2.0
E	1.0	1.9	1.9	1.9	1.9
F	1.0	2.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA61	3.2	1.283	7.5
NA62	3.5	2.417	13.0
NA63	4.0	2.588	14.0
NA64	4.0	2.745	15.1
NA66	4.2	3.082	17.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA61	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.266 1.523	1.923 2.057	2.757 2.647	3.768 3.307	4.615 3.834
NA62	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.882 1.060	1.582 1.552	2.351 2.004	3.040 2.378	3.802 2.772
NA63	**Number of Equivalent Loads**		**1**	**14**	**28**	**43**	**57 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.828 1.052	1.514 1.562	2.211 1.972	2.939 2.359	3.607 2.691
NA64	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.878 1.153	1.567 1.681	2.264 2.057	2.905 2.369	3.581 2.673
NA66	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.933 1.220	1.586 1.853	2.262 2.248	2.936 2.573	3.610 2.859

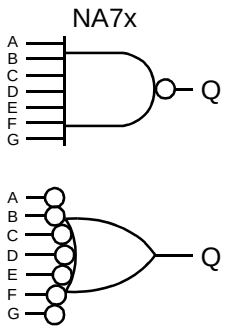
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA7x is a family of 7-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	X	X	X	X	X	X	H
X	L	X	X	X	X	X	H
X	X	L	X	X	X	X	H
X	X	X	L	X	X	X	H
X	X	X	X	L	X	X	H
X	X	X	X	X	L	X	H
X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA7x *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: NA7x port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads				
	NA71	NA72	NA73	NA74	NA76
A	1.9	1.9	1.9	1.9	1.9
B	1.9	1.9	1.9	1.9	1.9
C	2.0	2.0	2.0	2.0	2.0
D	2.1	2.1	2.0	2.1	2.0
E	2.0	2.0	2.0	2.1	2.0
F	2.0	2.0	1.9	2.0	2.0
G	2.0	2.0	1.9	2.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA71	4.5	2.504	11.9
NA72	4.5	2.852	17.0
NA73	4.8	3.013	17.8
NA74	4.8	3.170	19.2
NA76	5.0	3.506	21.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA71	Number of Equivalent Loads		1	5	10	16	21 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.140 1.822	1.827 2.444	2.667 3.079	3.660 3.760	4.481 4.288
NA72	Number of Equivalent Loads		1	10	20	29	39 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.012 1.513	1.719 2.100	2.460 2.576	3.127 2.949	3.887 3.329
NA73	Number of Equivalent Loads		1	14	28	43	57 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.962 1.536	1.671 2.143	2.368 2.581	3.086 2.976	3.738 3.305
NA74	Number of Equivalent Loads		1	19	38	56	75 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.010 1.474	1.693 2.251	2.374 2.699	3.028 3.024	3.735 3.310
NA76	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.015 1.587	1.738 2.398	2.415 2.870	3.069 3.246	3.712 3.571

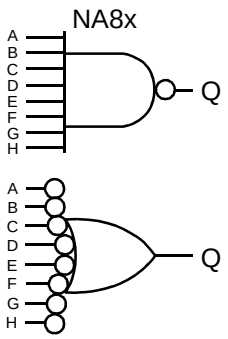
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NA8x is a family of 8-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA8x *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: NA8x port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads				
	NA81	NA82	NA83	NA84	NA86
A	1.0	1.9	1.9	1.9	1.9
B	1.0	1.8	1.9	1.9	1.9
C	1.0	1.8	1.9	1.9	1.9
D	1.0	1.9	1.9	1.9	1.9
E	1.0	1.9	2.0	2.0	1.9
F	1.0	1.8	1.9	1.9	1.9
G	1.0	2.0	1.9	1.9	2.0
H	1.0	1.9	1.9	1.9	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA81	3.8	1.469	8.1
NA82	4.8	3.068	17.5
NA83	4.8	3.222	18.8
NA84	4.8	3.381	19.9
NA86	5.0	3.719	22.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NA81	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.428 1.629	2.097 2.149	2.933 2.740	3.934 3.413	4.769 3.955
NA82	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.978 1.471	1.677 2.008	2.440 2.496	3.128 2.898	3.896 3.320
NA83	**Number of Equivalent Loads**		**1**	**14**	**28**	**43**	**57 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.964 1.508	1.649 2.128	2.343 2.577	3.079 2.982	3.771 3.320
NA84	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.958 1.561	1.681 2.228	2.349 2.662	2.990 3.002	3.717 3.322
NA86	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.006 1.709	1.698 2.469	2.401 2.921	3.079 3.278	3.729 3.582

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

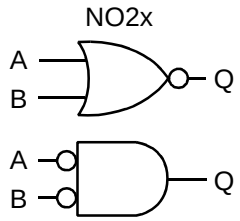
NO2x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NO2x is a family of 2-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

HDL Syntax

Verilog ..... NO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NO21	NO22	NO23	NO24	NO26
A	0.9	1.9	3.7	1.8	1.8
B	0.9	2.0	3.6	1.8	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO21	1.0	0.383	0.9
NO22	1.5	0.720	1.4
NO23	1.8	1.385	3.1
NO24	2.5	1.807	9.6
NO26	2.8	2.154	11.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.481 0.505	1.141 0.779	2.035 1.108	2.605 1.320	3.445 1.650
NO22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.442 0.315	1.052 0.569	1.766 0.800	2.636 1.054	3.374 1.270
NO23	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.333 0.259	1.013 0.559	1.665 0.805	2.242 1.013	2.903 1.251
NO24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.880 0.748	1.562 1.198	2.277 1.525	2.954 1.874	3.672 2.236
NO26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.920 0.839	1.637 1.277	2.344 1.619	3.042 1.956	3.735 2.304

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

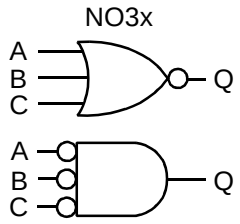
NO3x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NO3x is a family of 3-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

HDL Syntax

Verilog ..... NO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NO31	NO32	NO33	NO34	NO36
A	1.0	1.9	1.9	1.9	1.9
B	1.0	1.9	1.9	1.9	1.9
C	0.9	1.8	1.8	1.8	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO31	1.2	0.539	1.5
NO32	1.2	1.004	2.4
NO33	2.2	1.574	7.1
NO34	2.8	2.108	10.6
NO36	2.8	2.448	12.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.002 0.544	1.433 0.696	2.242 0.946	3.049 1.164	3.889 1.366
NO32	**Number of Equivalent Loads**		**1**	**4**	**8**	**11**	**15 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.584 0.248	1.215 0.492	2.017 0.748	2.605 0.913	3.384 1.112
NO33	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.267 0.880	1.988 1.341	2.752 1.790	3.424 2.171	4.162 2.579
NO34	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.180 0.785	1.906 1.256	2.673 1.595	3.354 1.908	4.045 2.260
NO36	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.242 0.827	1.945 1.324	2.620 1.686	3.313 2.024	4.024 2.360

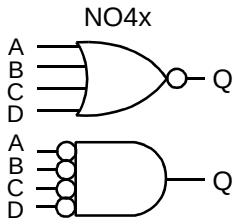
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NO4x is a family of 4-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... NO4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NO4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NO41	NO42	NO43	NO44	NO46
A	1.0	1.0	1.8	1.9	1.8
B	1.0	1.0	1.8	1.8	1.8
C	1.0	1.0	1.8	1.8	1.8
D	1.0	1.0	1.9	1.8	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO41	1.8	0.664	1.8
NO42	2.8	1.154	6.3
NO43	2.5	1.793	7.4
NO44	2.8	2.328	11.4
NO46	3.0	2.671	13.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.143 0.411	1.675 0.610	2.705 0.951	3.222 1.100	4.278 1.372
NO42	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.358 1.210	2.059 1.688	2.902 2.257	3.891 2.920	4.704 3.463
NO43	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.431 0.924	2.085 1.377	2.842 1.829	3.536 2.217	4.317 2.634
NO44	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.312 0.796	1.986 1.236	2.685 1.645	3.343 1.971	4.034 2.298
NO46	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.404 0.848	2.065 1.323	2.742 1.694	3.427 2.023	4.123 2.327

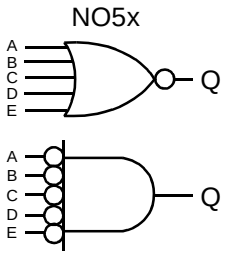
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

NO5x is a family of 5-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

HDL Syntax

Verilog ..... NO5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NO5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NO51	NO52	NO53	NO54	NO56
A	1.0	1.0	1.9	1.9	1.8
B	1.1	1.0	1.9	1.8	1.8
C	1.0	1.0	1.9	1.9	1.9
D	1.0	1.0	1.9	1.9	1.8
E	1.0	1.0	1.8	1.8	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
NO51	2.0	0.788	2.1
NO52	3.0	1.310	6.8
NO53	3.0	2.271	10.0
NO54	3.5	2.816	14.1
NO56	3.5	3.169	16.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

NO51	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.307 0.626	1.941 0.800	2.575 0.951	3.211 1.091	4.499 1.352
NO52	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.408 1.260	2.113 1.748	2.920 2.312	3.891 2.966	4.749 3.501
NO53	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.160 1.078	1.897 1.553	2.645 2.002	3.314 2.378	4.082 2.777
NO54	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.940 0.849	1.644 1.336	2.355 1.720	3.021 2.041	3.732 2.352
NO56	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.037 0.969	1.728 1.484	2.410 1.853	3.093 2.175	3.787 2.470

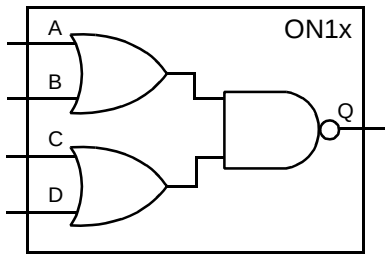
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON1x is a family of OR-NAND circuits consisting of two 2-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON11	ON12	ON14	ON16
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.8
C	1.0	1.0	1.0	1.9
D	1.0	1.0	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON11	1.5	0.485	2.3
ON12	2.8	1.285	6.8
ON14	2.5	1.448	7.6
ON16	3.2	2.790	13.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON11	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.837 0.654	1.539 1.021	2.612 1.516	3.335 1.842	4.397 2.324
ON12	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.366 1.274	2.067 1.815	2.905 2.404	3.887 3.059	4.692 3.579
ON14	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.285 1.311	2.022 1.854	2.798 2.323	3.480 2.702	4.227 3.095
ON16	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.934 1.025	1.672 1.543	2.349 1.948	2.983 2.288	3.645 2.619

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

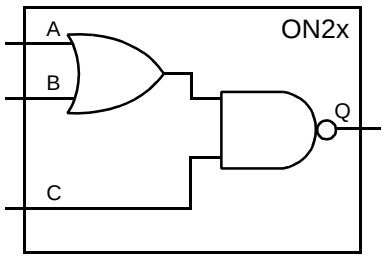
ON2X

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON2x is a family of OR-NAND circuits consisting of one 2-input OR and a direct input into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	Q
L	L	X	H
X	X	L	H
All other combinations			L

HDL Syntax

Verilog ..... ON2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: ON2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	ON21	ON22	ON24	ON26
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.9
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON21	1.2	0.399	1.8
ON22	2.5	1.122	6.0
ON24	2.5	1.296	7.2
ON26	3.0	2.309	13.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON21	**Number of Equivalent Loads**		**1**	**3**	**6**	**8**	**11 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.710 0.711	1.559 1.137	2.665 1.637	3.350 1.934	4.344 2.357
ON22	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.314 1.277	1.945 1.831	2.774 2.416	3.799 3.055	4.668 3.556
ON24	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.303 1.308	1.990 1.876	2.749 2.342	3.431 2.710	4.188 3.085
ON26	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.970 1.045	1.603 1.583	2.300 1.952	2.971 2.264	3.687 2.580

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

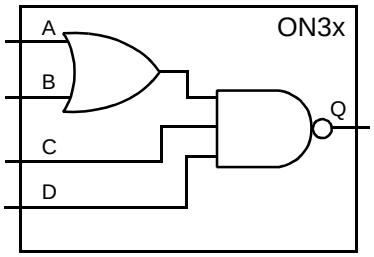
ON3x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON3x is a family of OR-NAND circuits consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON31	ON32	ON34	ON36
A	0.9	1.1	1.0	1.9
B	1.0	1.0	1.0	1.8
C	1.0	1.0	1.0	1.9
D	1.0	1.0	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON31	1.5	0.524	2.1
ON32	2.8	1.154	6.7
ON34	2.8	1.328	7.6
ON36	3.2	2.533	14.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.834 0.706	1.301 0.945	2.164 1.364	2.978 1.756	3.766 2.134
ON32	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.389 1.320	2.054 1.872	2.890 2.458	3.896 3.099	4.737 3.602
ON34	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.323 1.324	2.077 1.879	2.836 2.357	3.490 2.741	4.197 3.139
ON36	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.977 0.899	1.652 1.468	2.343 1.877	3.002 2.205	3.702 2.516

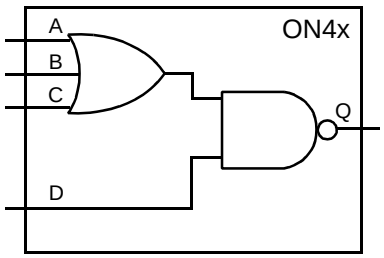
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ON4x

Description

ON4x is a family of OR-NAND circuits consisting of one 3-input OR gate into and a direct input into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON41	ON42	ON44	ON46
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.9
C	1.0	1.0	1.0	1.8
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON41	1.5	0.433	2.3
ON42	2.8	1.276	6.6
ON44	2.8	1.450	7.8
ON46	3.5	2.612	13.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON41	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.202 0.531	1.706 0.804	2.693 1.278	3.678 1.692	4.671 2.061
ON42	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.749 1.357	2.392 1.903	3.225 2.488	4.246 3.130	5.109 3.635
ON44	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.747 1.396	2.499 1.937	3.266 2.416	3.930 2.806	4.649 3.211
ON46	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.268 0.968	1.951 1.517	2.657 1.924	3.318 2.250	4.015 2.556

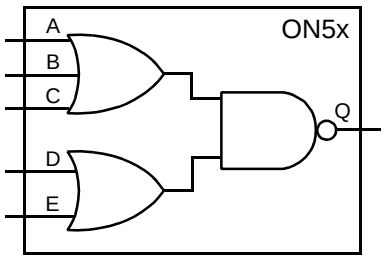
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON5x is a family of OR-NAND circuits consisting of one 3-input OR gate and one 2-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	L	H
All other combinations					L

HDL Syntax

Verilog ..... ON5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON52	ON54	ON56
A	1.1	1.1	1.9
B	1.1	1.1	1.8
C	1.1	1.1	1.8
D	1.0	1.0	1.9
E	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON52	3.0	1.437	7.0
ON54	3.0	1.611	8.3
ON56	3.5	3.086	14.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON52	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.777 1.390	2.436 1.899	3.273 2.491	4.286 3.173	5.135 3.727
ON54	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.770 1.438	2.544 1.968	3.304 2.447	3.953 2.840	4.649 3.252
ON56	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.346 0.993	2.026 1.537	2.737 1.931	3.414 2.253	4.143 2.562

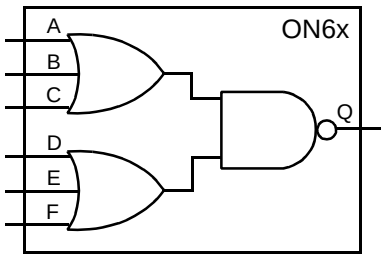
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON6x is a family of OR-NAND circuits consisting of two 3-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	L	H
All other combinations						L

HDL Syntax

Verilog ..... ON6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ON6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ON62	ON64	ON66
A	1.0	1.0	1.9
B	1.1	1.1	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	1.8
F	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON62	3.2	1.591	7.5
ON64	3.2	1.764	8.8
ON66	4.0	3.397	15.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON62	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.820 1.409	2.512 1.936	3.351 2.519	4.339 3.177	5.154 3.706
ON64	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.843 1.369	2.572 1.932	3.339 2.411	4.012 2.795	4.747 3.192
ON66	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.249 1.036	1.934 1.579	2.654 1.985	3.322 2.305	4.016 2.628

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

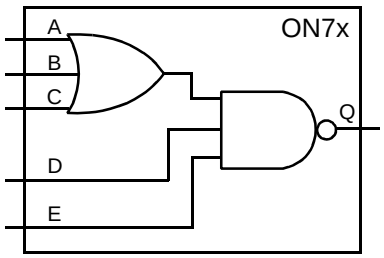
ON7x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON7x is a family of OR-NAND circuits consisting of one 3-input OR gate a two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Core Logic

HDL Syntax

Verilog ..... ON7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON72	ON74	ON76
A	1.0	1.0	1.9
B	1.0	1.0	1.8
C	1.0	1.0	1.8
D	1.0	1.0	1.9
E	1.0	1.0	1.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON72	3.0	1.305	6.9
ON74	3.0	1.480	8.2
ON76	3.5	2.826	14.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON72	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.754 1.373	2.459 1.930	3.299 2.516	4.278 3.156	5.079 3.657
ON74	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.629 1.453	2.316 1.985	3.083 2.436	3.776 2.816	4.546 3.232
ON76	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.272 1.074	1.989 1.636	2.669 2.033	3.322 2.371	4.016 2.720

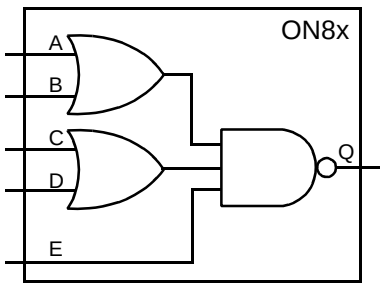
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON8x is a family of OR-NAND circuits consisting of two 2-input OR gates and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	X	X	X	H
X	X	L	L	X	H
X	X	X	X	L	H
All other combinations					L

HDL Syntax

Verilog ..... ON8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON82	ON84	ON86
A	1.1	1.0	1.9
B	1.1	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.8
E	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON82	3.5	1.633	8.7
ON84	3.5	1.807	10.1
ON86	4.2	3.461	17.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON82	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.436 1.636	2.138 2.248	2.978 2.880	3.962 3.561	4.768 4.090
ON84	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.444 1.704	2.161 2.362	2.929 2.893	3.609 3.310	4.356 3.732
ON86	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.994 1.343	1.703 2.002	2.423 2.450	3.109 2.816	3.840 3.166

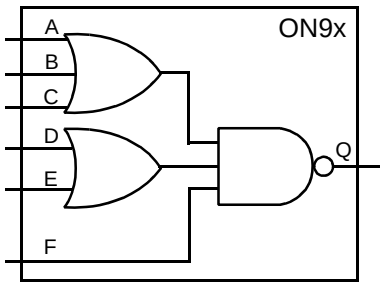
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ON9x is a family of OR-NAND circuits consisting of one 3-input OR gate, one 2-input OR gate, and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	X	H
X	X	X	X	X	L	H
All other combinations						L

HDL Syntax

Verilog ..... ON9x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ON9x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ON92	ON94	ON96
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.8
D	1.0	1.0	1.8
E	1.0	1.0	1.8
F	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON92	4.0	1.797	9.0
ON94	4.0	1.970	10.3
ON96	4.5	3.760	18.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON92	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.868 1.724	2.605 2.338	3.447 2.973	4.407 3.659	5.182 4.193
ON94	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.904 1.756	2.612 2.384	3.382 2.922	4.068 3.353	4.826 3.798
ON96	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.361 1.329	2.040 2.005	2.740 2.451	3.396 2.815	4.088 3.173

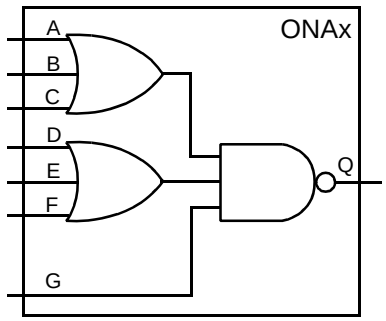
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ONAx

Description

ONAx is a family of OR-NAND circuits consisting of two 3-input OR gates and a direct input into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	L	X	H
X	X	X	X	X	X	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONAx port map (Q, A, B, C, D, E, F, G;)

Pin Loading

Pin Name	Equivalent Loads		
	ONA2	ONA4	ONA6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.8
D	1.0	1.1	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.8
G	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONA2	4.2	1.951	9.8
ONA4	4.2	2.125	11.0
ONA6	5.0	4.067	19.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONA2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.892 1.728	2.562 2.365	3.402 2.995	4.410 3.660	5.250 4.169
ONA4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.899 1.797	2.624 2.462	3.394 2.948	4.072 3.344	4.817 3.789
ONA6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.350 1.361	2.004 2.000	2.731 2.422	3.434 2.765	4.185 3.095

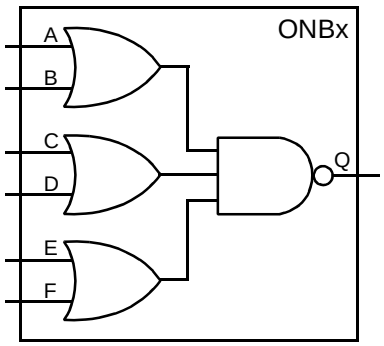
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ONBx

Description

ONBx is a family of OR-NAND circuits consisting of three 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	X	X	X	X	H
X	X	L	L	X	X	H
X	X	X	X	L	L	H
All other combinations						L

HDL Syntax

Verilog ..... ONBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ONBx port map (Q, A, B, C, D, E, F)

Pin Loading

Pin Name	Equivalent Loads		
	ONB2	ONB4	ONB6
A	1.1	1.0	1.9
B	1.0	1.0	1.8
C	1.1	1.0	1.9
D	1.0	1.0	1.8
E	1.1	1.0	1.9
F	1.1	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONB2	3.8	1.793	9.1
ONB4	3.8	1.967	10.1
ONB6	4.5	3.771	18.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONB2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.422 1.685	2.155 2.274	2.995 2.912	3.956 3.617	4.733 4.175
ONB4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.442 1.678	2.122 2.301	2.861 2.836	3.534 3.267	4.289 3.712
ONB6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.997 1.296	1.726 1.972	2.414 2.398	3.064 2.752	3.747 3.097

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

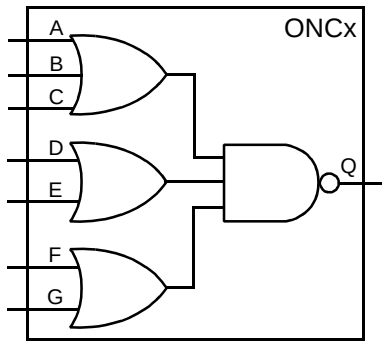
ONCx

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ONCx is a family of OR-NAND circuits consisting of one 3-input OR gate and two 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	X	X	H
X	X	X	X	X	L	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ONC2	ONC4	ONC6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.8
D	1.0	1.0	1.9
E	1.0	1.0	1.8
F	1.0	1.0	1.9
G	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONC2	4.0	1.947	9.4
ONC4	4.0	2.124	10.8
ONC6	4.8	4.070	19.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONC2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.878 1.719	2.583 2.363	3.424 2.991	4.408 3.645	5.213 4.144
ONC4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.870 1.758	2.563 2.433	3.332 2.955	4.025 3.358	4.795 3.762
ONC6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.326 1.282	2.043 1.963	2.737 2.410	3.371 2.760	4.049 3.087

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

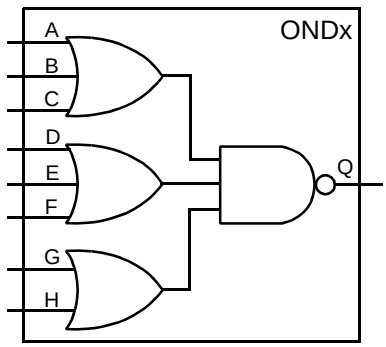
ONDx

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ONDx is a family of OR-NAND circuits consisting of two 3-input OR gates and one 2-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	L	L	X	X	X	X	X	H
X	X	X	L	L	L	X	X	H
X	X	X	X	X	X	L	L	H
All other combinations								L

HDL Syntax

Verilog ..... ONDx *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: ONDx port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads		
	OND2	OND4	OND6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.8
D	1.1	1.1	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.8
G	1.0	1.0	1.9
H	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OND2	4.5	2.111	10.1
OND4	4.5	2.285	11.4
OND6	5.0	4.369	20.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OND2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.895 1.735	2.608 2.329	3.450 2.966	4.429 3.667	5.228 4.220
OND4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.915 1.759	2.620 2.423	3.389 2.959	4.075 3.372	4.833 3.783
OND6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.348 1.471	2.089 2.087	2.765 2.481	3.412 2.830	4.099 3.199

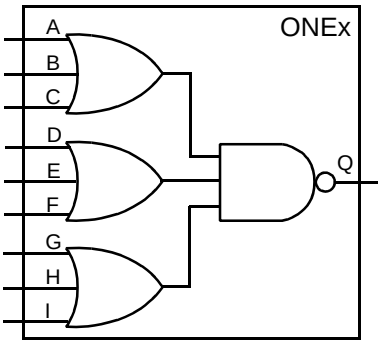
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

ONEx is a family of OR-NAND circuits consisting of three 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
L	L	L	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	L	L	L	H
All other combinations									L

HDL Syntax

Verilog ..... ONEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ONEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ONE2	ONE4	ONE6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.8
D	1.1	1.1	1.9
E	1.0	1.0	1.9
F	1.0	1.0	1.8
G	1.0	1.0	1.9
H	1.0	1.0	1.9
I	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONE2	4.8	2.265	10.5
ONE4	4.8	2.439	11.7
ONE6	5.5	4.673	21.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONE2	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.889 1.719	2.545 2.314	3.383 2.950	4.400 3.649	5.254 4.200
ONE4	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.896 1.758	2.653 2.426	3.420 2.951	4.083 3.357	4.800 3.767
ONE6	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	1.364 1.382	2.074 1.969	2.764 2.381	3.405 2.735	4.082 3.078

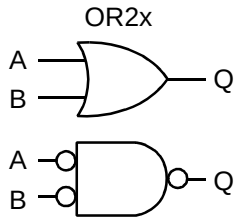
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

OR2x is a family of 2-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

HDL Syntax

Verilog ..... OR2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR21	OR22	OR24	OR26
A	1.0	1.0	1.9	1.9
B	1.0	1.0	1.9	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR21	1.2	0.570	2.4
OR22	1.5	0.747	3.5
OR24	1.8	1.420	6.3
OR26	2.0	1.781	9.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR21	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.756 0.908	1.427 1.450	2.246 2.027	3.234 2.676	4.066 3.212
OR22	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.708 0.953	1.423 1.573	2.200 2.035	2.893 2.408	3.658 2.816
OR24	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.461 0.816	1.162 1.288	1.855 1.644	2.501 1.955	3.209 2.279
OR26	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.619 0.808	1.306 1.458	1.959 1.819	2.635 2.159	3.336 2.508

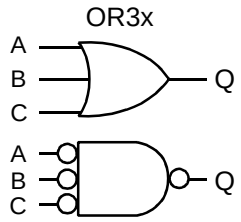
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

OR3x is a family of 3-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

HDL Syntax

Verilog ..... OR3x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR3x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR31	OR32	OR34	OR36
A	1.0	1.0	1.8	3.0
B	1.0	1.0	1.8	3.0
C	1.0	1.0	1.9	2.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR31	1.5	0.724	3.0
OR32	1.5	0.898	4.2
OR34	2.0	1.719	7.6
OR36	3.5	2.595	11.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR31	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.821 1.300	1.509 1.921	2.333 2.549	3.322 3.220	4.165 3.740
OR32	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.804 1.326	1.506 1.999	2.278 2.524	2.971 2.942	3.738 3.380
OR34	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.534 1.071	1.251 1.717	1.939 2.140	2.597 2.495	3.314 2.849
OR36	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.523 0.856	1.235 1.527	1.888 1.971	2.572 2.318	3.264 2.653

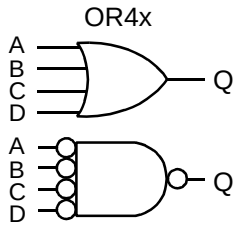
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

OR4x is a family of 4-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

HDL Syntax

Verilog ..... OR4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: OR4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	OR41	OR42	OR44	OR46
A	1.1	1.1	2.9	2.8
B	1.1	1.1	2.8	2.9
C	1.1	1.1	2.9	2.9
D	1.1	1.1	3.0	2.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR41	2.0	0.851	3.4
OR42	2.0	1.025	4.7
OR44	3.2	2.554	9.4
OR46	3.5	2.919	12.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR41	**Number of Equivalent Loads**		**1**	**5**	**10**	**16**	**21 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.893 1.543	1.576 2.251	2.414 2.930	3.407 3.632	4.229 4.164
OR42	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.914 1.578	1.615 2.340	2.371 2.916	3.052 3.356	3.813 3.794
OR44	**Number of Equivalent Loads**		**1**	**19**	**38**	**56**	**75 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.526 0.911	1.237 1.622	1.911 2.048	2.551 2.418	3.266 2.770
OR46	**Number of Equivalent Loads**		**1**	**28**	**56**	**84**	**112 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.501 1.077	1.174 1.789	1.845 2.246	2.516 2.627	3.199 2.965

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

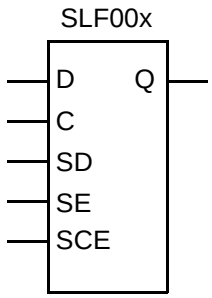
SLF00x

AMI500MXSC 0.5 micron CMOS Standard Cell

Description

SLF00x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low.

Logic Symbol



Truth Table

C	D	SD	SE	SCE	Q
↑	H	X	L	L	H
↑	L	X	L	L	L
↑	X	H	H	L	H
↑	X	L	H	L	L
L	X	X	X	L	NC
L	H	X	L	H	H
L	L	X	L	H	L
L	X	H	H	H	H
L	X	L	H	H	L
H	X	X	X	H	NC

NC = No Change

HDL Syntax

Verilog ..... SLF00x *inst_name* (Q, C, D, SCE, SD, SE);

VHDL..... *inst_name*: SLF00x port map (Q, C, D, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF001	SLF002	SLF004	SLF006
C	1.0	1.1	1.1	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3
SCE	1.0	1.1	1.0	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF001	7.2	2.592	13.7
SLF002	7.8	2.965	17.1
SLF004	8.2	3.335	19.9
SLF006	8.5	3.679	22.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
SLF001	From: C To: Q	t_{PLH} t_{PHL}	2.84 4.23	3.60 4.75	4.45 5.38	5.41 6.12	6.18 6.74
	From: D To: Q	t_{PLH} t_{PHL}	2.67 3.83	3.39 4.39	4.25 5.02	5.24 5.74	6.05 6.32
	From: SCE To: Q	t_{PLH} t_{PHL}	1.80 1.77	2.50 2.39	3.35 3.01	4.36 3.69	5.18 4.21
	From: SD To: Q	t_{PLH} t_{PHL}	2.66 3.79	3.37 4.40	4.22 5.03	5.22 5.71	6.04 6.23
	From: SE To: Q	t_{PLH} t_{PHL}	2.92 4.22	3.62 4.83	4.48 5.46	5.48 6.13	6.31 6.66
SLF002	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	2.83 4.02	3.52 4.57	4.28 5.05	4.98 5.44	5.75 5.84
	From: D To: Q	t_{PLH} t_{PHL}	2.64 3.68	3.40 4.31	4.17 4.76	4.83 5.10	5.55 5.42
	From: SCE To: Q	t_{PLH} t_{PHL}	1.75 1.43	2.41 2.01	3.18 2.49	3.87 2.87	4.66 3.26
	From: SD To: Q	t_{PLH} t_{PHL}	2.53 3.55	3.33 3.95	4.10 4.43	4.74 4.88	5.41 5.39
	From: SE To: Q	t_{PLH} t_{PHL}	2.93 4.03	3.55 4.53	4.31 5.02	5.03 5.43	5.86 5.87

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	Number of Equivalent Loads		1	19	38	56	75 (max)
SLF004	From: C To: Q	t_{PLH} t_{PHL}	2.88 4.18	3.73 4.77	4.39 5.11	5.01 5.38	5.63 5.64
	From: D To: Q	t_{PLH} t_{PHL}	2.71 3.70	3.36 4.22	4.00 4.56	4.61 4.84	5.25 5.13
	From: SCE To: Q	t_{PLH} t_{PHL}	1.83 1.51	2.48 2.12	3.16 2.52	3.82 2.86	4.50 3.19
	From: SD To: Q	t_{PLH} t_{PHL}	2.70 3.67	3.42 4.26	4.08 4.62	4.73 4.90	5.49 5.15
	From: SE To: Q	t_{PLH} t_{PHL}	2.87 4.15	3.77 4.68	4.48 5.08	5.08 5.41	5.66 5.74
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
SLF006	From: C To: Q	t_{PLH} t_{PHL}	2.99 4.14	3.74 4.93	4.44 5.29	5.11 5.59	5.76 5.85
	From: D To: Q	t_{PLH} t_{PHL}	2.81 3.89	3.62 4.67	4.30 5.02	4.97 5.27	5.64 5.49
	From: SCE To: Q	t_{PLH} t_{PHL}	1.77 1.92	2.55 2.43	3.24 2.76	3.90 3.12	4.56 3.53
	From: SD To: Q	t_{PLH} t_{PHL}	2.78 3.77	3.55 4.33	4.23 4.73	4.86 5.10	5.46 5.46
	From: SE To: Q	t_{PLH} t_{PHL}	3.08 4.28	3.71 4.85	4.39 5.30	5.08 5.70	5.77 6.08

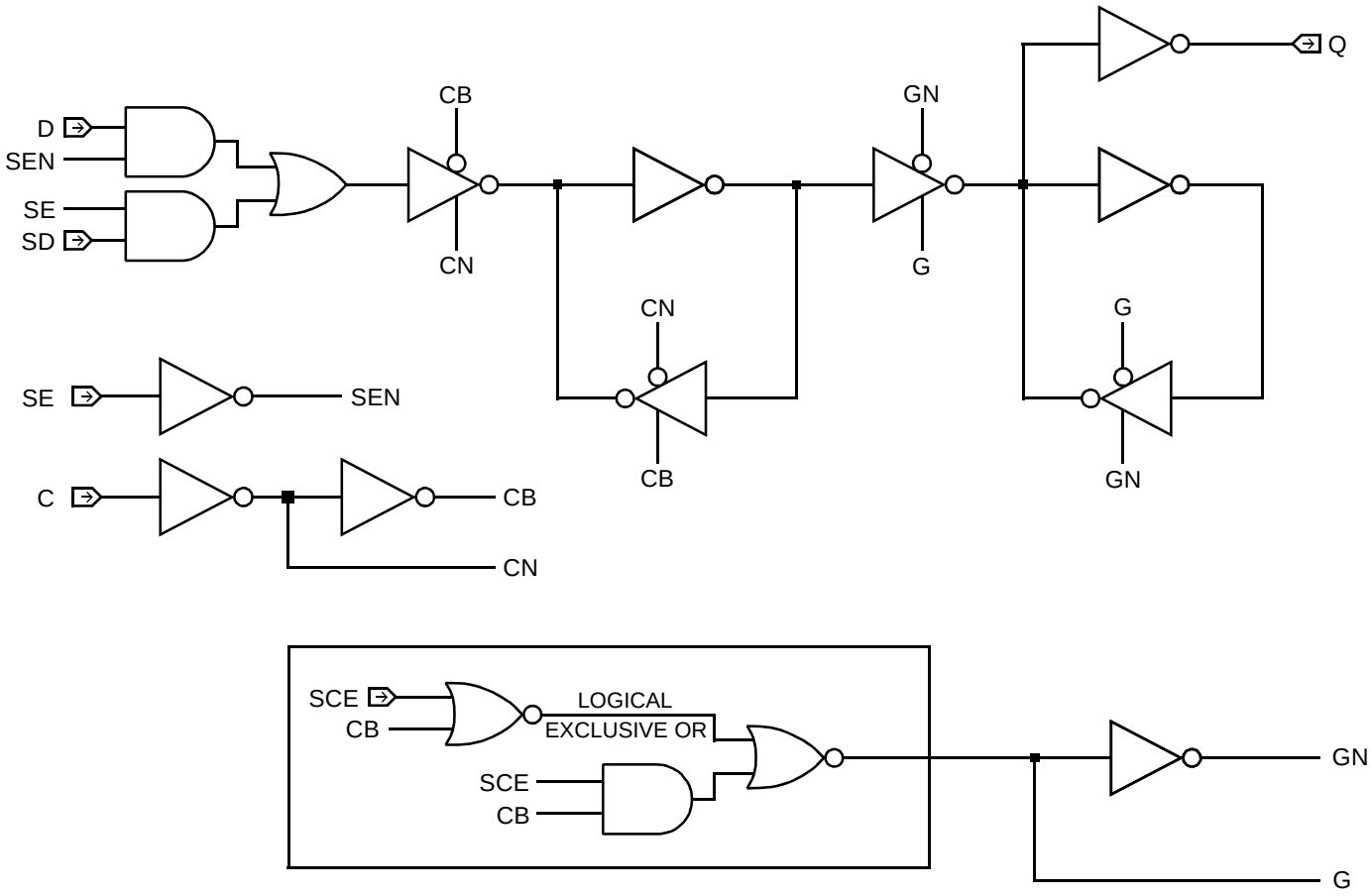
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF001	SLF002	SLF004	SLF006
Min C Width	High	t_w	2.51	2.56	2.69	2.80
Min C Width	Low	t_w	2.80	2.92	2.93	2.93
Min D Setup		t_{su}	2.40	2.52	2.52	2.52
Min D Hold		t_h	0.46	0.46	0.46	0.46
Min SD Setup		t_{su}	2.40	2.52	2.52	2.52
Min SD Hold		t_h	0.46	0.46	0.46	0.46
Min SE Setup		t_{su}	2.74	2.86	2.86	2.87
Min SE Hold		t_h	0.46	0.46	0.46	0.46
Min SCE Setup		t_{su}	1.69	1.74	1.86	1.99
Min SCE Hold		t_h	2.80	2.92	2.93	2.93

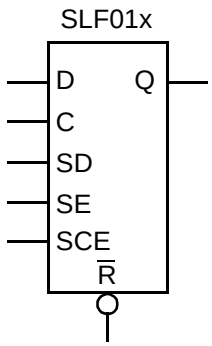
Logic Schematic



Description

SLF01x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. RESET is asynchronous and active low.

Logic Symbol



Truth Table

RN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF01x *inst_name* (Q, C, D, RN, SCE, SD, SE);

VHDL..... *inst_name*: SLF01x port map (Q, C, D, RN, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF011	SLF012	SLF014	SLF016
C	1.1	1.1	1.1	1.1
D	1.0	1.0	1.0	1.1
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3
SCE	1.1	1.1	1.1	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF011	8.2	3.276	19.1
SLF012	8.8	3.481	21.1
SLF014	9.0	3.825	23.1
SLF016	9.0	4.515	28.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
SLF011	From: C To: Q	t_{PLH} t_{PHL}	3.55 4.81	4.17 5.53	5.02 6.14	6.08 6.73	6.99 7.16
	From: D To: Q	t_{PLH} t_{PHL}	3.31 4.40	3.95 5.13	4.80 5.73	5.85 6.30	6.75 6.72
	From: RN To: Q	t_{PLH} t_{PHL}	2.59 2.60	3.35 3.26	4.21 3.88	5.18 4.52	5.96 5.00
	From: SCE To: Q	t_{PLH} t_{PHL}	1.94 1.91	2.71 2.59	3.56 3.22	4.53 3.86	5.30 4.33
	From: SD To: Q	t_{PLH} t_{PHL}	3.27 4.19	4.03 4.77	4.89 5.42	5.86 6.15	6.64 6.73
	From: SE To: Q	t_{PLH} t_{PHL}	3.54 4.66	4.24 5.30	5.10 5.94	6.11 6.62	6.95 7.15
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
SLF012	From: C To: Q	t_{PLH} t_{PHL}	3.31 4.25	4.13 4.86	4.90 5.33	5.53 5.68	6.20 6.03
	From: D To: Q	t_{PLH} t_{PHL}	3.14 3.95	3.97 4.33	4.73 4.81	5.36 5.27	6.03 5.80
	From: RN To: Q	t_{PLH} t_{PHL}	2.73 4.27	3.45 5.24	4.22 6.00	4.90 6.59	5.66 7.18
	From: SCE To: Q	t_{PLH} t_{PHL}	1.78 1.45	2.56 2.02	3.33 2.52	3.98 2.93	4.68 3.35
	From: SD To: Q	t_{PLH} t_{PHL}	3.15 3.75	3.89 4.19	4.66 4.68	5.34 5.11	6.08 5.60
	From: SE To: Q	t_{PLH} t_{PHL}	3.40 4.28	4.11 4.88	4.88 5.34	5.58 5.71	6.34 6.07

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	Number of Equivalent Loads		1	19	38	56	75 (max)
SLF014	From: C To: Q	t_{PLH} t_{PHL}	3.47 4.39	4.18 4.98	4.86 5.38	5.47 5.70	6.10 6.00
	From: D To: Q	t_{PLH} t_{PHL}	3.23 3.92	3.86 4.57	4.63 4.98	5.36 5.32	6.11 5.66
	From: RN To: Q	t_{PLH} t_{PHL}	2.51 4.96	3.34 6.12	4.05 6.73	4.67 7.22	5.28 7.73
	From: SCE To: Q	t_{PLH} t_{PHL}	1.79 1.49	2.61 2.12	3.35 2.60	4.00 2.91	4.66 3.29
	From: SD To: Q	t_{PLH} t_{PHL}	3.18 3.85	3.90 4.42	4.59 4.80	5.23 5.10	5.88 5.39
	From: SE To: Q	t_{PLH} t_{PHL}	3.43 4.37	4.18 4.96	4.84 5.37	5.49 5.71	6.26 6.03
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
SLF016	From: C To: Q	t_{PLH} t_{PHL}	4.71 5.46	5.32 5.63	5.93 5.94	6.52 6.35	7.10 6.83
	From: D To: Q	t_{PLH} t_{PHL}	4.40 4.97	4.89 5.40	5.58 5.70	6.33 5.97	7.12 6.22
	From: RN To: Q	t_{PLH} t_{PHL}	3.70 1.68	4.29 2.17	4.97 2.53	5.67 2.83	6.36 3.11
	From: SCE To: Q	t_{PLH} t_{PHL}	3.30 2.48	3.87 2.97	4.45 3.29	5.04 3.57	5.63 3.83
	From: SD To: Q	t_{PLH} t_{PHL}	4.37 4.84	5.11 5.24	5.72 5.52	6.28 5.77	6.82 5.99
	From: SE To: Q	t_{PLH} t_{PHL}	4.70 5.36	5.48 5.72	6.08 6.02	6.62 6.29	7.11 6.54

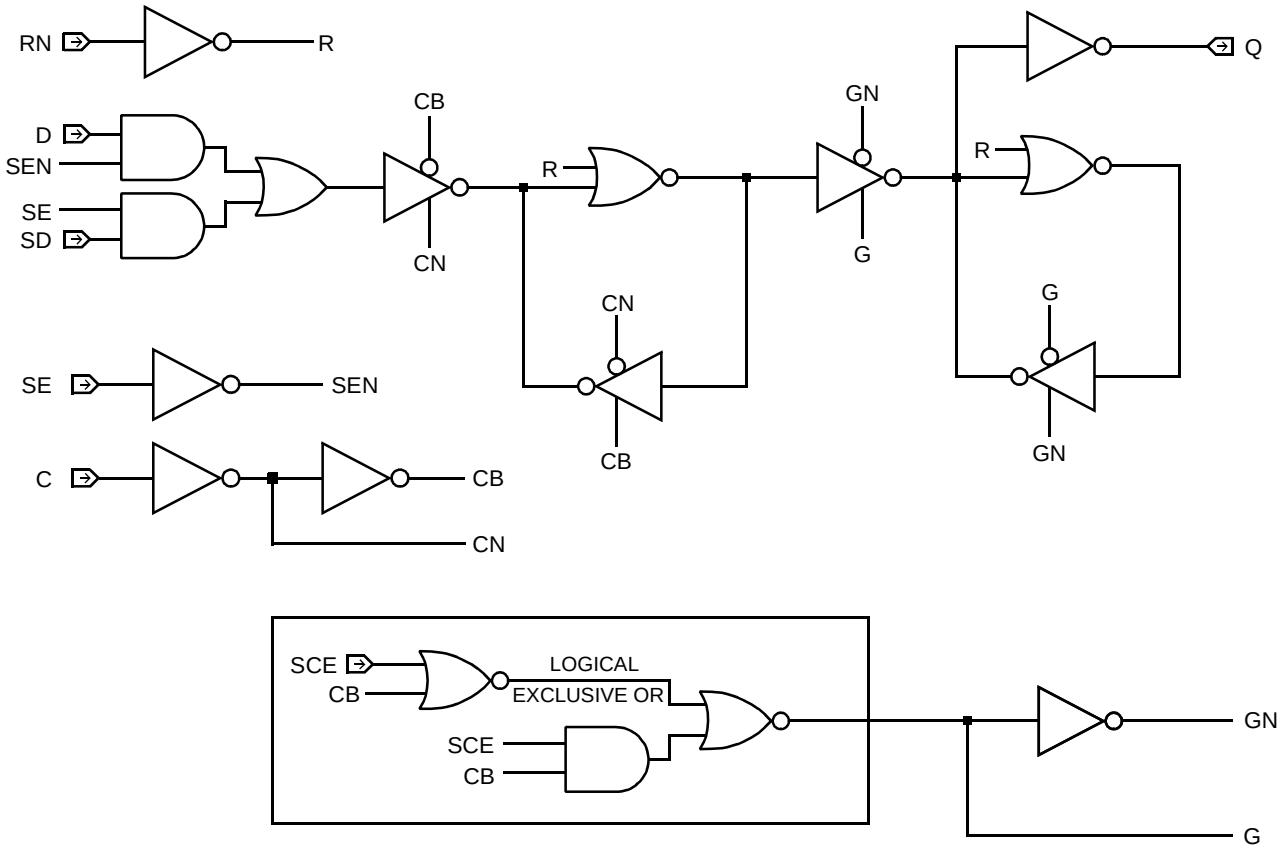
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF011	SLF012	SLF014	SLF016
Min C Width	High	t_w	2.94	2.79	2.92	3.16
Min C Width	Low	t_w	3.22	3.10	3.10	3.22
Min RN Width	Low	t_w	1.91	2.77	2.77	1.92
Min D Setup		t_{su}	2.70	2.70	2.70	2.69
Min D Hold		t_h	0.47	0.46	0.46	0.47
Min SD Setup		t_{su}	2.70	2.70	2.70	2.69
Min SD Hold		t_h	0.47	0.46	0.46	0.47
Min SE Setup		t_{su}	3.05	3.05	3.05	3.05
Min SE Hold		t_h	0.47	0.46	0.46	0.47
Min SCE Setup		t_{su}	2.07	1.96	2.10	2.30
Min SCE Hold		t_h	3.22	3.10	3.10	3.22
Min RN Setup		t_{su}	1.21	1.32	1.32	1.23
Min RN Hold		t_h	1.05	1.59	1.59	1.04

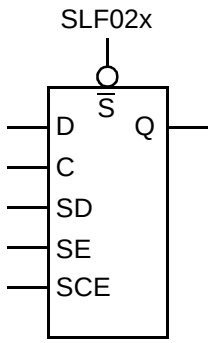
Logic Schematic



Description

SLF02x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET is asynchronous and active low.

Logic Symbol



Truth Table

SN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	H

NC = No Change

HDL Syntax

Verilog ..... SLF02x *inst_name* (Q, C, D, SCE, SD, SE, SN);

VHDL..... *inst_name*:SLF02x port map (Q, C, D, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF021	SLF022	SLF024	SLF026
C	1.1	1.1	1.1	1.1
D	1.1	1.1	1.1	1.1
SD	1.0	1.0	1.0	1.0
SE	2.3	2.3	2.3	2.3
SCE	1.1	1.1	1.1	1.1
SN	2.2	2.2	2.2	2.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF021	7.8	2.912	16.2
SLF022	8.2	3.040	18.2
SLF024	8.5	3.385	20.2
SLF026	8.8	3.914	23.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	5	10	16	21 (max)
SLF021	From: C To: Q	t_{PLH} t_{PHL}	3.08 5.02	3.68 5.73	4.52 6.35	5.59 6.95	6.52 7.40
	From: D To: Q	t_{PLH} t_{PHL}	2.83 4.58	3.58 5.14	4.43 5.79	5.41 6.53	6.20 7.13
	From: SCE To: Q	t_{PLH} t_{PHL}	1.93 1.86	2.61 2.51	3.47 3.15	4.48 3.83	5.33 4.34
	From: SD To: Q	t_{PLH} t_{PHL}	2.82 4.43	3.50 5.00	4.36 5.64	5.38 6.38	6.23 6.98
	From: SE To: Q	t_{PLH} t_{PHL}	3.09 4.92	3.73 5.52	4.57 6.17	5.62 6.88	6.52 7.45
	From: SN To: Q	t_{PLH} t_{PHL}	1.71 2.36	2.42 3.01	3.28 3.75	4.27 4.58	5.09 5.25
	Number of Equivalent Loads		**1**	**10**	**20**	**29**	**39 (max)**
SLF022	From: C To: Q	t_{PLH} t_{PHL}	3.02 4.27	3.68 4.86	4.45 5.33	5.15 5.70	5.94 6.08
	From: D To: Q	t_{PLH} t_{PHL}	2.84 4.00	3.54 4.56	4.31 5.04	4.99 5.43	5.75 5.83
	From: SCE To: Q	t_{PLH} t_{PHL}	1.78 1.47	2.48 2.02	3.25 2.50	3.93 2.88	4.69 3.28
	From: SD To: Q	t_{PLH} t_{PHL}	2.81 3.83	3.56 4.34	4.33 4.83	4.99 5.24	5.70 5.68
	From: SE To: Q	t_{PLH} t_{PHL}	3.07 4.28	3.87 4.79	4.63 5.28	5.27 5.70	5.95 6.13
	From: SN To: Q	t_{PLH} t_{PHL}	2.92 1.88	3.89 2.52	4.73 3.07	5.40 3.51	6.09 3.97

AMI500MXSC 0.5 micron CMOS Standard Cell

	Number of Equivalent Loads		1	19	38	56	75 (max)
SLF024	From: C To: Q	t_{PLH} t_{PHL}	3.07 4.38	3.71 4.93	4.46 5.36	5.19 5.67	5.99 5.93
	From: D To: Q	t_{PLH} t_{PHL}	2.85 3.91	3.61 4.68	4.38 5.17	5.10 5.54	5.85 5.89
	From: SCE To: Q	t_{PLH} t_{PHL}	1.85 1.48	2.59 2.05	3.32 2.48	3.99 2.82	4.68 3.15
	From: SD To: Q	t_{PLH} t_{PHL}	2.78 3.90	3.54 4.44	4.34 4.85	5.06 5.18	5.78 5.51
	From: SE To: Q	t_{PLH} t_{PHL}	3.00 4.37	3.72 4.97	4.48 5.30	5.21 5.54	5.97 5.77
	From: SN To: Q	t_{PLH} t_{PHL}	3.45 1.86	4.42 2.55	5.26 3.07	5.97 3.50	6.64 3.91
	Number of Equivalent Loads		**1**	**28**	**56**	**84**	**112 (max)**
SLF026	From: C To: Q	t_{PLH} t_{PHL}	3.74 5.15	4.37 5.55	4.99 5.82	5.60 6.09	6.19 6.36
	From: D To: Q	t_{PLH} t_{PHL}	3.43 4.84	4.06 5.02	4.74 5.29	5.42 5.60	6.12 5.94
	From: SCE To: Q	t_{PLH} t_{PHL}	2.50 2.44	3.26 2.88	3.92 3.16	4.54 3.47	5.14 3.84
	From: SD To: Q	t_{PLH} t_{PHL}	3.49 4.63	4.19 4.99	4.84 5.28	5.46 5.53	6.06 5.77
	From: SE To: Q	t_{PLH} t_{PHL}	3.83 5.16	4.46 5.43	5.08 5.74	5.72 6.06	6.38 6.39
	From: SN To: Q	t_{PLH} t_{PHL}	1.25 2.57	1.94 3.19	2.63 3.57	3.30 3.90	3.97 4.22

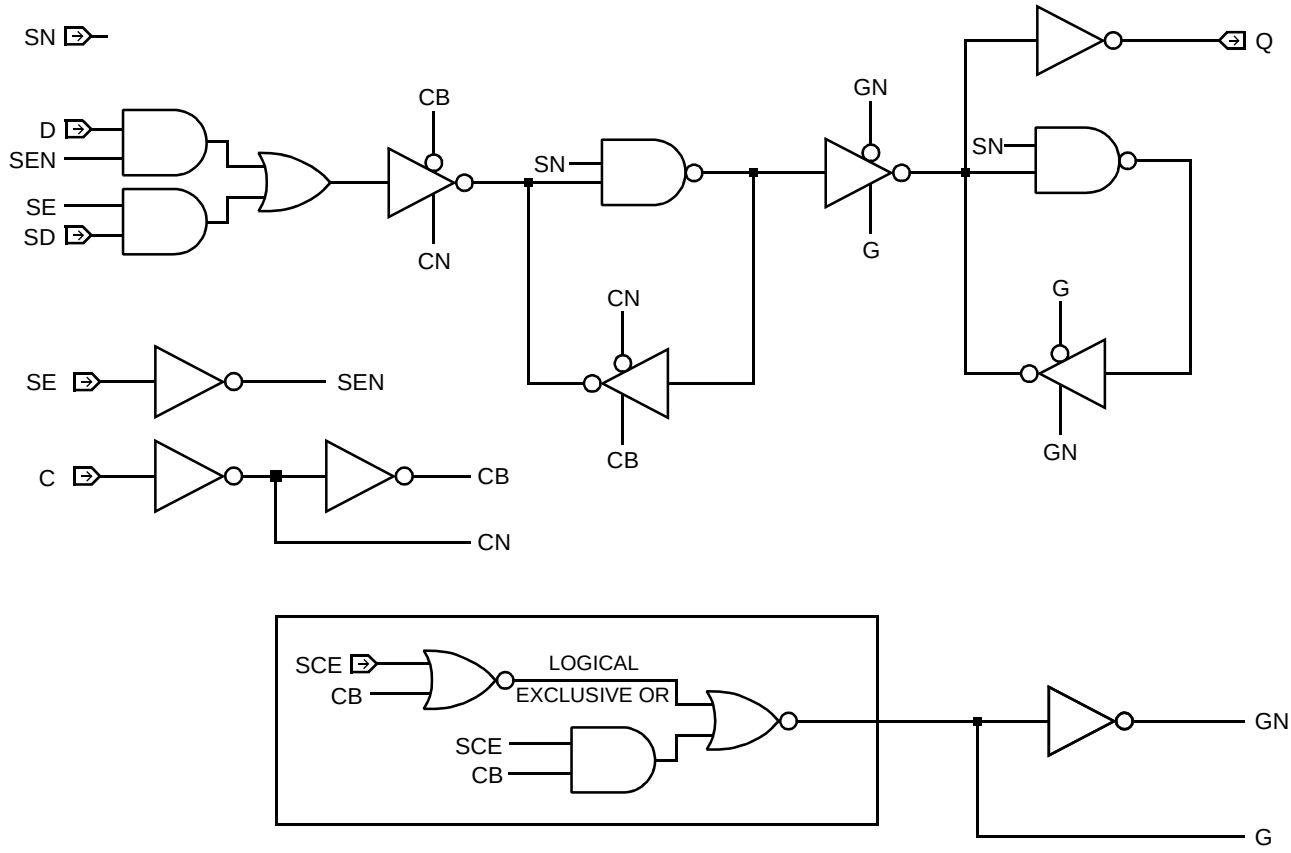
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF021	SLF022	SLF024	SLF026
Min C Width	High	t_w	2.85	2.69	2.80	2.74
Min C Width	Low	t_w	3.41	3.11	3.10	2.98
Min SN Width	Low	t_w	1.25	2.14	2.13	1.95
Min D Setup		t_{su}	2.89	2.71	2.70	2.58
Min D Hold		t_h	0.47	0.46	0.46	0.46
Min SD Setup		t_{su}	2.89	2.71	2.70	2.58
Min SD Hold		t_h	0.47	0.46	0.46	0.46
Min SE Setup		t_{su}	3.24	3.06	3.06	2.93
Min SE Hold		t_h	0.47	0.46	0.46	0.46
Min SCE Setup		t_{su}	2.01	1.86	1.98	1.91
Min SCE Hold		t_h	3.41	3.11	3.10	2.98
Min SN Setup		t_{su}	0.71	0.66	0.67	0.57
Min SN Hold		t_h	1.49	1.91	1.91	1.92

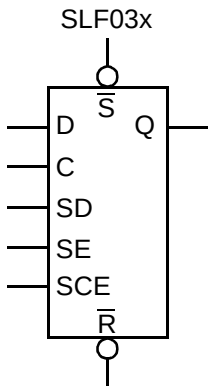
Logic Schematic



Description

SLF03x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET and RESET are asynchronous and active low.

Logic Symbol



Truth Table

RN	SN	C	D	SD	SE	SCE	Q
H	H	↑	H	X	L	L	H
H	H	↑	L	X	L	L	L
H	H	↑	X	H	H	L	H
H	H	↑	X	L	H	L	L
H	H	L	X	X	X	L	NC
H	H	L	H	X	L	H	H
H	H	L	L	X	L	H	L
H	H	L	X	H	H	H	H
H	H	L	X	L	H	H	L
H	H	H	X	X	X	H	NC
H	L	X	X	X	X	X	H
L	X	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF03x *inst_name* (Q, C, D, RN, SCE, SD, SE, SN);

VHDL..... *inst_name*: SLF03x port map (Q, C, D, RN, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF031	SLF032	SLF034	SLF036
C	1.1	1.1	1.1	1.1
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.1
SE	2.3	2.3	2.3	2.3
SCE	1.1	1.1	1.1	1.0
SN	2.3	2.2	2.3	2.3

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF031	8.8	2.905	19.2
SLF032	9.5	3.275	22.9
SLF034	9.8	3.608	24.9
SLF036	10.2	3.978	28.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	10	20	29	39 (max)
SLF031	From: C To: Q	t_{PLH} t_{PHL}	3.61 4.57	5.09 5.97	6.77 7.11	8.29 8.02	10.00 8.94
	From: D To: Q	t_{PLH} t_{PHL}	3.38 4.29	4.97 5.40	6.65 6.58	8.13 7.63	9.74 8.79
	From: RN To: Q	t_{PLH} t_{PHL}	2.79 3.89	4.48 5.48	6.16 6.79	7.58 7.84	9.12 8.91
	From: SCE To: Q	t_{PLH} t_{PHL}	1.90 1.85	3.49 3.10	5.17 4.26	6.64 5.24	8.26 6.30
	From: SD To: Q	t_{PLH} t_{PHL}	3.38 4.10	4.97 5.23	6.65 6.42	8.13 7.46	9.75 8.59
	From: SE To: Q	t_{PLH} t_{PHL}	3.67 4.61	5.12 5.82	6.79 7.00	8.34 8.00	10.07 9.07
	From: SN To: Q	t_{PLH} t_{PHL}	2.47 2.26	4.16 3.72	5.88 5.08	7.36 6.21	8.97 7.41
SLF032	Number of Equivalent Loads		1	10	20	29	39 (max)
	From: C To: Q	t_{PLH} t_{PHL}	3.79 4.49	4.50 4.96	5.28 5.45	5.97 5.88	6.74 6.35
	From: D To: Q	t_{PLH} t_{PHL}	3.58 4.15	4.31 4.67	5.09 5.16	5.77 5.56	6.52 5.99
	From: RN To: Q	t_{PLH} t_{PHL}	2.91 4.39	3.65 5.45	4.43 6.18	5.11 6.72	5.85 7.25
	From: SCE To: Q	t_{PLH} t_{PHL}	1.80 1.50	2.47 2.09	3.24 2.57	3.94 2.94	4.73 3.31
	From: SD To: Q	t_{PLH} t_{PHL}	3.58 4.05	4.23 4.57	5.01 5.06	5.73 5.47	6.54 5.90
	From: SE To: Q	t_{PLH} t_{PHL}	3.82 4.51	4.52 5.11	5.29 5.58	5.99 5.94	6.77 6.31
	From: SN To: Q	t_{PLH} t_{PHL}	3.00 2.07	3.88 2.68	4.74 3.23	5.47 3.69	6.26 4.17

	Number of Equivalent Loads		1	19	38	56	75 (max)
SLF034	From: C To: Q	t_{PLH} t_{PHL}	3.87 4.32	4.58 4.96	5.25 5.46	5.85 5.87	6.45 6.27
	From: D To: Q	t_{PLH} t_{PHL}	3.52 4.12	4.27 4.75	4.96 5.14	5.58 5.45	6.21 5.73
	From: RN To: Q	t_{PLH} t_{PHL}	3.01 5.02	3.80 6.15	4.44 6.91	5.05 7.50	5.76 8.05
	From: SCE To: Q	t_{PLH} t_{PHL}	1.88 1.51	2.58 2.18	3.27 2.62	3.94 2.96	4.69 3.28
	From: SD To: Q	t_{PLH} t_{PHL}	3.64 4.05	4.37 4.63	5.02 5.01	5.64 5.35	6.29 5.77
	From: SE To: Q	t_{PLH} t_{PHL}	3.75 4.58	4.49 5.17	5.19 5.56	5.81 5.87	6.42 6.15
	From: SN To: Q	t_{PLH} t_{PHL}	3.52 2.15	4.45 2.77	5.26 3.15	5.95 3.46	6.64 3.72
SLF036	Number of Equivalent Loads		1	28	56	84	112 (max)
	From: C To: Q	t_{PLH} t_{PHL}	4.06 4.67	4.61 5.42	5.26 5.79	5.96 6.07	6.68 6.31
	From: D To: Q	t_{PLH} t_{PHL}	3.86 4.46	4.55 5.07	5.24 5.47	5.92 5.81	6.59 6.11
	From: RN To: Q	t_{PLH} t_{PHL}	3.16 5.67	4.06 6.85	4.73 7.63	5.33 8.28	5.92 8.86
	From: SCE To: Q	t_{PLH} t_{PHL}	1.93 1.62	2.69 2.36	3.39 2.83	4.06 3.21	4.72 3.54
	From: SD To: Q	t_{PLH} t_{PHL}	3.77 4.34	4.52 4.99	5.21 5.43	5.91 5.78	6.65 6.08
	From: SE To: Q	t_{PLH} t_{PHL}	4.15 4.81	4.97 5.52	5.63 5.88	6.21 6.16	6.76 6.39
	From: SN To: Q	t_{PLH} t_{PHL}	4.15 2.27	5.38 3.14	6.15 3.64	6.77 4.04	7.31 4.38

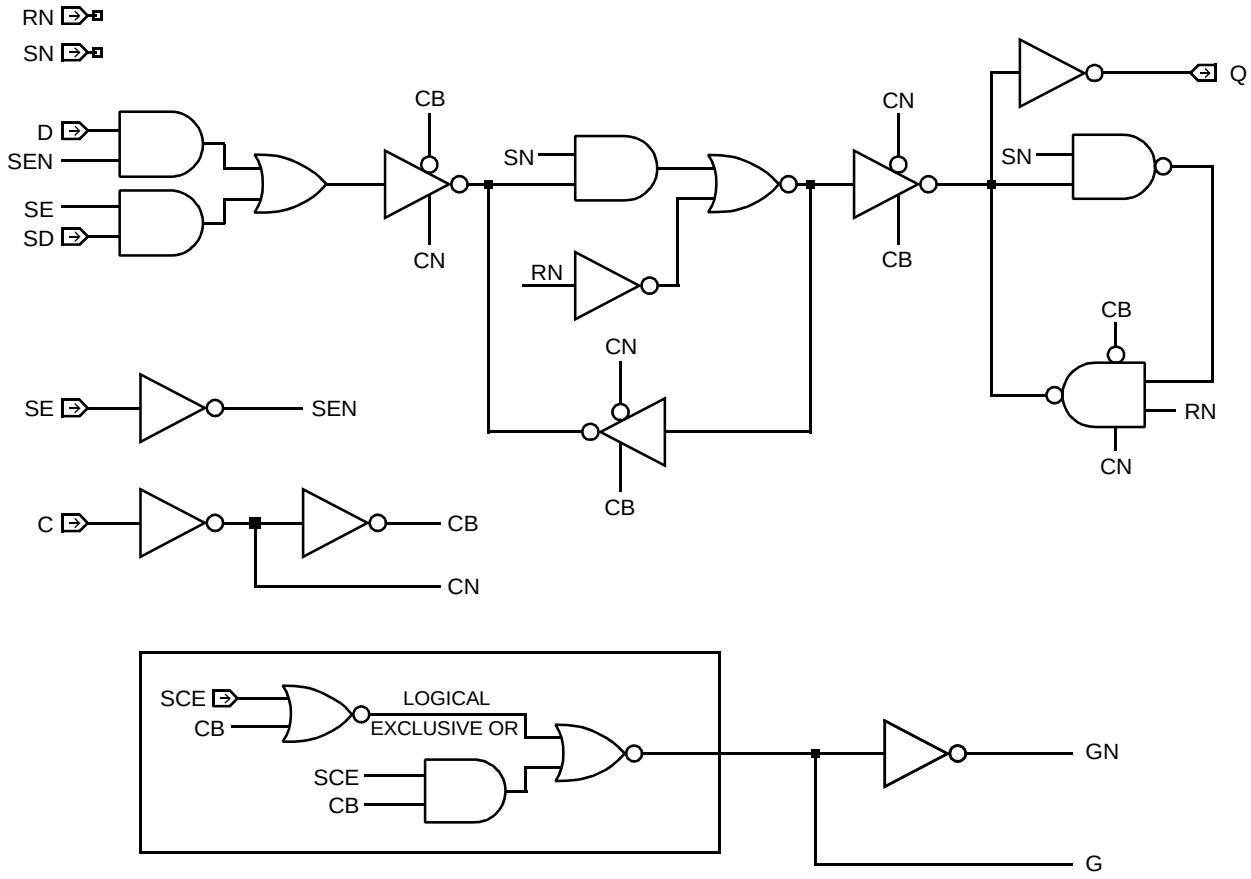
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF031	SLF032	SLF034	SLF036
Min C Width	High	t_w	2.89	2.92	3.05	3.13
Min C Width	Low	t_w	3.04	3.26	3.23	3.23
Min RN Width	Low	t_w	2.80	3.01	2.98	3.01
Min SN Width	Low	t_w	1.94	2.17	2.14	2.18
Min D Setup		t_{su}	2.64	2.85	2.83	2.87
Min D Hold		t_h	0.46	0.46	0.46	0.45
Min RN Setup		t_{su}	1.35	1.59	1.57	1.63
Min RN Hold		t_h	1.59	1.63	1.61	1.60
Min SCE Setup		t_{su}	2.06	2.09	2.22	2.34
Min SCE Hold		t_h	3.04	3.26	3.23	3.23
Min SD Setup		t_{su}	2.64	2.85	2.83	2.87
Min SD Hold		t_h	0.46	0.46	0.46	0.45
Min SE Setup		t_{su}	2.99	3.20	3.17	3.22
Min SE Hold		t_h	0.46	0.46	0.46	0.45
Min SN Setup		t_{su}	0.68	0.81	0.80	0.83
Min SN Hold		t_h	1.91	1.93	1.92	1.88

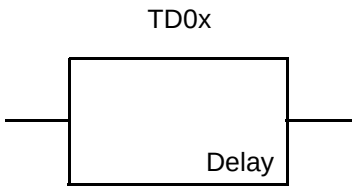
Logic Schematic



Description

TD0x is a family of non-inverting time delays.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... TD0x *inst_name* (Q, A);

VHDL..... *inst_name*: TD0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	TD02	TD03	TD08
A	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
TD02	4.2	1.481	12.1
TD03	6.0	1.740	16.1
TD08	11.8	3.573	40.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

TD02	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	5.843 5.642	6.627 6.079	7.382 6.514	8.021 6.888	8.703 7.290
TD03	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	8.919 8.840	10.661 9.917	12.265 10.621	13.595 11.127	14.996 11.613
TD08	**Number of Equivalent Loads**		**1**	**10**	**20**	**29**	**39 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	24.373 24.800	25.345 24.883	25.669 25.168	25.849 25.614	25.996 26.333

Delay will vary with input conditions. See page 2-15 for interconnect estimates.