BURR-BROWN®

ADS602

12-Bit 1MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW LINEARITY ERROR
- SAMPLE RATE: 1MHz
- INPUT RANGES: ±5V, 0V to +10V
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- 32-PIN CERAMIC DIP PACKAGE

APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- HIGH-SPEED DATA ACQUISITION SYSTEMS
- MEDICAL INSTRUMENTATION
- ANALYTICAL INSTRUMENTATION
- TEST AND IMAGING SYSTEMS
- WAVEFORM ANALYZERS

DESCRIPTION

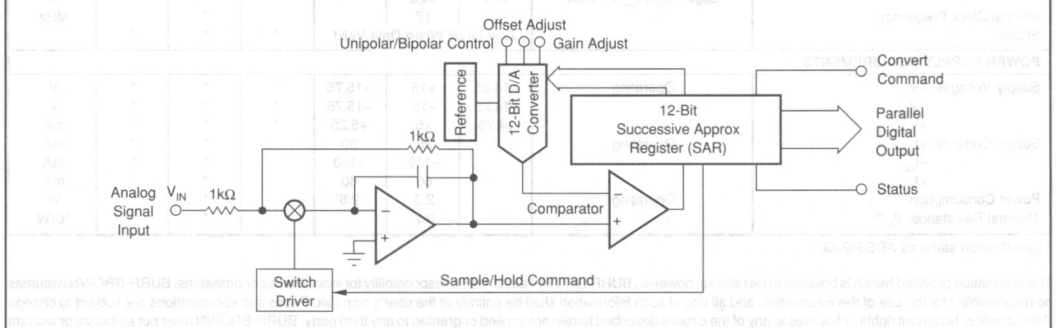
The ADS602 is a high-speed successive approximation analog-to-digital converter with internal sample/hold amplifier. This unique design utilizes a bipolar technology with on-chip thin film resistors to preserve analog accuracy and a high-speed CMOS chip to perform digital logic control. Outstanding linearity, noise, and dynamic range are achieved by this converter design. The ADS602 is thoroughly tested for dynamic performance.

The ADS602 is complete with internal reference, clock, and comparator and is packaged in a 32-pin ceramic DIP. Sample rate is set at the factory to 1MHz. Performance is guaranteed with no missing codes over the input voltage, power supply, and operating temperature range. The gain and offset errors are laser trimmed to specification. Optionally they may be externally adjusted to zero.

The user can switch between unipolar (0V to +10V) and bipolar (±5V) operation through one digital logic level input.

Output codes are available in complementary binary for unipolar inputs and complementary offset binary for bipolar inputs.

All digital input and output are TTL-compatible. Power supply requirements are ±15V and +5V.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, 1MHz sampling rate, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADS602JG MIN	ADS602JG TYP	ADS602JG MAX	ADS602KG MIN	ADS602KG TYP	ADS602KG MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG CHARACTERISTICS								
INPUTS								
Voltage Ranges: Bipolar	Full Scale (FSR) (1, 2)	–5		+5	*		*	V
Unipolar	Full Scale (FSR) (1, 2)	0		+10	*		*	V
Input Resistance			1			*		kΩ
Input Capacitance			5	10		*	*	pF
TRANSFER CHARACTERISTICS								
STATIC ACCURACY								
Gain Error (3, 4)			±0.2	±0.3		±0.1	±0.2	% of FSR
Input Offset Error (3, 4): Unipolar			±0.1	±0.8		*	±0.4	% of FSR
Bipolar			±0.1	±0.6		*	±0.4	% of FSR
Integral Linearity Error			1.2	1.5		0.9	1.25	LSB
Differential Linearity Error			1.2	1.5		0.9	1.25	LSB
No Missing Codes			Guaranteed			*		
Power Supply Rejection of Offset and Gain	$\Delta \pm V_{CC} = \pm 10\%$		±0.0036	0.5		*	*	%FSR/%V_{CC}
	$\Delta \pm V_{DD} = \pm 10\%$		±0.001	0.5		*	*	%FSR/%V_{DD}
CONVERSION CHARACTERISTICS								
Sample Rate	Without User Adjustment	DC		1M	*	*	*	samples/s
Power Supply Rejection of Conversion Time	$\Delta + V_{DD} = \pm 5\%$		±1			*		ns/%V_{DD}
DYNAMIC CHARACTERISTICS (The sampling frequency [f_S] = 1MHz and the input signal level = –0.5dB, unless otherwise stated.)								
Differential Linearity Error(5)	f_C = 480kHz, 68% of All Codes		0.35			0.25		LSB
	99% of All Codes		0.6			0.5		LSB
	100% of All Codes		1.2			0.9	1.25	LSB
Spurious Free Dynamic Range	f_C = 10kHz		–74			–86	–76	dB
	f_C = 480kHz		–68			–73	–70	dB
Total Harmonic Distortion(6)	f_C = 10kHz		–79			–83	–75	dBc
	f_C = 480kHz		–70			–72	–70	dBc
Two-Tone Intermodulation Distortion (6, 7)	f_C = 90kHz and 110kHz (–6.5dB)		–77			*		dBc
Signal-to-Noise and Distortion	f_C = 10kHz		71		70	72		dB
(SINAD) Ratio	f_C = 480kHz		63		64	67		dB
Signal-to-Noise Ratio (SNR)	f_C = 10kHz		71		70	73		dB
	f_C = 480kHz		67		67	69		dB
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		16			*		MHz
Full Power	0dB Input		4			*		MHz
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			–150			*	µA
Convert Command			High Level When Converting		*	*	*	
OUTPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Bits 1 through 12, Status	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I_{OH} = –1mA	+2.7	+4.9		*	*		V
Internal Clock Frequency			17			*		MHz
Status			Low Level When Data Valid		*	*	*	
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$–V_{CC}$		–14.25	–15	–15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	mA
Supply Currents: $+I_{CC}$	Operating		26	30		*	*	mA
$–I_{CC}$			–110	–140		*	*	mA
$+I_{DD}$			60	80		*	*	mA
Power Consumption	Operating		2.3	2.8		*	*	W
Thermal Resistance, θ_{JC}(8)			8.7			*		°C/W

* Specification same as ADS602JG.

SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE SPECIFICATIONS)

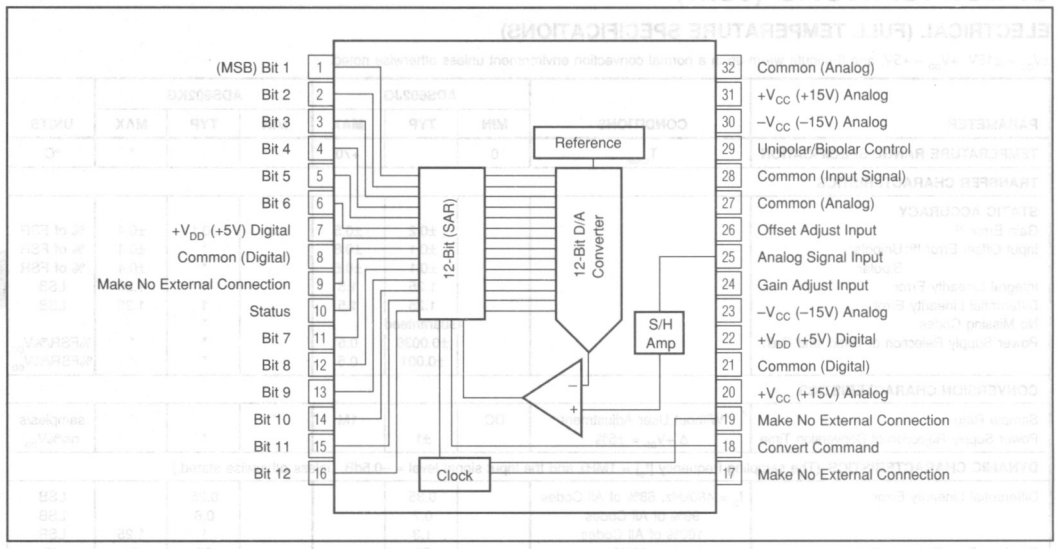
$\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADS602JG MIN	ADS602JG TYP	ADS602JG MAX	ADS602KG MIN	ADS602KG TYP	ADS602KG MAX	UNITS
TEMPERATURE RANGE SPECIFICATION	T_{CASE}	0		+70	*		*	°C
TRANSFER CHARACTERISTICS								
STATIC ACCURACY								
Gain Error (4)			±0.2	±0.5		±0.1	±0.4	% of FSR
Input Offset Error (4): Unipolar			±0.1	±0.8		*	±0.4	% of FSR
Bipolar			±0.1	±0.6		*	±0.4	% of FSR
Integral Linearity Error			1.25	1.5		1	1.25	LSB
Differential Linearity Error			1.25	1.5		1	1.25	LSB
No Missing Codes			Guaranteed			*		
Power Supply Rejection of Offset and Gain			±0.0036	0.5		*	*	%FSR/%V_{CC}
			±0.001	0.5		*	*	%FSR/%V_{DD}
CONVERSION CHARACTERISTICS								
Sample Rate	Without User Adjustment	DC		1M	*		*	samples/s
Power Supply Rejection of Conversion Time	Δ $+V_{DD}$ = ±5%		±1			*		ns/%V_{DD}
DYNAMIC CHARACTERISTICS (The sampling frequency [f_S] = 1MHz and the input signal level ≈ –0.5dB, unless otherwise stated.)								
Differential Linearity Error	f_C = 480kHz, 68% of All Codes		0.35			0.25		LSB
	99% of All Codes		0.7			0.6		LSB
	100% of All Codes		1.3			1	1.25	LSB
Spurious Free Dynamic Range	f_C = 10kHz		73			85	71	dB
	f_C = 480kHz		62			65		dB
Total Harmonic Distortion	f_C = 10kHz		–81			–83	–70	dBc
	f_C = 480kHz		–63			–65		dBc
Two-Tone Intermodulation Distortion (7)	f_C = 90kHz and 110kHz (–6.5dB)		–77			–79		dBc
Signal-to-Noise and Distortion	f_C = 10kHz		71		68	70		dB
(SINAD) Ratio	f_C = 480kHz		63			64		dB
Signal-to-Noise Ratio (SNR)	f_C = 10kHz		71		70	73		dB
	f_C = 480kHz		67		67	69		dB
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		16			*		MHz
Full Power	0dB		4			*		MHz
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			–150			*	µA
Convert Command			High Level When Converting		*	*	*	
OUTPUT								
Logic Family			TTL-Compatible CMOS		*	*	*	
Bits 1 through 12, Status	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I_{OH} = –1mA	+2.7	+4.9		*	*		V
Internal Clock Frequency			17			*		MHz
Status			Low Level When Data Valid		*	*	*	
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		–14.25	–15	–15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	mA
Supply Currents: $+I_{CC}$	Operating		26	30		*	*	mA
$-I_{CC}$			–110	–140		*	*	mA
$+I_{DD}$			60	80		*	*	mA
Power Consumption	Operating		2.3	2.8		*	*	W
Thermal Resistance, θ_{JC} (8)			8.7			*		°C/W

* Specification same as ADS602JG.

NOTES: (1) Over or under range on the analog input results in constant maximum or minimum digital output. (2) FSR = Full Scale Range. (3) Adjustable to zero. (4) If gain and offset adjust pins are not used, they should be grounded. (5) See Typical Performance Curves. (6) dBc = level referred to carrier input signal ≈ –0.5dB of full scale; f_C = input frequency, f_S = sampling frequency. (7) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (≈0dB), the intermodulation products will be 6dB lower. (8) Temperature ranges refer to case temperature. Thermal resistance was measured on a small (5" diameter) handwired circuit board, with the test device in a zero-insertion-force socket. Thermal resistance will be lower if the ADS602 is soldered into the PC board, a ground plane is used directly underneath the package, multiple PC board layers are used, or forced air cooling is employed. Use heat sinking if necessary to keep the case at specified and operating temperatures.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$+V_{DD}$	+7V
Digital Inputs	+5.5V
Analog Inputs	$\pm V_{CC}$
Case Temperature	+125°C
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C

Stresses above these ratings may permanently damage the device.

ORDERING INFORMATION

ADS602 ( ) G

Basic Model Number

Performance Grade Code
J, K: 0°C to +70°C Case Temperature

Package Code
G: Ceramic Bottom Braze

PACKAGE INFORMATION[1]

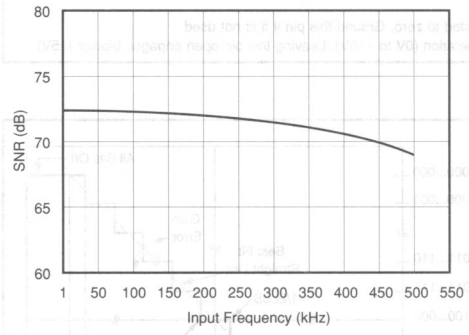
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS602JG	32-Pin Ceramic	153

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

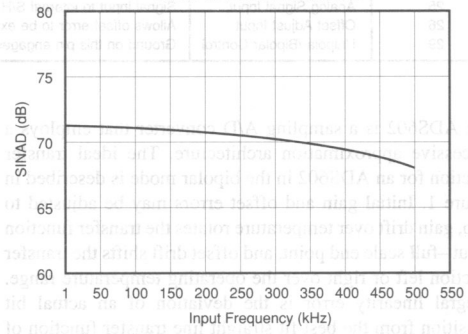
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, 1MHz sampling rate, 6-minute warmup, and T_C = +25°C unless otherwise noted.

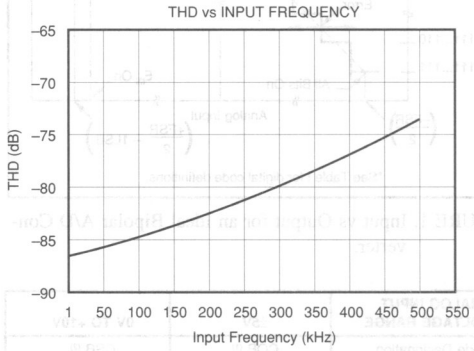
SNR vs INPUT FREQUENCY



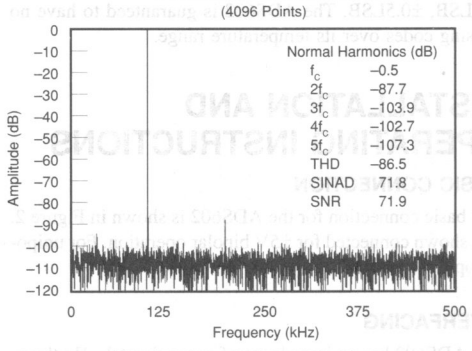
SINAD vs INPUT FREQUENCY



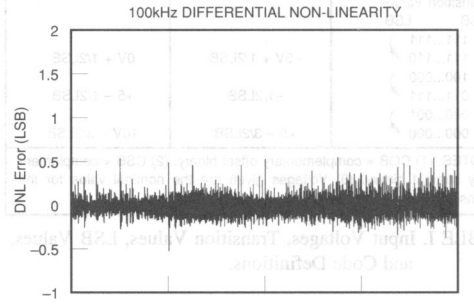
THD vs INPUT FREQUENCY



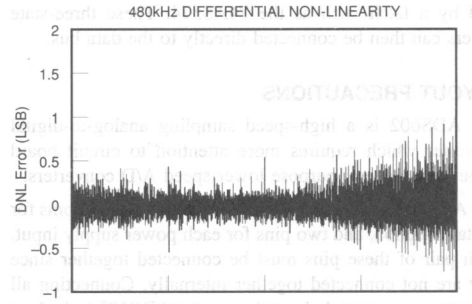
100kHz HARMONIC DISTORTION
(4096 Points)



100kHz DIFFERENTIAL NON-LINEARITY



480kHz DIFFERENTIAL NON-LINEARITY



PIN DEFINITIONS

PIN NUMBER	DESIGNATION	DESCRIPTION
1-6 and 11-16	Bit 1 to Bit 12	12-bit parallel output data.
10	Status	Conversion status strobe is high during data conversion, low when parallel data is valid.
18	Convert Command	High transition starts conversion, and should remain high during conversion. Low will reset clock and SAR logic. Rising edge may be used to latch data from previous conversion.
24	Gain Adjust Input	Allows gain error to be externally adjusted to zero. Ground this pin if it is not used.
25	Analog Signal Input	Signal input to internal S/H amplifier.
26	Offset Adjust Input	Allows offset error to be externally adjusted to zero. Ground this pin if it is not used.
29	Unipolar/Bipolar Control	Ground on this pin engages unipolar operation (0V to +10V). Leaving this pin open engages bipolar (±5V).

The ADS602 is a sampling A/D converter that employs a successive approximation architecture. The ideal transfer function for an ADS602 in the bipolar mode is described in Figure 1. Initial gain and offset errors may be adjusted to zero, gain drift over temperature rotates the transfer function about –full scale end point, and offset drift shifts the transfer function left or right over the operating temperature range. Integral linearity error is the deviation of an actual bit transition from the best fit straight line transfer function of the converter. A differential linearity error of 0.012% means that the width of each bit step over the range of the converter is 1LSB, ±0.5LSB. The ADS602 is guaranteed to have no missing codes over its temperature range.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection for the ADS602 is shown in Figure 2. It is shown connected for ±5V bipolar operation. For unipolar operation, pin 29 should be grounded.

INTERFACING

The ADS602 has an impedance of approximately 1k; therefore, to maintain gain accuracy it must be driven from a low impedance source. The digital output lines should be buffered by a latch such as the 74AS574. These three-state drivers can then be connected directly to the data bus.

LAYOUT PRECAUTIONS

The ADS602 is a high-speed sampling analog-to-digital converter which requires more attention to circuit board layout than general purpose lower speed A/D converters.

The ADS602 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins must be connected together since they are not connected together internally. Connecting all commons to a ground plane close to the ADS602 is the best method to maximize performance. The ground plane minimizes noise and provides additional heat dissipation.

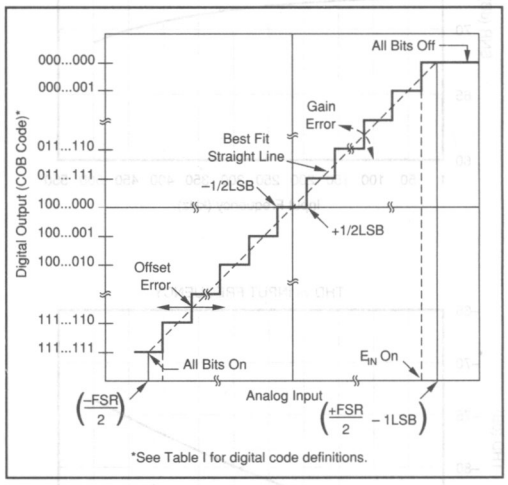


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

ANALOG INPUT VOLTAGE RANGE	±5V	0V TO +10V
Code Designation	COB (1)	CSB (2)
One Least Significant Bit (LSB)	2.44mV	2.44mV
Transition Values MSB LSB (3)		
111...111 / 111...110	–5V + 1/2LSB	0V + 1/2LSB
100...000 / 011...111	–1/2LSB	+5 – 1/2LSB
000...001 / 000...000	+5 – 3/2LSB	10V – 3/2LSB

NOTES: (1) COB = complementary offset binary. (2) CSB = complementary straight binary. (3) Voltages given are the nominal value for the transition from the next code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

POWER SUPPLY DECOUPLING AND POWER SUPPLY SENSITIVITY

The +15V and +5V power supply pins should be bypassed with a 10µF tantalum capacitor as shown in Figure 2. Pin 30 requires bypassing with a 150µF tantalum capacitor. These capacitors should be located close to the ADS602 supply pins. Ceramic 0.01µF bypass capacitors have been provided internally for more effective bypassing and need not be added externally.

Changes in the DC power supply voltages will affect accuracy. Regulated power supplies with 1% or less ripple are recommended for use with the ADS602. Power supply decoupling helps to keep ripple low.

POWER DISSIPATION

The ADS602 dissipates approximately 2.3W. The package has a junction-to-case thermal resistance (θ_{JC}) of 8.7°C/W and a case-to-ambient thermal resistance (θ_{CA}) of 13.7°C/W in a normal convection environment.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and offset errors may be trimmed to zero using external trim potentiometers as shown in Figure 2. Multiturn potentiometers with 100ppm/°C temperature coefficient are recommended for minimum drift. If the gain adjust or offset adjust pins are not used, they must be grounded to meet the specified accuracy.

DYNAMIC PERFORMANCE TESTING

The ADS602 is a high performance sampling A/D converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on important dynamic performance parameters.

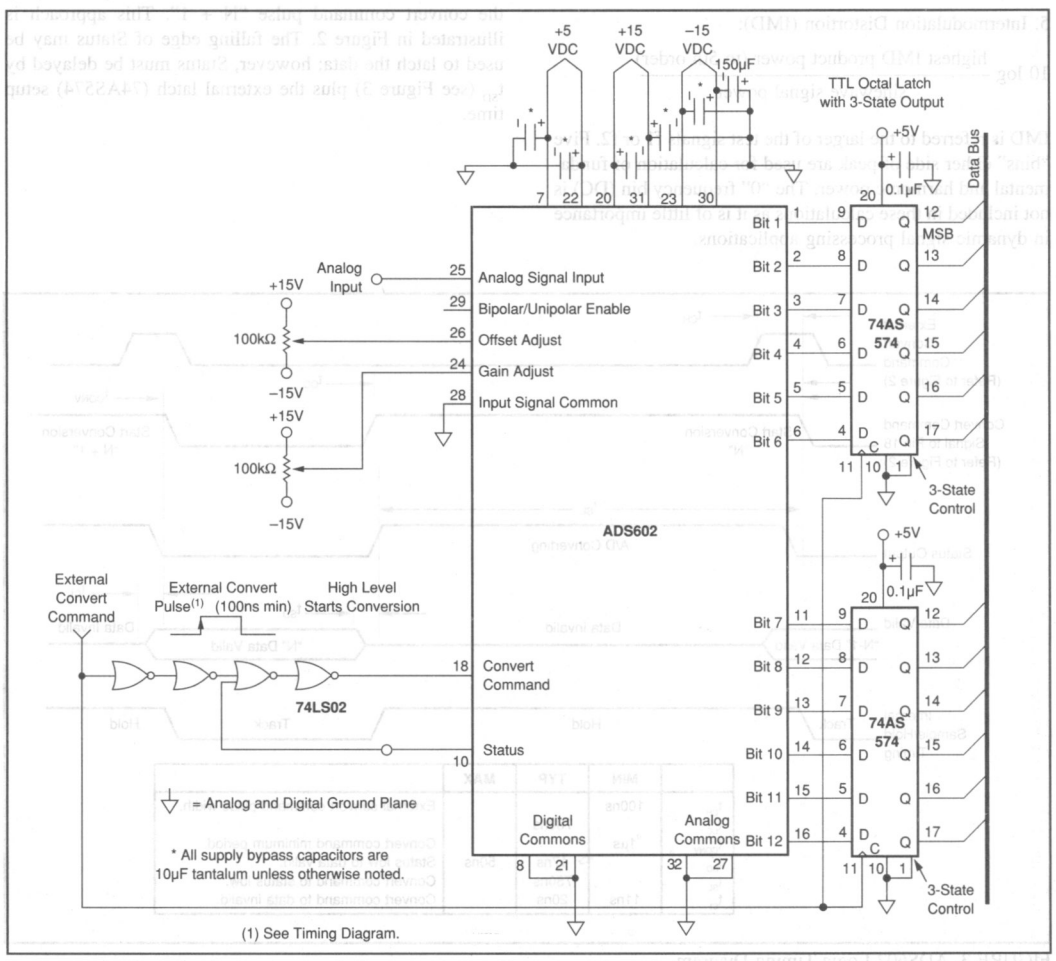


FIGURE 2. ADS602 Application Circuit.

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10 \log \frac{\text{sinewave signal power}}{\text{noise + harmonic power (first 9 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{sinewave signal power}}{\text{noise power}}$$

3. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{harmonic power (first 9 harmonics)}}{\text{sinewave signal power}}$$

4. Spurious Free Dynamic Range (SFDR):

$$10 \log \frac{\text{largest harmonic power}}{\text{sinewave signal power}}$$

5. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{highest IMD product power (to 5th order)}}{\text{sinewave signal power}}$$

IMD is referred to the larger of the test signals f1 or f2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

TIMING CONSIDERATIONS

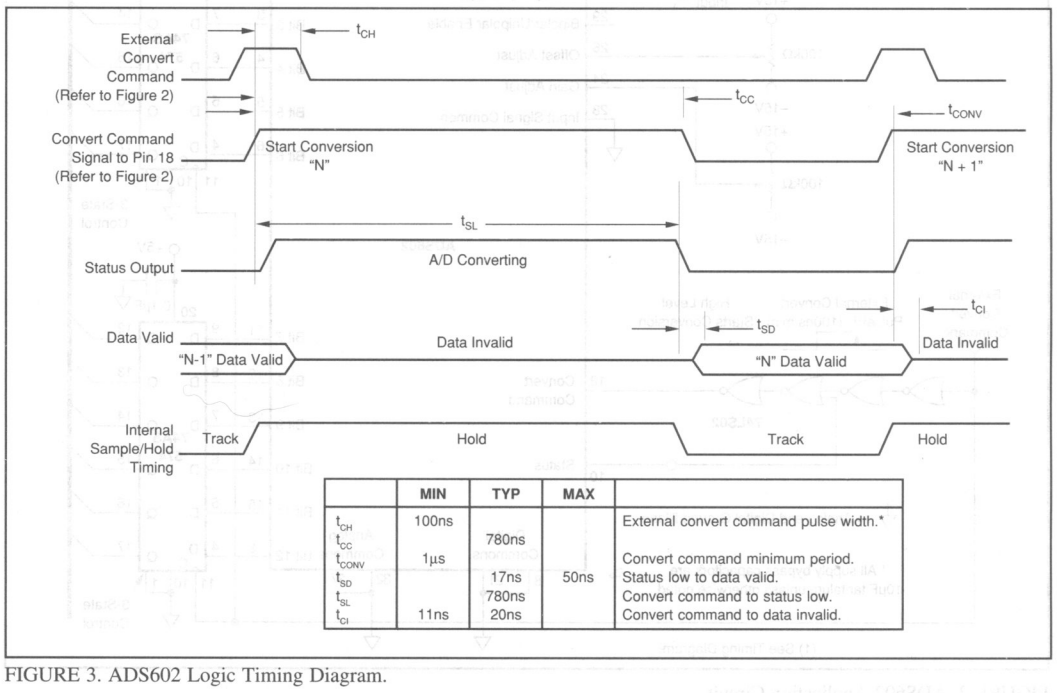
In addition to the timing details in Figure 3, the following list contains some important timing considerations for the ADS602:

1. When power is first applied, the convert command should be held low or below the +5V supply to prevent latch up.

2. The rising edge of the convert command pulse initiates a conversion. This convert command should remain high until the Status falls (i.e., the internal ADC is finished converting). A simple circuit that provides the correct convert command (pin 18) pulse length, is shown in Figure 2.

3. The ADS602 goes directly into the "hold" mode when a convert command signal is given. The Status falls approximately 780ns later, indicating that the conversion is complete. At this time, the sample-hold (internal to the ADS602) enters the track mode. The ADS602 will remain in the track mode until the next convert command is given.

4. The data from conversion "N" can be latched directly by the convert command pulse "N + 1". This approach is illustrated in Figure 2. The falling edge of Status may be used to latch the data; however, Status must be delayed by t_{SD} (see Figure 3) plus the external latch (74AS574) setup time.



	MIN	TYP	MAX	
t_{CH}	100ns			External convert command pulse width.*
t_{CC}		780ns		
t_{CONV}	1µs			Convert command minimum period.
t_{SD}		17ns	50ns	Status low to data valid.
t_{SL}		780ns		Convert command to status low.
t_{CI}	11ns	20ns		Convert command to data invalid.

FIGURE 3. ADS602 Logic Timing Diagram.