ADC12DJ3200 6.4-GSPS Single Channel or 3.2-GSPS Dual Channel, 12-bit, RF-Sampling Analog-to-Digital Converter (ADC)

1 Features

- ADC Core:
  - 12-bit Resolution
  - Up to 6.4 GSPS in single channel mode
  - Up to 3.2 GSPS in dual channel mode
- Buffered Analog Inputs with V_{CMI} of 0 V
  - Analog input bandwidth (-3 dB): 8.0 GHz
  - Usable input frequency range: >10 GHz
  - Full-scale input voltage (V_{FS}, default): 0.8 V_{PP}
- Noise Floor (No signal, V_{FS} = 1.0 V_{PP}):
  - Dual channel mode: -151.8 dBFS/Hz
  - Single channel mode: -154.6 dBFS/Hz
- Noiseless Aperture Delay (T_{AD}) Adjustment
  - Precise sampling control: 19-fs step
  - Temperature and voltage invariant delays
- Easy-to-use Synchronization Features
  - Automatic SYSREF timing calibration
  - Timestamp for sample marking
- JESD204B Serial Data Interface
  - Supports subclass 0 and 1
  - Maximum lane rate: 12.8 Gbps
  - Up to 16 lanes allows reduced lane rate
- Digital Down-Converters in Dual Channel Mode
  - Real output: DDC bypass or 2x decimation
  - Complex output: 4x, 8x or 16x decimation
  - Four independent 32-bit NCOs per DDC
- Power consumption: 3.0 W
- Power Supplies: 1.1 V, 1.9 V

2 Applications

- Communications testers (802.11ad, 5G)
- Satellite communications (SATCOM)
- Phased array radar, SIGINT and ELINT
- Synthetic aperture radar (SAR)
- Time-of-flight and LIDAR distance measurement
- Oscilloscopes and wideband digitizers
- RF sampling software defined radio (SDR)

3 Description

ADC12DJ3200 is an RF-sampling giga-sample ADC that can directly sample input frequencies from DC to above 10 GHz. In dual channel mode, ADC12DJ3200 can sample up to 3200-MSPS and in single channel mode up to 6400-MSPS. Programmable tradeoffs in channel count (dual channel mode) and Nyquist bandwidth (single channel mode) allow development of flexible hardware that meets the needs of both high channel count or wide instantaneous signal bandwidth applications. Full power input bandwidth (-3 dB) of 8.0 GHz, with usable frequencies exceeding the -3 dB point in both dual and single channel modes, allows direct RF sampling of L-band, S-band, C-band and X-band for frequency agile systems.

ADC12DJ3200 uses a high speed JESD204B output interface with up to 16 serialized lanes and subclass-1 compliance for deterministic latency and multi-device synchronization. The serial output lanes support up to 12.8 Gbps and can be configured to trade-off bit rate and number of lanes. Innovative synchronization features, including noiseless aperture delay (T_{AD}) adjustment and SYSREF windowing, simplify system design for phased array radar and MIMO communications. Optional digital down converters (DDCs) in dual channel mode allow for reduction in interface rate (real and complex decimation modes) and digital mixing of the signal (complex decimation modes only).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC12DJ3200	FCBGA (144)	10.00 mm x 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADC12DJ3200 Measured Input Bandwidth

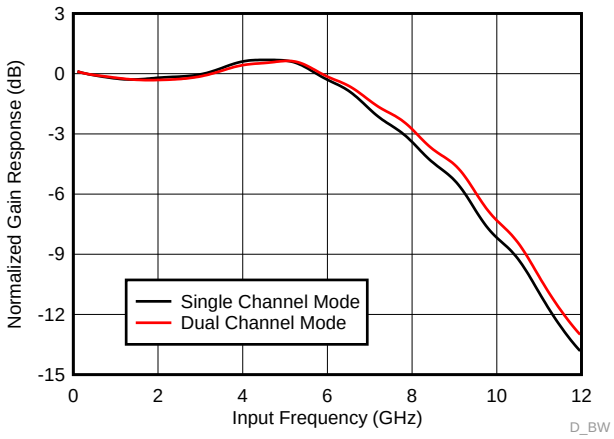


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2017	*	Advance Information release
June 2017	*	Production Data release

5 Pin Configuration and Functions

AAV Package
144-Ball Flip Chip BGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12
A	AGND	AGND	AGND	INA+	INA-	AGND	AGND	DA3+	DA3-	DA2+	DA2-	DGND
B	TMSTP+	AGND	AGND	AGND	AGND	AGND	AGND	DA7+	DA7-	DA6+	DA6-	DGND
C	TMSTP-	$\overline{\text{SYNCSE}}$	BG	VA19	VA11	AGND	NCOA0	ORA0	VD11	VD11	DA5+	DA1+
D	AGND	VA11	VA11	VA19	VA11	AGND	NCOA1	ORA1	DGND	DGND	DA5-	DA1-
E	AGND	VA19	VA19	VA19	VA11	AGND	CALTRIG	$\overline{\text{SCS}}$	VD11	VD11	DA4+	DA0+
F	CLK+	AGND	AGND	VA19	VA11	AGND	CALSTAT	SCLK	DGND	DGND	DA4-	DA0-
G	CLK-	AGND	AGND	VA19	VA11	AGND	VD11	SDI	DGND	DGND	DB4-	DB0-
H	AGND	VA19	VA19	VA19	VA11	AGND	VD11	SDO	VD11	VD11	DB4+	DB0+
J	AGND	VA11	VA11	VA19	VA11	AGND	NCOB1	ORB1	DGND	DGND	DB5-	DB1-
K	SYSREF+	TDIODE+	TDIODE-	VA19	VA11	PD	NCOB0	ORB0	VD11	VD11	DB5+	DB1+
L	SYSREF-	AGND	AGND	AGND	AGND	AGND	AGND	DB7+	DB7-	DB6+	DB6-	DGND
M	AGND	AGND	AGND	INB+	INB-	AGND	AGND	DB3+	DB3-	DB2+	DB2-	DGND

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	A1, A2, A3, A6, A7, B2, B3, B4, B5, B6, B7, C6, D1, D6, E1, E6, F2, F3, F6, G2, G3, G6, H1, H6, J1, J6, L2, L3, L4, L5, L6, L7, M1, M2, M3, M6, M7	—	Analog supply ground. AGND and DGND should be tied to a common ground plane (GND) on circuit board.
DGND	A12, B12, D9, D10, F9, F10, G9, G10, J9, J10, L12, M12	—	Digital supply ground. AGND and DGND should be tied to a common ground plane (GND) on circuit board.
BG	C3	O	Bandgap voltage output. This pin is capable of sourcing only small currents and driving limited capacitive loads as specified in Recommended Operating Conditions. This pin can be left disconnected if not used.
CALSTAT	F7	O	Foreground calibration status output or device alarm output. Functionality is programmed through CAL_STATUS_SEL. This pin can be left disconnected if not used.
CALTRIG	E7	I	Foreground calibration trigger input. This pin is only used if hardware calibration triggering is selected in CAL_TRIG_EN, otherwise software triggering is performed using CAL_SOFT_TRIG. This pin should be tied to GND if not used.
CLK+	F1	I	Device (sampling) clock positive input. The clock signal is strongly recommended to be AC coupled to this input for best performance. In single channel mode, the analog input signal is sampled on both rising and falling edges. In dual channel mode, the analog signal is sampled on the rising edge. This differential input has an internal untrimmed 100-Ω differential termination and is self-biased to the optimal input common mode voltage as long as DEVCLK_LVPECL_EN is set to 0.
CLK-	G1	I	Device (sampling) clock negative input. Strongly recommended to use AC coupling for best performance.
DA0+	E12	O	High-speed serialized-data output for channel A, lane 0, positive connection. This differential output must be AC-coupled and should always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA0-	F12	O	High-speed serialized-data output for channel A, lane 0, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA1+	C12	O	High-speed serialized-data output for channel A, lane 1, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA1-	D12	O	High-speed serialized-data output for channel A, lane 1, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA2+	A10	O	High-speed serialized-data output for channel A, lane 2, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA2-	A11	O	High-speed serialized-data output for channel A, lane 2, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA3+	A8	O	High-speed serialized-data output for channel A, lane 3, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DA3-	A9	O	High-speed serialized-data output for channel A, lane 3, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA4+	E11	O	High-speed serialized-data output for channel A, lane 4, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA4-	F11	O	High-speed serialized-data output for channel A, lane 4, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA5+	C11	O	High-speed serialized-data output for channel A, lane 5, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA5-	D11	O	High-speed serialized-data output for channel A, lane 5, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA6+	B10	O	High-speed serialized-data output for channel A, lane 6, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA6-	B11	O	High-speed serialized-data output for channel A, lane 6, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA7+	B8	O	High-speed serialized-data output for channel A, lane 7, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DA7-	B9	O	High-speed serialized-data output for channel A, lane 7, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB0+	H12	O	High-speed serialized-data output for channel B, lane 0, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB0-	G12	O	High-speed serialized-data output for channel B, lane 0, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB1+	K12	O	High-speed serialized-data output for channel B, lane 1, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB1-	J12	O	High-speed serialized-data output for channel B, lane 1, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB2+	M10	O	High-speed serialized-data output for channel B, lane 2, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB2-	M11	O	High-speed serialized-data output for channel B, lane 2, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB3+	M8	O	High-speed serialized-data output for channel B, lane 3, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB3-	M9	O	High-speed serialized-data output for channel B, lane 3, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DB4+	H11	O	High-speed serialized-data output for channel B, lane 4, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB4-	G11	O	High-speed serialized-data output for channel B, lane 4, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB5+	K11	O	High-speed serialized-data output for channel B, lane 5, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB5-	J11	O	High-speed serialized-data output for channel B, lane 5, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB6+	L10	O	High-speed serialized-data output for channel B, lane 6, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB6-	L11	O	High-speed serialized-data output for channel B, lane 6, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB7+	L8	O	High-speed serialized-data output for channel B, lane 7, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
DB7-	L9	O	High-speed serialized-data output for channel B, lane 7, negative connection. This pin can be left disconnected if not used. See note beneath Recommended Operating Conditions for information regarding reliable serializer operation.
INA+	A4	I	Channel A analog input positive connection. The differential full-scale input voltage is determined by the FS_RANGE_A register (see Full-Scale Voltage (V_{FS}) Adjustment). This input is terminated to ground through a 50-Ω termination resistor. The input common mode voltage should typically be set to 0 V (GND) and should follow the recommendations in Recommended Operating Conditions. This pin can be left disconnected if not used. **NOTE** Use of INA+/– is recommended in single channel mode for optimized performance.
INA-	A5	I	Channel A analog input negative connection. See INA+ for detailed description. This input is terminated to ground through a 50-Ω termination resistor. This pin can be left disconnected if not used.
INB+	M4	I	Channel B analog input positive connection. The differential full-scale input voltage is determined by the FS_RANGE_B register (see Full-Scale Voltage (V_{FS}) Adjustment). This input is terminated to ground through a 50-Ω termination resistor. The input common mode voltage should typically be set to 0 V (GND) and should follow the recommendations in Recommended Operating Conditions. This pin can be left disconnected if not used. Use of INA+/- is recommended for single channel mode for optimized performance.
INB-	M5	I	Channel B analog input negative connection. See INB+ for detailed description. This input is terminated to ground through a 50-Ω termination resistor. This pin can be left disconnected if not used.
NCOA0	C7	I	LSB of NCO selection control for DDC A. NCOA0 and NCOA1 select which NCO, of a possible four NCOs, is used for digital mixing when using a complex output JMODE. The remaining unselected NCOs continue to run to maintain phase coherency and can be swapped in by changing the values of NCOA0 and NCOA1 (when CMODE = 1). This is an asynchronous input. See NCO Fast Frequency Hopping (FFH) and NCO Selection for more information. This pin should be tied to GND if not used.
NCOA1	D7	I	MSB of NCO selection control for DDC A. This pin should be tied to GND if not used.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
NCOB0	K7	I	LSB of NCO selection control for DDC B. NCOB0 and NCOB1 select which NCO, of a possible four NCOs, is used for digital mixing when using a complex output JMODE. The remaining unselected NCOs continue to run to maintain phase coherency and can be swapped in by changing the values of NCOB0 and NCOB1 (when CMODE = 1). This is an asynchronous input. See NCO Fast Frequency Hopping (FFH) and NCO Selection for more information. This pin should be tied to GND if not used.
NCOB1	J7	I	MSB of NCO selection control for DDC B. This pin should be tied to GND if not used.
ORA0	C8	O	Fast over-range detection status for channel A for OVR_T0 threshold. When the analog input exceeds the threshold programmed into OVR_T0, this status indicator will go high. The minimum pulse duration is set by OVR_N. See ADC Over-Range Detection for more information. This pin can be left disconnected if not used.
ORA1	D8	O	Fast over-range detection status for channel A for OVR_T1 threshold. When the analog input exceeds the threshold programmed into OVR_T1, this status indicator will go high. The minimum pulse duration is set by OVR_N. See ADC Over-Range Detection for more information. This pin can be left disconnected if not used.
ORB0	K8	O	Fast over-range detection status for channel B for OVR_T0 threshold. When the analog input exceeds the threshold programmed into OVR_T0, this status indicator will go high. The minimum pulse duration is set by OVR_N. See ADC Over-Range Detection for more information. This pin can be left disconnected if not used.
ORB1	J8	O	Fast over-range detection status for channel B for OVR_T1 threshold. When the analog input exceeds the threshold programmed into OVR_T1, this status indicator will go high. The minimum pulse duration is set by OVR_N. See ADC Over-Range Detection for more information. This pin can be left disconnected if not used.
PD	K6	I	This pin disables all analog circuits and serializer outputs when set high for temperature diode calibration only. This pin should not be used to power down the device for power savings. This pin should be tied to GND during normal operation. See note beneath Recommended Operating Conditions for more information.
SCLK	F8	I	Serial interface clock. This pin functions as the serial-interface clock input which clocks the serial programming data in and out. *Using the Serial Interface* describes the serial interface in more detail. Supports 1.1 V and 1.8 V CMOS levels.
$\overline{\text{SCS}}$	E8	I	Serial interface chip select active low input. *Using the Serial Interface* describes the serial interface in more detail. Supports 1.1 V and 1.8 V CMOS levels. This pin has a 82-kΩ pull-up resistor to VD11.
SDI	G8	I	Serial interface data input. *Using the Serial Interface* describes the serial interface in more detail. Supports 1.1 V and 1.8 V CMOS levels.
SDO	H8	O	Serial interface data output. *Using the Serial Interface* describes the serial interface in more detail. This pin is high impedance during normal device operation. This pin outputs 1.9-V CMOS levels during serial interface read operations. This pin can be left disconnected if not used.
$\overline{\text{SYNCSE}}$	C2	I	Single-ended JESD204B SYNC signal. This input is an active low input that is used to initialize the JESD204B serial link when SYNC_SEL is set to 0. When toggled low it initiates code group synchronization (Code Group Synchronization (CGS)). After code group synchronization, it must be toggled high to start the initial lane alignment sequence (Initial Lane Alignment Sequence (ILAS)). A differential SYNC signal can be used instead by setting SYNC_SEL to 1 and using TMSTP+/– as a differential $\overline{\text{SYNC}}$ input. This pin should be tied to GND if differential $\overline{\text{SYNC}}$ (TMSTP+/-) is used as the JESD204B SYNC signal.
SYSREF+	K1	I	SYSREF positive input used to achieve synchronization and deterministic latency across the JESD204B interface. This differential input (SYSREF+ to SYSREF–) has an internal untrimmed 100-Ω differential termination and can be AC coupled when SYSREF_LVPECL_EN is set to 0. This input is self-biased when SYSREF_LVPECL_EN is set to 0. The termination changes to 50 Ω to ground on each input pin (SYSREF+ and SYSREF–) and can be DC coupled when SYSREF_LVPECL_EN is set to 1. This input is not self-biased when SYSREF_LVPECL_EN is set to 1 and must be biased externally to the input common mode voltage range provided in Recommended Operating Conditions.
SYSREF-	L1	I	SYSREF negative input.
TDIODE+	K2	I	Temperature diode positive (anode) connection. An external temperature sensor can be connected to TDIODE+ and TDIODE- to monitor the junction temperature of the device. This pin can be left disconnected if not used.
TDIODE-	K3	I	Temperature diode negative (cathode) connection. This pin can be left disconnected if not used.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TMSTP+	B1	I	Timestamp input positive connection or differential JESD204B $\overline{\text{SYNC}}$ positive connection. This input is a timestamp input, used to mark a specific sample, when TIMESTAMP_EN is set to 1. This differential input is used as the JESD204B SYNC signal input when SYNC_SEL is set 1. It can be used as both timestamp and differential SYNC input at the same time, allowing feedback of the SYNC signal using the timestamp mechanism. TMSTP+/– uses active low signaling when used as JESD204B SYNC. For additional usage information refer to *Timestamp*. TMSTP_RECV_EN must be set to 1 to use this input. This differential input (TMSTP+ to TMSTP–) has an internal untrimmed 100-Ω differential termination and can be AC coupled when TMSTP_LVPECL_EN is set to 0. The termination changes to 50 Ω to ground on each input pin (TMSTP+ and TMSTP–) and can be DC coupled when TMSTP_LVPECL_EN is set to 1. This pin is not self-biased and therefore it must be externally biased for both AC and DC coupled configurations. The common mode voltage must be within the range provided in Recommended Operating Conditions when both AC and DC coupled. This pin can be left disconnected and disabled (TMSTP_RECV_EN = 0) if $\overline{\text{SYNCSE}}$ is used for JESD204B SYNC and timestamp is not required.
TMSTP-	C1	I	Timestamp input positive connection or differential JESD204B $\overline{\text{SYNC}}$ negative connection. This pin can be left disconnected and disabled (TMSTP_RECV_EN = 0) if $\overline{\text{SYNCSE}}$ is used for JESD204B SYNC and timestamp is not required.
VA11	C5, D2, D3, D5, E5, F5, G5, H5, J2, J3, J5, K5	I	1.1-V analog supply.
VA19	C4, D4, E2, E3, E4, F4, G4, H2, H3, H4, J4, K4	I	1.9-V analog supply.
VD11	C9, C10, E9, E10, G7, H7, H9, H10, K9, K10	I	1.1-V digital supply.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range	VA19(2)	-0.3	2.35	V
	VA11(2)	-0.3	1.32	V
	VD11(3)	-0.3	1.32	V
	Voltage between VD11 and VA11	-1.32	1.32	V
Voltage between AGND and DGND		-0.1	0.1	V
Terminal Voltage Range	DA0...7+, DA0...7-, DB0...7+, DB0...7-, TMSTP+, TMSTP–(3)	-0.5	min(1.32, VD11+0.5)	V
	CLK+, CLK–, SYSREF+, SYSREF–(2)	-0.5	min(1.32, VA11+0.5)	V
	BG, TDIODE+, TDIODE–(2)	-0.5	min(2.35, VA19+0.5)	V
	INA+, INA–, INB+, INB–(2)	-1	1	V
	CALSTAT, CALTRIG, NCOA0, NCOA1, NCOB0, NCOB1, $\overline{\text{ORA0}}$, ORA1, ORB0, $\overline{\text{ORB1}}$, PD, SCLK, $\overline{\text{SCS}}$, SDI, SDO, $\overline{\text{SYNCSE}}$(2)	-0.5	VA19+0.5	V
Peak input current (any input except INA+, INA–, INB+, INB–)		-25	25	mA
Peak input current (INA+, INA–, INB+, INB–)		-50	50	mA
Peak RF input power (INA+, INA–, INB+, INB–)	Single-ended with $Z_{S\text{-}SE}$ = 50 Ω or differential with $Z_{S\text{-}DIFF}$ = 100 Ω		16.4	dBm
Peak total input current (sum of absolute value of all currents forced in or out, not including power supply current)			100	mA
Operating junction temperature, T_j			150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured to AGND.
(3) Measured to DGND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply Voltage Range	VA19, Analog 1.9V supply(1)	1.8	1.9	2.0	V
		VA11, Analog 1.1V supply(1)	1.05	1.1	1.15	V
		VD11, Digital 1.1V supply(2)	1.05	1.1	1.15	V
V_{CMI}	Input common mode voltage	INA+, INA–, INB+, INB–(1)	-50	0	100	mV
		CLK+, CLK–, SYSREF+, SYSREF–(1)(3)	0.0	0.3	0.55	V
		TMSTP+, TMSTP–(1)(4)	0.0	0.3	0.55	V
V_{ID}	Input voltage, peak-to-peak differential	CLK+ to CLK–, SYSREF+ to SYSREF–, TMSTP+ to TMSTP–	0.4	1.0	2.0	$V_{PP-DIFF}$
		INA+ to INA–, INB+ to INB–			1.0(5)	$V_{PP-DIFF}$
V_{IH}	High level input voltage	CALTRIG, NCOA0, $\overline{\text{NCOA1}}$, NCOB0, $\overline{\text{NCOB1}}$, PD, SCLK, $\overline{\text{SCS}}$, SDI, $\overline{\text{SYNCSE}}$(1)	0.7			V
V_{IL}	Low level input voltage	CALTRIG, NCOA0, $\overline{\text{NCOA1}}$, NCOB0, $\overline{\text{NCOB1}}$, PD, SCLK, $\overline{\text{SCS}}$, SDI, $\overline{\text{SYNCSE}}$(1)			0.45	V
I_{C_TD}	Temperature diode input current	TDIODE+ to TDIODE–		100		µA
C_L	BG max load capacitance				50	pF
I_O	BG max output current				100	µA
DC	Input clock duty cycle		30	50	70	%
T_A	Operating free-air temperature		-40		85	ºC
T_j	Operating junction temperature				105(6)(7)	ºC

(1) Measured to AGND.
(2) Measured to DGND.
(3) It is strongly recommended that CLK+/– be AC coupled with DEVCLK_LVPECL_EN set to 0 to allow CLK+/– to self bias to the optimal input common mode voltage for best performnace. TI recommends AC coupling for SYSREF+/– unless DC coupling is required, in which case LVPECL input mode must be used (SYSREF_LVPECL_EN = 1).
(4) TMSTP+/– does not have internal biasing which requires TMSTP+/– to be biased externally whether AC coupled with TMSTP_LVPECL_EN = 0 or DC coupled with TMSTP_LVPECL_EN = 1.
(5) ADC output code will saturate when V_{ID} for INA+/– or INB+/– exceeds the programmed full-scale voltage (V_{FS}) set by FS_RANGE_A for INA+/– or FS_RANGE_B for INB+/–.
(6) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.
(7) Tested up to 1000 hours continuous operation at T_j = 125°C. See Absolute Maximum Ratings for absolute maximum operational temperature.

NOTE

Power down of the high speed data outputs (DA0+/– ... DA7+/–, DB0+/– ... DB7+/–) for extended times may reduce performance of the output serializers, especially at high data rates. Power down of the serializers occurs when the PD pin is held high, the MODE register is programmed to a value other than 0x00 or 0x01, PD_ACH or PD_BCH registers settings are programmed to 1 or when the JMODE register setting is programmed to a mode that uses less than the 16 total lanes the device allows. For instance, JMODE 0 uses eight total lanes and therefore the four highest indexed lanes for each JESD204B link (DA4+/– ... DA7+/–, DB4+/– ... DB7+/–) are powered down in this mode. When the PD pin is held high or the MODE register is programmed to a value other than 0x00 or 0x01 then all of the output serializers are powered down. When PD_ACH or PD_BCH register settings are programmed to 1 the associated ADC channel and lanes are powered down. To prevent unreliable operation the PD pin and MODE register should only be used for brief periods of time to measure temperature diode offsets and not used for long-term power savings. Further, use of a JMODE that uses fewer than 16 lanes will result in unreliable operation of the unused lanes. If the system will never use the unused lanes during the lifetime of the device then the unused lanes will not cause issues and can be powered down. If the system may make use of the unused lanes at a later time, the reliable operation of the serializer outputs can be maintained by enabling JEXTRA_A and JEXTRA_B which results in VD11 power consumption to increase and the output serializers to toggle.

6.4 Thermal Information

THERMAL METRIC(1)		ADC12DJ3200 AAV (FCBGA) 144 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics - DC Specifications

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
Resolution		Resolution with no missing codes		12		bits
DNL	Differential nonlinearity			±0.3		LSB
INL	Integral nonlinearity			±2.5		LSB
ANALOG INPUTS (INA+, INA–, INB+, INB–)						
V_{OFF}	Offset Error	Default full-scale voltage, OS_CAL disabled		±0.6		mV
V_{OFF_ADJ}	Input offset voltage adjustment range	Available offset correction range (see OS_CAL or OADJ_x_INx)		±55		mV
V_{OFF_DRIFT}	Offset Drift	Foreground calibration at nominal temperature only		23		µV/°C
		Foreground calibration at each temperature		0		µV/°C
V_{IN_FSR}	Analog differential input full scale range	Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000)	750	800	850	mV_{PP}
		Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF)	1000	1040		mV_{PP}
		Minimum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0x2000)		480	500	mV_{PP}
$V_{IN\_FSR\_DRIFT}$	Analog differential input full scale range drift	Default FS_RANGE_A and FS_RANGE_B setting, foreground calibration at nominal temperature only, inputs driven by 50-Ω source, includes effect of R_{IN} drift		-0.01		%/°C
		Default FS_RANGE_A and FS_RANGE_B setting, foreground calibration at each temperature, inputs driven by 50-Ω source, includes effect of R_{IN} drift		0.03		%/°C
$V_{IN\_FSR\_MATCH}$	Analog differential input full scale range matching	Matching between INA+/INA– and INB+/INB–, default setting, dual channel mode		0.625		%
R_{IN}	Single-ended input resistance to AGND	Each input terminal is terminated to AGND, measured at T_A = 25°C	48	50	52	Ω
R_{IN_TEMPCO}	Input termination linear temperature coefficient			17.6		mΩ/°C
C_{IN}	Single-ended input capacitance	Single channel mode at DC		0.4		pF
		Dual channel mode at DC		0.4		pF
TEMPERATURE DIODE CHARACTERISTICS (TDIODE+, TDIODE–)						
ΔV_{BE}	Temperature diode voltage slope	Forced forward current of 100 µA. Offset voltage (approx. 0.792 V at 0°C) varies with process and must be measured for each part. Offset measurement should be done with the device unpowered or with the PD pin asserted to minimize device self-heating. PD pin should be asserted only long enough to take the offset measurement.		-1.6		mV/°C
BANDGAP VOLTAGE OUTPUT (BG)						
V_{BG}	Reference output voltage	I_L ≤ 100 µA		1.1		V
V_{BG_DRIFT}	Reference output temperature drift	I_L ≤ 100 µA		-64		µV/°C

Electrical Characteristics - DC Specifications (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK INPUTS (CLK+, CLK–, SYSREF+, SYSREF–, TMSTP+, TMSTP–)						
Z_T	Internal termination	Differential termination with DEVCLK_LVPECL_EN = 0, SYSREF_LVPECL_EN = 0 and TMSTP_LVPECL_EN = 0		110		Ω
		Single ended termination to GND (per pin) with DEVCLK_LVPECL_EN = 0, SYSREF_LVPECL_EN = 0 and TMSTP_LVPECL_EN = 0		55		Ω
V_{CM}	Input common mode voltage, self-biased	Self-biasing common mode voltage for CLK+/– when AC coupled (DEVCLK_LVPECL_EN must be set to 0)		0.26		V
		Self-biasing common mode voltage for SYSREF+/– when AC coupled (SYSREF_LVPECL_EN must be set to 0) and with receiver enabled (SYSREF_RECV_EN = 1).		0.29		V
		Self-biasing common mode voltage for SYSREF+/– when AC coupled (SYSREF_LVPECL_EN must be set to 0) and with receiver disabled (SYSREF_RECV_EN = 0).		VA11		V
C_{L_DIFF}	Differential input capacitance	Between positive and negative differential input pins		0.1		pF
C_{L_SE}	Single-ended input capacitance	Each input to ground		0.5		pF
SERDES OUTPUTS (DA0+/DA0–...DA7+/DA7–, DB0+/DB0–...DB7+/DB7–)						
V_{OD}	Differential output voltage, peak-to-peak	100-Ω load	550	600	650	$mV_{PP-DIFF}$
V_{CM}	Output common mode voltage	AC coupled		VD11/2		V
Z_{DIFF}	Differential output impedance			100		Ω
CMOS INTERFACE: SCLK, SDI, SDO, $\overline{SCS}$, PD, NCOA0, NCOA1, NCOB0, NCOB1, CALSTAT, CALTRIG, ORA0, ORA1, ORB0, ORB1, SYNCSE						
I_{IH}	High level input current		–40		40	µA
I_{IL}	Low level input current		–40		40	µA
C_I	Input capacitance			2		pF
V_{OH}	High level output voltage	I_{LOAD} = –400 µA	1.65			V
V_{OL}	Low level output voltage	I_{LOAD} = 400 µA			150	mV

6.6 Electrical Characteristics - Power Consumption

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VA19}	1.9-V analog supply current	Power mode 1: Single channel mode, JMODE 1 (16 lanes, DDC bypassed), foreground calibration		897		mA
I_{VA11}	1.1-V analog supply current			491		mA
I_{VD11}	1.1-V digital supply current			640		mA
P_{DIS}	Power dissipation			3.0		W
I_{VA19}	1.9-V analog supply current	Power mode 2: Single channel mode, JMODE 0 (8 lanes, DDC bypassed), foreground calibration		875	950	mA
I_{VA11}	1.1-V analog supply current			515	600	mA
I_{VD11}	1.1-V digital supply current			615	750	mA
P_{DIS}	Power dissipation			2.9	3.5	W
I_{VA19}	1.9-V analog supply current	Power mode 3: Single channel mode, JMODE 1 (16 lanes, DDC bypassed), background calibration		1181		mA
I_{VA11}	1.1-V analog supply current			595		mA
I_{VD11}	1.1-V digital supply current			653		mA
P_{DIS}	Power dissipation			3.6		W
I_{VA19}	1.9-V analog supply current	Power mode 4: Dual channel mode, JMODE 3 (16 lanes, DDC bypassed), background calibration		1260		mA
I_{VA11}	1.1-V analog supply current			594		mA
I_{VD11}	1.1-V digital supply current			636		mA
P_{DIS}	Power dissipation			3.8		W
I_{VA19}	1.9-V analog supply current	Power mode 5: Dual channel mode, JMODE 11 (8 lanes, 4x decimation), foreground calibration		964		mA
I_{VA11}	1.1-V analog supply current			493		mA
I_{VD11}	1.1-V digital supply current			802		mA
P_{DIS}	Power dissipation			3.3		W

6.7 Electrical Characteristics - AC Specifications

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS (INA+, INA–, INB+, INB–)						
FPBW	Full-power input bandwidth (–3 dB)(1)	Dual channel mode, foreground calibration		8.1		GHz
		Single channel mode, foreground calibration		7.9		
		Dual channel mode, background calibration		8.1		
		Single channel mode, background calibration		7.9		
XTALK	Channel-to-channel Crosstalk	Dual channel mode, aggressor = 400 MHz, – 1 dBFS		–93		dB
		Dual channel mode, aggressor = 3 GHz, – 1 dBFS		–70		
		Dual channel mode, aggressor = 6 GHz, – 1 dBFS		–63		
DYNAMIC AC CHARACTERISTICS - DUAL CHANNEL MODE (JMODE 3)						
CER	Code error rate			10^{-18}		errors/sample
$NOISE_{DC}$	DC input noise standard deviation	No input, foreground calibration, excludes DC offset, includes fixed interleaving spur (Fs/2 spur)		2		LSB
NSD	Noise spectral density, no input signal, excludes fixed interleaving spur (Fs/2 spur)	Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF) setting, foreground calibration		-151.8		dBFS/Hz
		Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000) setting, foreground calibration		-150.2		
NF	Noise figure, no input, Z_S = 100 Ω	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting, foreground calibration		23.5		dB
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting, foreground calibration		22.8		
SNR	Signal to noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		56.6		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration		57.6		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		56.3		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	52	55.2		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration		56.1		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		52.6		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		51.3		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		49.8		

(1) Full-power input bandwidth (FPBW) is defined as the input frequency where the reconstructed output of the ADC has dropped 3 dB below the power of a full-scale input signal at a low input frequency. Useable bandwidth may exceed the -3-dB full-power input bandwidth.

Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal to noise ratio, small signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 347 MHz, A_{IN} = –16 dBFS		57.4		dBFS
		f_{IN} = 997 MHz, A_{IN} = –16 dBFS		57.5		
		f_{IN} = 2482 MHz, A_{IN} = –16 dBFS		57.4		
		f_{IN} = 4997 MHz, A_{IN} = –16 dBFS		57.1		
		f_{IN} = 6397 MHz, A_{IN} = –16 dBFS		57.3		
		f_{IN} = 8197 MHz, A_{IN} = –16 dBFS		56.9		
SINAD	Signal to noise and distortion ratio, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		56.0		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		55.7		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	51	54.6		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		50.3		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		48.9		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		47.4		
ENOB	Effective number of bits, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		9.0		bits
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		9.0		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	8.2	8.8		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		8.1		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		7.8		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		7.6		
SFDR	Spurious free dynamic range, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		67		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration		67		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		69		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	60	66		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration		63		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		56		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		55		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		52		
SFDR	Spurious free dynamic range, small signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –16 dBFS		73		dBFS
		f_{IN} = 997 MHz, A_{IN} = –16 dBFS		72		
		f_{IN} = 2482 MHz, A_{IN} = –16 dBFS		72		
		f_{IN} = 4997 MHz, A_{IN} = –16 dBFS		72		
		f_{IN} = 6397 MHz, A_{IN} = –16 dBFS		72		
		f_{IN} = 8197 MHz, A_{IN} = –16 dBFS		72		
F_S/2	F_S/2 fixed interleaving spur, independent of input signal	No input		–75	–55	dBFS

Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd order harmonic	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		–73		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration		–72		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		–72		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS		–67	–60	
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration		–66		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		–58		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		–57		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		–58		
HD3	3rd order harmonic	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		–70		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration		–68		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		–72		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS		–69	–60	
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration		–63		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		–57		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		–55		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		–52		
$F_S/2-F_{IN}$	$F_S/2-F_{IN}$ interleaving spur, signal dependent	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		–69		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		–70		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS		–70	–60	
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		–67		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		–63		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		–63		
SPUR	Worst harmonic 4th order or higher	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		–72		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		–72		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS		–73	–65	
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		–70		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		–69		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		–67		

Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd order intermodulation	f_{IN} = 347 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–81		dBFS
		f_{IN} = 997 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–78		
		f_{IN} = 2482 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–73		
		f_{IN} = 4997 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–65		
		f_{IN} = 6397 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–56		
		f_{IN} = 8197 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–46		

Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC AC CHARACTERISTICS - SINGLE CHANNEL MODE (JMODE 1)						
CER	Code error rate			10^{-18}		errors/sample
$NOISE_{DC}$	DC input noise standard deviation	No input, foreground calibration, excludes DC offset, includes fixed interleaving spurs (Fs/2 and Fs/4 spurs)		3.5		LSB
NSD	Noise spectral density, no input signal, excludes fixed interleaving spurs (Fs/2 and Fs/4 spur)	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting, foreground calibration		-154.6		dBFS/Hz
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting, foreground calibration		-153.1		
NF	Noise figure, no input, Z_S = 100 Ω	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting, foreground calibration		20.7		dB
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting, foreground calibration		19.9		
SNR	Signal to noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		56.6		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration		57.5		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		56.3		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	52	55.3		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration		56.1		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		53.0		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		51.6		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		50.0		
SNR	Signal to noise ratio, small signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 347 MHz, A_{IN} = –16 dBFS		57.4		dBFS
		f_{IN} = 997 MHz, A_{IN} = –16 dBFS		57.6		
		f_{IN} = 2482 MHz, A_{IN} = –16 dBFS		57.4		
		f_{IN} = 4997 MHz, A_{IN} = –16 dBFS		57.3		
		f_{IN} = 6397 MHz, A_{IN} = –16 dBFS		57.4		
		f_{IN} = 8197 MHz, A_{IN} = –16 dBFS		57.0		
SINAD	Signal to noise and distortion ratio, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		52.7		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		52.4		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	48	52.1		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		47.5		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		46.6		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		47.7		

Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits, large signal, excluding DC and F_S/2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		8.6		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		8.5		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	7.7	8.4		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		7.7		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		7.5		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		7.6		
SFDR	Spurious free dynamic range, large signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		67		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration		64		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		63		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	50	58		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration		55		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		51		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		50		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		48		
SFDR	Spurious free dynamic range, small signal, excluding DC, F_S/4 and F_S/2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –16 dBFS		75		dBFS
		f_{IN} = 997 MHz, A_{IN} = –16 dBFS		73		
		f_{IN} = 2482 MHz, A_{IN} = –16 dBFS		72		
		f_{IN} = 4997 MHz, A_{IN} = –16 dBFS		66		
		f_{IN} = 6397 MHz, A_{IN} = –16 dBFS		65		
		f_{IN} = 8197 MHz, A_{IN} = –16 dBFS		63		
F_S/2	F_S/2 fixed interleaving spur, independent of input signal	No input, OS_CAL disabled. Spur can be improved by running OS_CAL.		–56		dBFS
F_S/4	F_S/4 fixed interleaving spur, independent of input signal	No input		–65	–55	dBFS
HD2	2nd order harmonic	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		–73		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration		–76		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		–74		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS		–68	–60	
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration		–72		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		–62		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		–62		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		–61		

Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd order harmonic	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		–70		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration		–68		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		–68		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS		–69	–60	
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration		–64		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		–59		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		–58		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		–55		
$F_S/2-F_{IN}$	$F_S/2-F_{IN}$ interleaving spur, signal dependent	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		–68		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		–63		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS		–58	–50	
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		–51		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		–50		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		–48		
$F_S/4\pm F_{IN}$	$F_S/4\pm F_{IN}$ interleaving spurs, signal dependent	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		–74		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		–69		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS		–70	–60	
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		–66		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		–63		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		–61		
SPUR	Worst harmonic 4th order or higher	f_{IN} = 347 MHz, A_{IN} = –1 dBFS		–73		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS		–73		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS		–75	–65	
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS		–69		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS		–69		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS		–63		
IMD3	3rd order intermodulation	f_{IN} = 347 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–80		dBFS
		f_{IN} = 997 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–75		
		f_{IN} = 2482 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–72		
		f_{IN} = 4997 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–63		
		f_{IN} = 6397 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–65		
		f_{IN} = 8197 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone		–50		

6.8 Timing Requirements

			MIN	NOM	MAX	UNIT
DEVICE (SAMPLING) CLOCK (CLK+, CLK–)						
f_{CLK}	Input clock frequency (CLK+, CLK–), both single channel and dual channel modes(1)		800		3200	MHz
SYSREF (SYSREF+, SYSREF–)						
$t_{INV(SYSREF)}$	Width of invalid SYSREF capture region of CLK+/– period, indicating setup or hold time violation, as measured by SYSREF_POS status register(2)			48		ps
$t_{INV(TEMP)}$	Drift of invalid SYSREF capture region over temperature, positive number indicates a shift toward MSB of SYSREF_POS register			0		ps/°C
$t_{INV(VA11)}$	Drift of invalid SYSREF capture region over VA11 supply voltage, positive number indicates a shift toward MSB of SYSREF_POS register			0.36		ps/mV
$t_{STEP(SP)}$	Delay of SYSREF_POS LSB	SYSREF_ZOOM = 0		77		ps
		SYSREF_ZOOM = 1		24		ps
$t_{(PH\_SYS)}$	Minimum SYSREF+/– assertion duration after SYSREF+/– rising edge event			4		ns
$t_{(PL\_SYS)}$	Minimum SYSREF+/– deassertion duration after SYSREF+/– falling edge event			1		ns
JESD204B SYNC TIMING ($\overline{\text{SYNCSE}}$ OR TMSTP+/–)						
$t_{H(\overline{SYNCSE})}$	Minimum hold time from multi-frame boundary (SYSREF rising edge captured high) to de-assertion of JESD204B SYNC signal ($\overline{\text{SYNCSE}}$ if SYNC_SEL = 0 or TMSTP+/– if SYNC_SEL = 1) for NCO synchronization (NCO_SYNC_ILA = 1)	JMODE = 0, 2, 4, 6, 10, 13 or 15		21		t_{CLK} cycles
		JMODE = 1, 3, 5, 7, 9, 11, 14 or 16		17		
		JMODE = 12, 17 or 18		9		
$t_{SU(\overline{SYNCSE})}$	Minimum setup time from de-assertion of JESD204B SYNC signal ($\overline{\text{SYNCSE}}$ if SYNC_SEL = 0 or TMSTP+/– if SYNC_SEL = 1) to multi-frame boundary (SYSREF rising edge captured high) for NCO synchronization (NCO_SYNC_ILA = 1)	JMODE = 0, 2, 4, 6, 10, 13 or 15		–2		t_{CLK} cycles
		JMODE = 1, 3, 5, 7, 9, 11, 14 or 16		2		
		JMODE = 12, 17 or 18		10		
$t_{(\overline{SYNCSE})}$	$\overline{\text{SYNCSE}}$ minimum assertion time to trigger link resynchronization			4		Frames
SERIAL PROGRAMMING INTERFACE (SCLK, SDI, $\overline{\text{SCS}}$)						
$f_{CLK(SCLK)}$	Maximum serial clock frequency			15.625		MHz
$t_{(PH)}$	Minimum serial clock high value pulse width			32		ns
$t_{(PL)}$	Minimum serial clock low value pulse width			32		ns
$t_{SU(\overline{SCS})}$	Minimum setup time from $\overline{\text{SCS}}$ to rising edge of SCLK			30		ns
$t_{H(\overline{SCS})}$	Minimum hold time from rising edge of SCLK to $\overline{\text{SCS}}$			3		ns
$t_{SU(SDI)}$	Minimum setup time from SDI to rising edge of SCLK			30		ns
$t_{H(SDI)}$	Minimum hold time from rising edge of SCLK to SDI			3		ns

(1) Unless functionally limited to a smaller range in Table 18 based on programmed JMODE.
(2) SYSREF_POS should be used to select an optimal SYSREF_SEL value for SYSREF capture, see SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) for more information on SYSREF Windowing. The invalid region, specified by $t_{INV(SYSREF)}$, indicates the portion of the CLK+/– period (t_{CLK}), as measured by SYSREF_SEL, that may result in a setup and hold violation. The user should verify that the timing skew between SYSREF+/– and CLK+/– over system operating conditions from the nominal conditions (that used to find optimal SYSREF_SEL) does not result in the invalid region occurring at the selected SYSREF_SEL position in SYSREF_POS, otherwise a temperature dependent SYSREF_SEL selection may be needed to track the skew between CLK+/– and SYSREF+/–.

6.9 Switching Characteristics

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE (SAMPLING) CLOCK (CLK+, CLK–)						
t_{AD}	Sampling (aperture) delay from CLK+/- rising edge (dual channel mode) or rising and falling edge (single channel mode) to sampling instant	TAD_COARSE = 0x00, TAD_FINE = 0x00 and TAD_INV = 0		360		ps
$t_{TAD(MAX)}$	Maximum t_{AD} Adjust programmable delay, not including clock inversion (TAD_INV = 0)	Coarse adjustment (TAD_COARSE = 0xFF)		289		ps
		Fine adjustment (TAD_FINE = 0xFF)		4.9		ps
$t_{TAD(STEP)}$	t_{AD} Adjust programmable delay step size	Coarse adjustment (TAD_COARSE)		1.13		ps
		Fine adjustment (TAD_FINE)		19		fs
t_{AJ}	Aperture jitter, rms	Minimum t_{AD} Adjust coarse setting (TAD_COARSE = 0x00, TAD_INV = 0)		50		fs
		Maximum t_{AD} Adjust coarse setting (TAD_COARSE = 0xFF) excluding TAD_INV (TAD_INV = 0)		70 (1)		fs
SERIAL DATA OUTPUTS (DA0+...DA7+, DA0–...DA7–, DB0+...DB7+, DB0–...DB7–)						
f_{SERDES}	Serialized output bit rate		1		12.8	Gbps
UI	Serialized output unit interval		78.125		1000	ps
t_{TLH}	Low-to-high transition time (differential)	20% to 80%, PRBS-7 test pattern, 12.8 Gbps, SER_PE = 0x04		37		ps
t_{THL}	High-to-low transition time (differential)	20% to 80%, PRBS-7 test pattern, 12.8 Gbps, SER_PE = 0x04		37		ps
DDJ	Data dependent jitter, peak-to-peak	PRBS-7 test pattern, 12.8 Gbps, SER_PE = 0x04, JMODE = 2		7.8		ps
RJ	Random jitter, RMS	PRBS-7 test pattern, 12.8 Gbps, SER_PE = 0x04, JMODE = 2		1.1		ps
TJ	Total jitter, peak-to-peak, with gaussian portion defined with respect to a BER=1e-15 (Q=7.94)	PRBS-7 test pattern, 12.8 Gbps, SER_PE = 0x04, JMODE = 0, 2		25		ps
		PRBS-7 test pattern, 6.4 Gbps, SER_PE = 0x04, JMODE = 1, 3		21		ps
		PRBS-7 test pattern, 8 Gbps, SER_PE = 0x04, JMODE = 4, 5, 6, 7		28		ps
		PRBS-7 test pattern, 8 Gbps, SER_PE = 0x04, JMODE = 9		35		ps
		PRBS-7 test pattern, 8 Gbps, SER_PE = 0x04, JMODE = 10, 11		40		ps
		PRBS-7 test pattern, 3.2 Gbps, SER_PE = 0x04, JMODE = 12		26		ps
		PRBS-7 test pattern, 8 Gbps, SER_PE = 0x04, JMODE = 13, 14		39		ps
		PRBS-7 test pattern, 8 Gbps, SER_PE = 0x04, JMODE = 15, 16		34		ps

(1) t_{AJ} increases due to additional attenuation on internal clock path.

Switching Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC CORE LATENCY						
t_{ADC}	Deterministic delay from the CLK+/– edge that samples the reference sample to the CLK+/– edge that samples SYSREF going high(2)	JMODE = 0		-8.5		t_{CLK} cycles
		JMODE = 1		-20.5		
		JMODE = 2		-9		
		JMODE = 3		-21		
		JMODE = 4		-4.5		
		JMODE = 5		-24.5		
		JMODE = 6		-5		
		JMODE = 7		-25		
		JMODE = 9		60		
		JMODE = 10		140		
		JMODE = 11		136		
		JMODE = 12		120		
		JMODE = 13		232		
		JMODE = 14		232		
		JMODE = 15		446		
		JMODE = 16		430		
		JMODE = 17		-48.5		
		JMODE = 18		-49		
JESD204B AND SERIALIZER LATENCY						
t_{TX}	Delay from the CLK+/– rising edge that samples SYSREF high to the first bit of the multi-frame on the JESD204B serial output lane corresponding to the reference sample of t_{ADC} (3)	JMODE = 0	72		84	t_{CLK} cycles
		JMODE = 1	119		132	
		JMODE = 2	72		84	
		JMODE = 3	119		132	
		JMODE = 4	67		80	
		JMODE = 5	106		119	
		JMODE = 6	67		80	
		JMODE = 7	106		119	
		JMODE = 9	106		119	
		JMODE = 10	67		80	
		JMODE = 11	106		119	
		JMODE = 12	213		225	
		JMODE = 13	67		80	
		JMODE = 14	106		119	
		JMODE = 15	67		80	
		JMODE = 16	106		119	
		JMODE = 17	195		208	
		JMODE = 18	195		208	

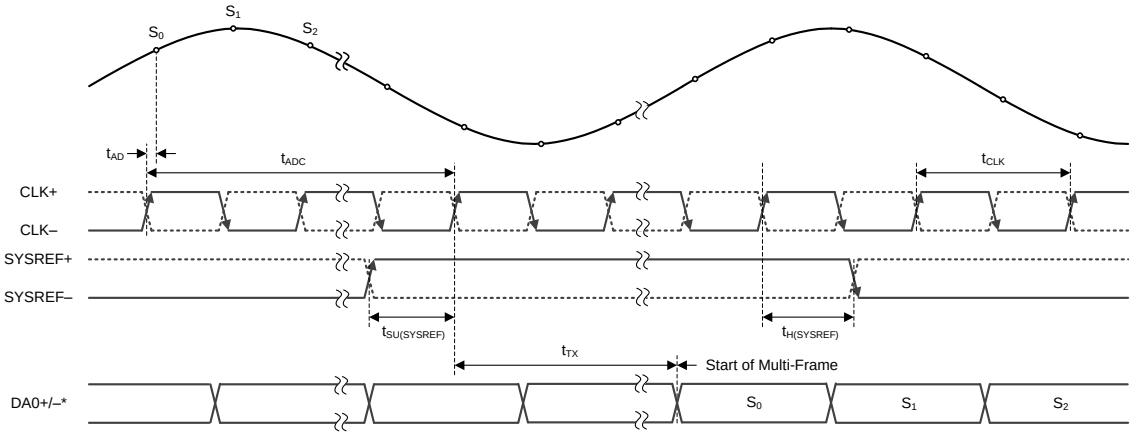
(2) t_{ADC} is an exact, unrounded, deterministic delay. The delay can be negative if the reference sample is sampled after the SYSREF high capture point, in which case the total latency is smaller than the delay given by t_{TX}.

(3) The values given for t_{TX} include deterministic and non-deterministic delays. Over process, temperature, and voltage, the delay will vary. JESD204B accounts for these variations when operating in subclass-1 mode in order to achieve deterministic latency. Proper receiver RBD value must be chosen such that the elastic buffer release point does not occur within the invalid region of the local multi-frame clock (LMFC) cycle.

Switching Characteristics (continued)

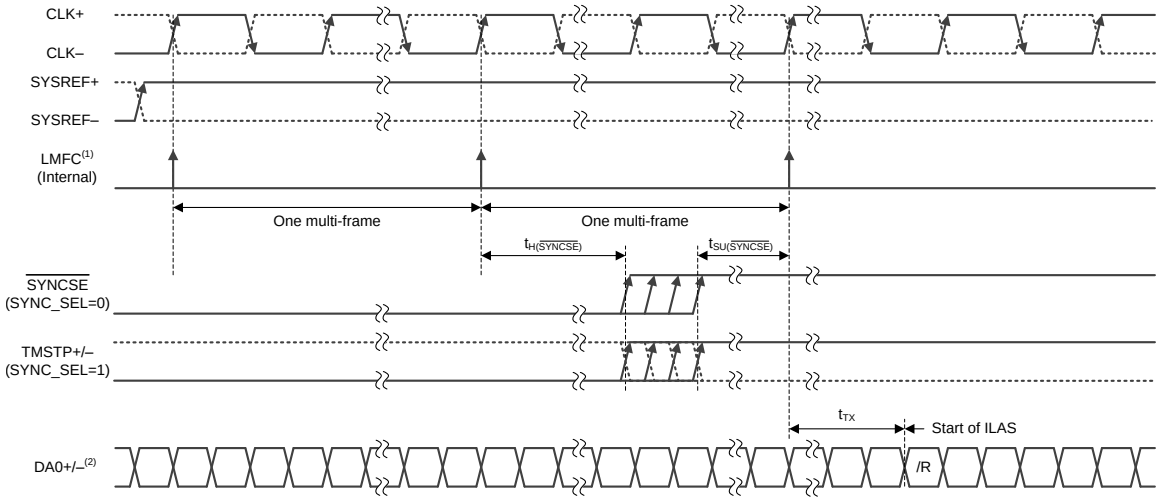
Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = 1.1V, VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/– in single channel modes, f_{IN} = 248 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum rated clock frequency, filtered 1-Vpp sine-wave clock, JMODE = 1, background calibration, unless otherwise noted. Minimum and maximum values are at nominal supply voltages and over operating free-air temperature range provided in Recommended Operating Conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL PROGRAMMING INTERFACE (SDO)						
$t_{(OZD)}$	Maximum delay from falling edge of 16th SCLK cycle during read operation for SDO transition from tri-state to valid data			7		ns
$t_{(ODZ)}$	Maximum delay from $\overline{SCS}$ rising edge for SDO transition from valid data to tri-state			7		ns
$t_{(OD)}$	Maximum delay from falling edge of 16th SCLK cycle during read operation to SDO valid			12		ns



* Only serdes lane DA0+/- is shown, but it is representative of all lanes. The number of output lanes used and bit-packing format is dependent on the programmed JMODE value.

Figure 1. ADC Timing Diagram



(1) It is assumed that the internal LMFC is aligned with the rising edge of CLK+/- that captures SYSREF+/- high value.
(2) Only serdes lane DA0+/- is shown, but it is representative of all lanes. All lanes will output /R at approximately the same point in time. Number of lanes is dependent on the programmed JMODE value.

Figure 2. $\overline{SYNCSE}$ and TMSTP+/– Timing Diagram for NCO Synchronization

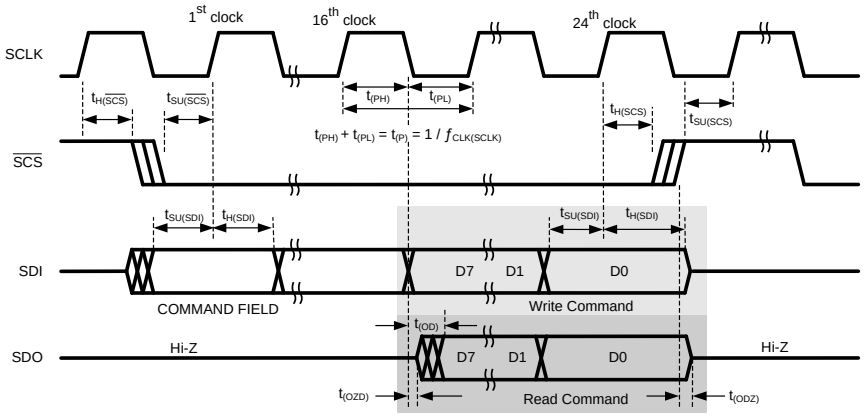


Figure 3. Serial Interface Timing

6.10 Typical Characteristics

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.

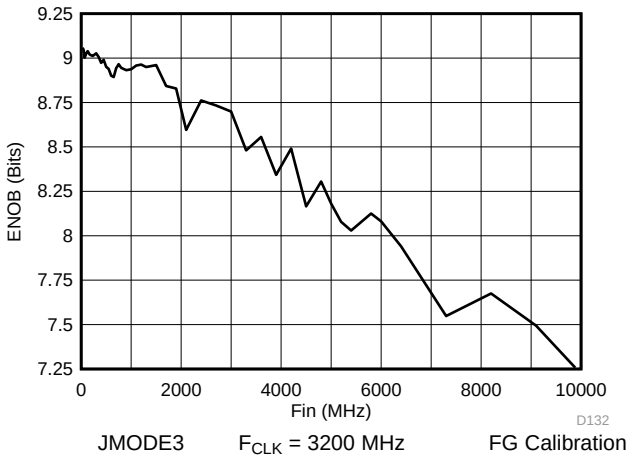


Figure 4. ENOB vs Input Frequency

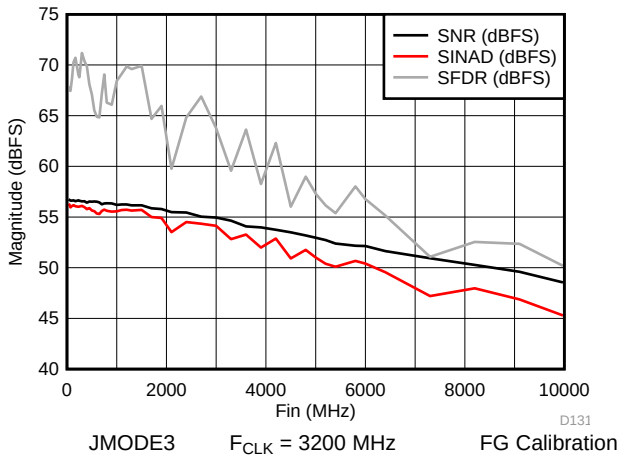


Figure 5. SNR, SINAD, SFDR vs Input Frequency

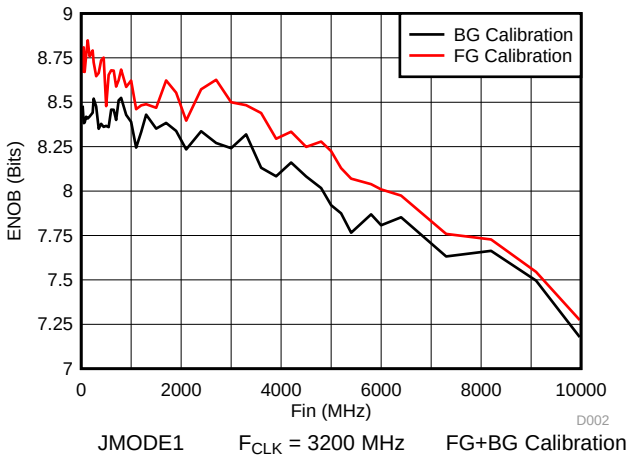


Figure 6. ENOB vs Input Frequency

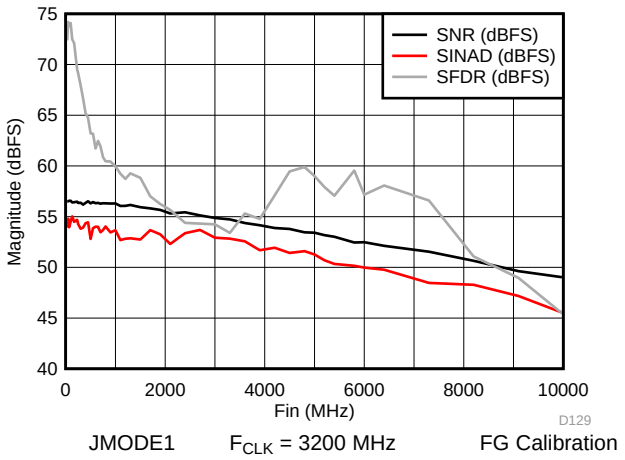


Figure 7. SNR, SINAD, SFDR vs Input Frequency

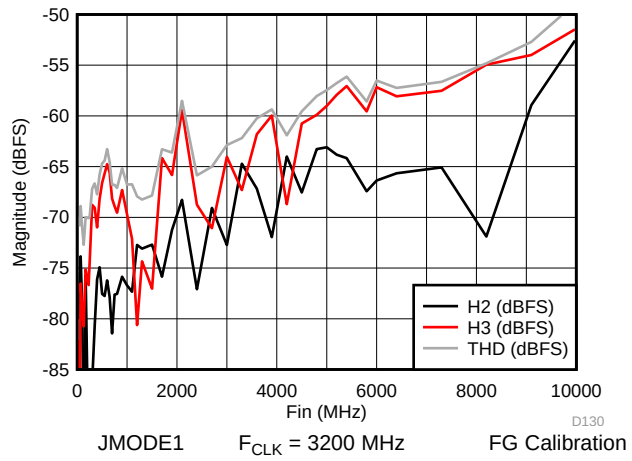


Figure 8. H2, H3, THD vs Input Frequency

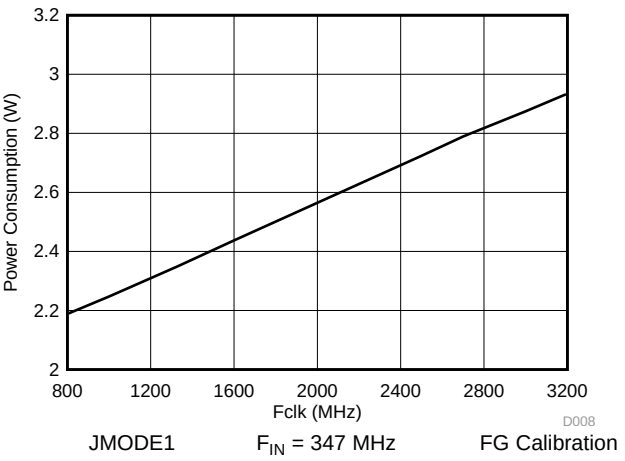
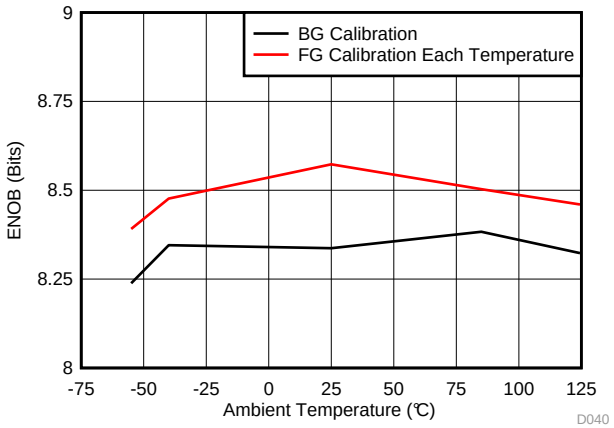


Figure 9. Power Consumption vs Clock Frequency

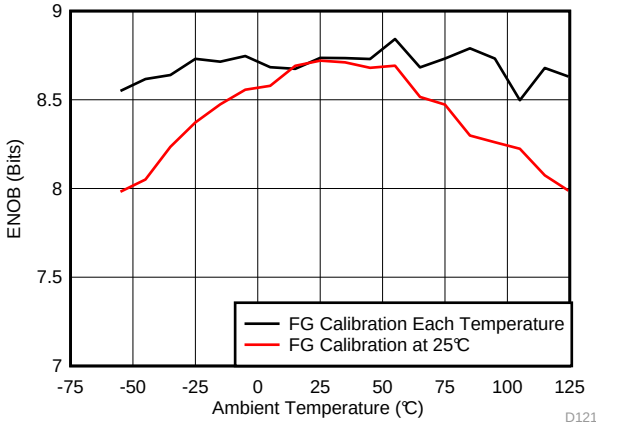
Typical Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.



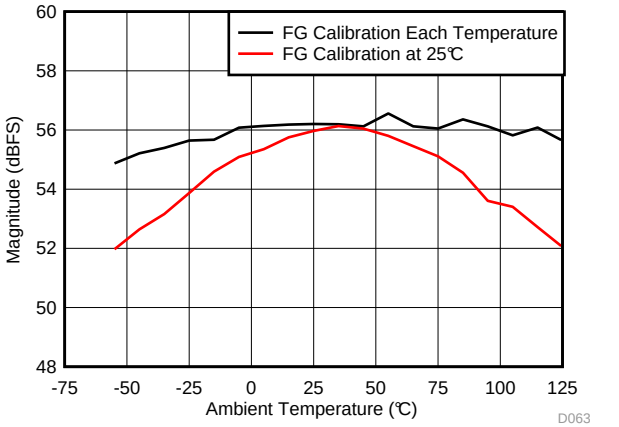
JMODE1 F_{IN} = 2400 MHz

Figure 10. ENOB vs Temperature



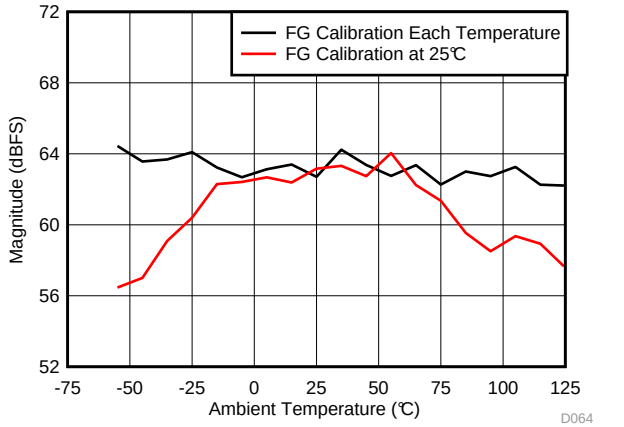
JMODE1 F_{IN} = 600 MHz F_{CLK} = 3200 MHz

Figure 11. ENOB vs Temperature and Calibration Type



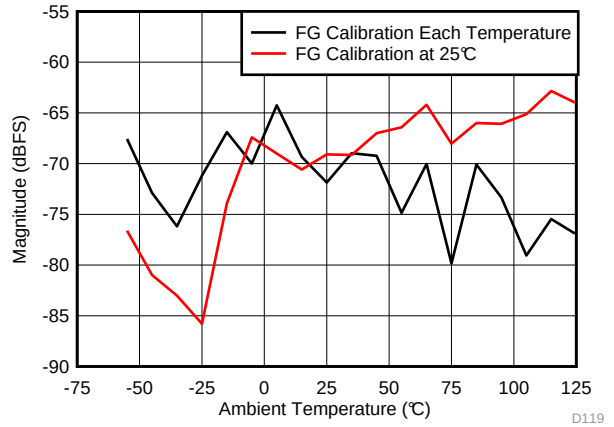
JMODE1 F_{IN} = 600 MHz F_{CLK} = 3200 MHz

Figure 12. SNR vs Temperature and Calibration Type



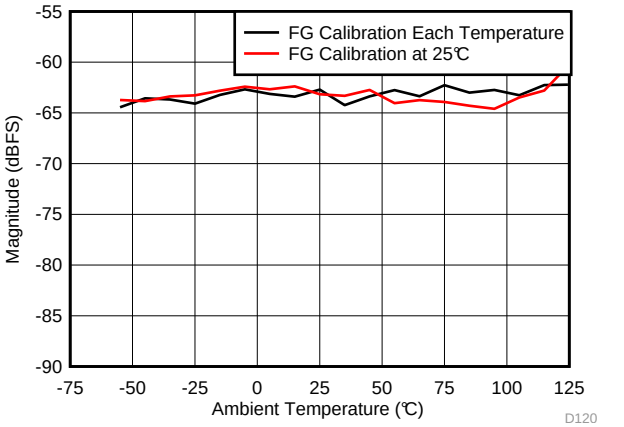
JMODE1 F_{IN} = 600 MHz F_{CLK} = 3200 MHz

Figure 13. SFDR vs Temperature and Calibration Type



JMODE1 F_{IN} = 600 MHz F_{CLK} = 3200 MHz

Figure 14. H2 vs Temperature and Calibration Type



JMODE1 F_{IN} = 600 MHz F_{CLK} = 3200 MHz

Figure 15. H3 vs Temperature and Calibration Type

Typical Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.

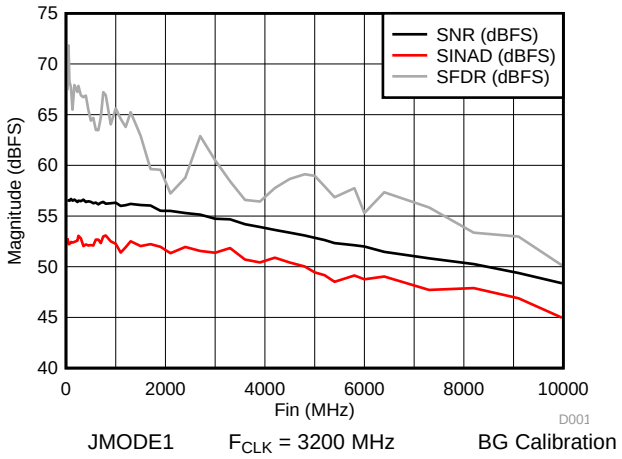


Figure 16. SNR, SINAD, SFDR vs Input Frequency

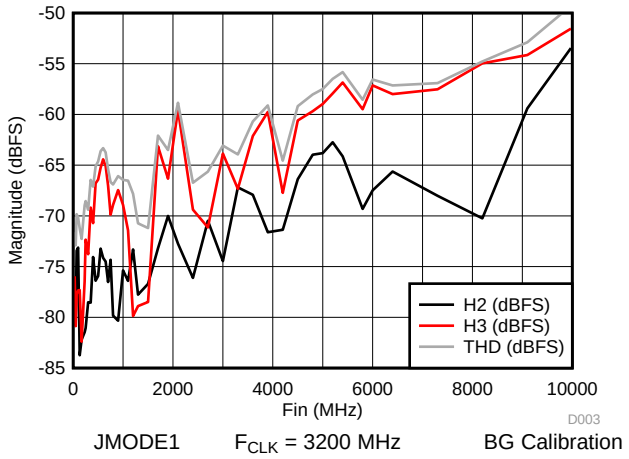


Figure 17. H2, H3, THD vs Input Frequency

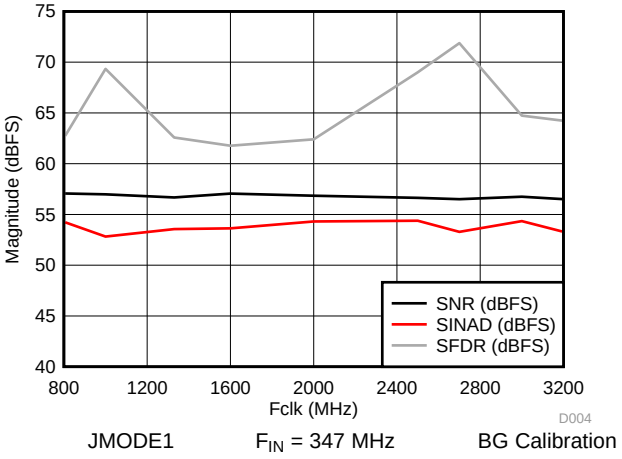


Figure 18. SNR, SINAD, SFDR vs Clock Frequency

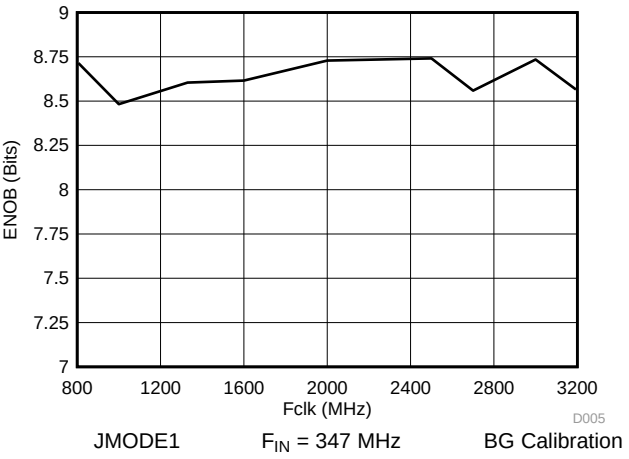


Figure 19. ENOB vs Clock Frequency

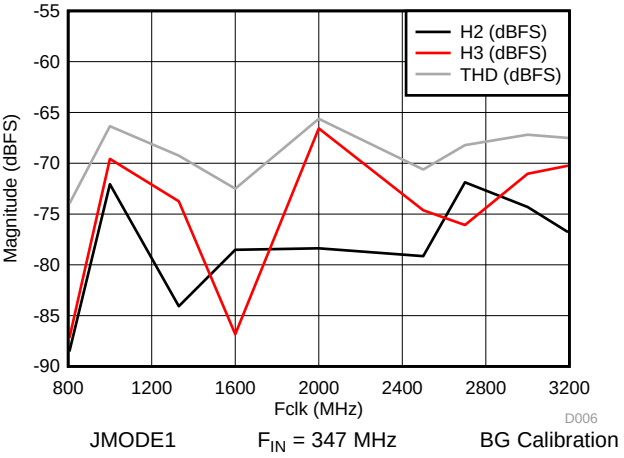


Figure 20. H2, H3, THD vs Clock Frequency

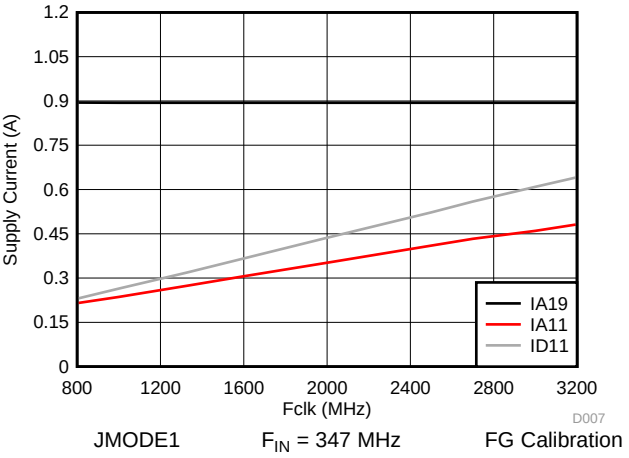


Figure 21. Supply Current vs Clock Frequency

Typical Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.

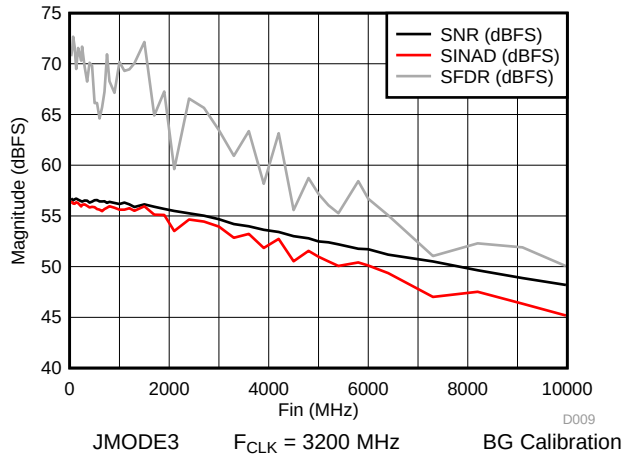


Figure 22. SNR, SINAD, SFDR vs Input Frequency

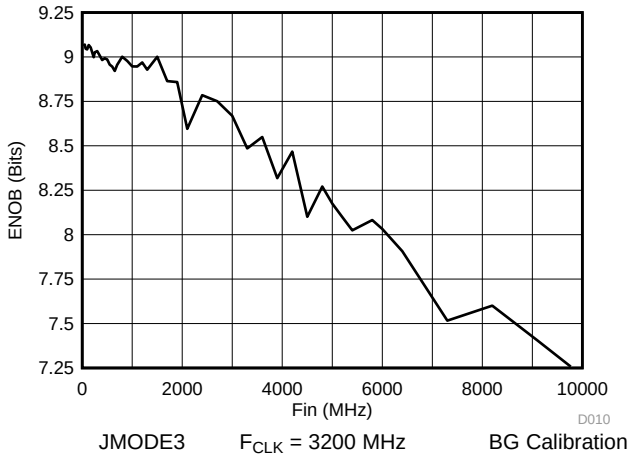


Figure 23. ENOB vs Input Frequency

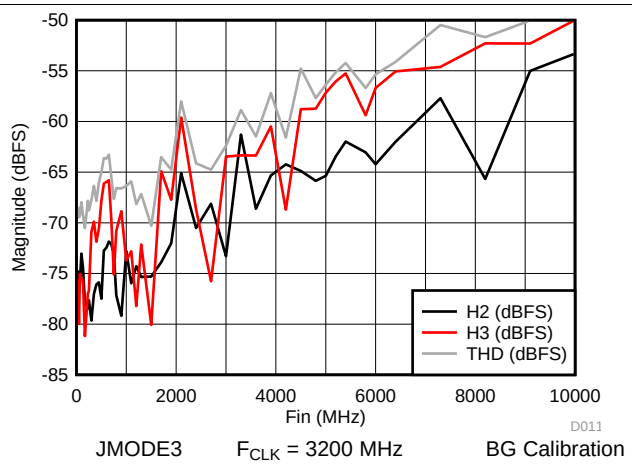


Figure 24. H2, H3, THD vs Input Frequency

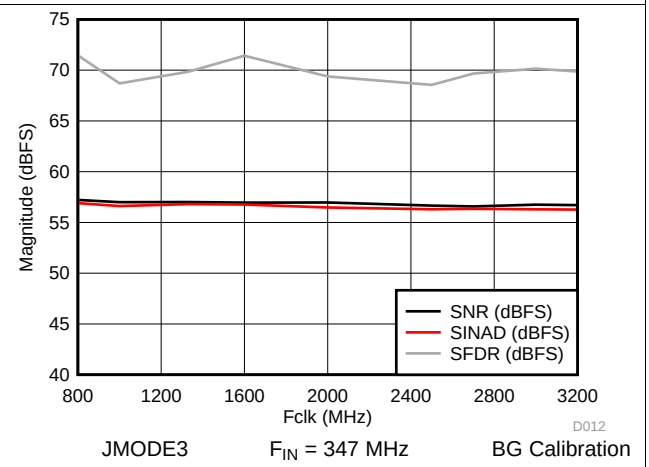


Figure 25. SNR, SINAD, SFDR vs Clock Frequency

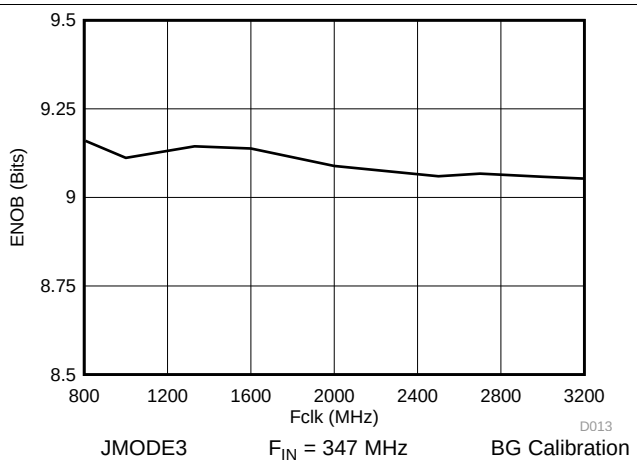


Figure 26. ENOB vs Clock Frequency

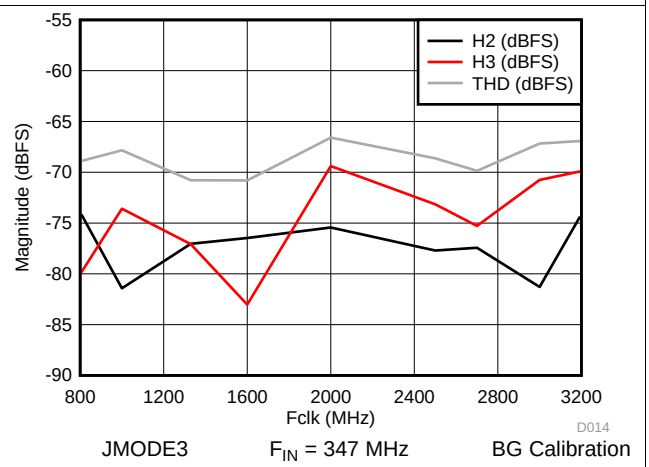


Figure 27. H2, H3, THD vs Clock Frequency

Typical Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.

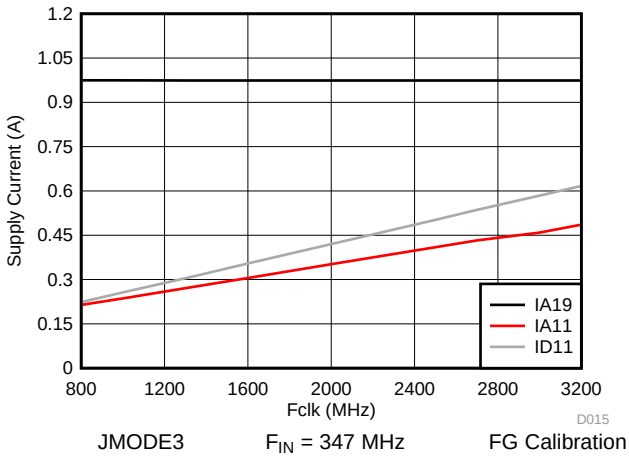


Figure 28. Supply Current vs Clock Frequency

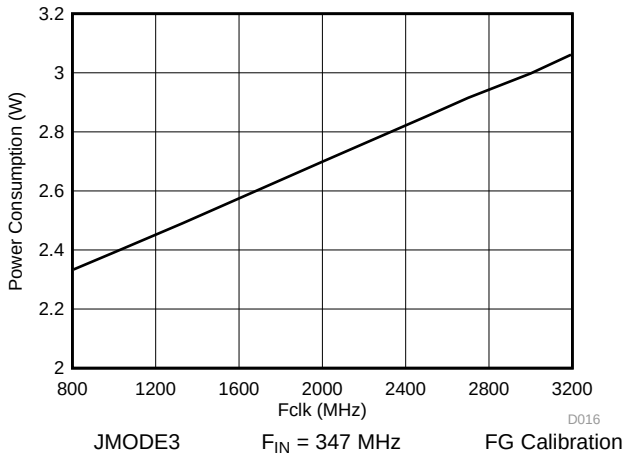


Figure 29. Power Consumption vs Clock Frequency

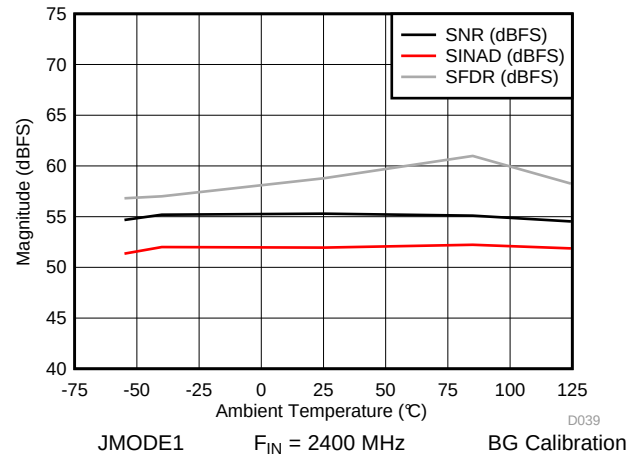


Figure 30. SNR, SINAD, SFDR vs Temperature

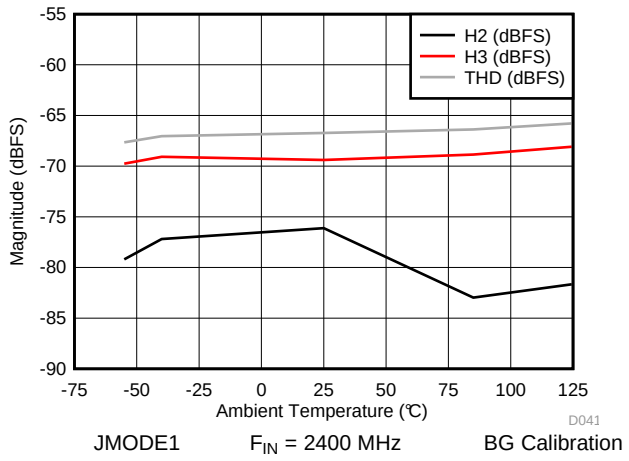


Figure 31. H2, H3, THD vs Temperature

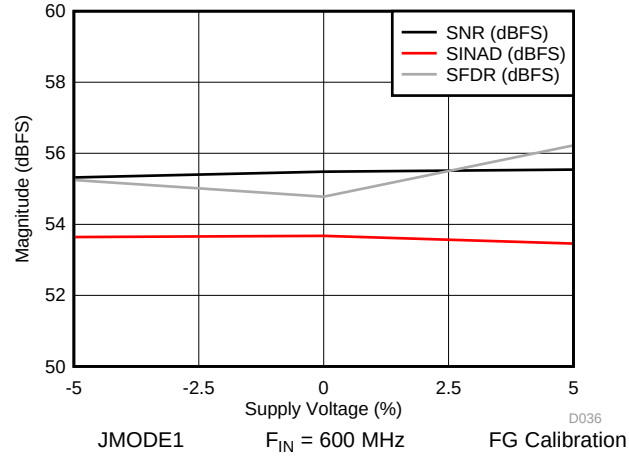


Figure 32. SNR SINAD SFDR vs Supply Voltage

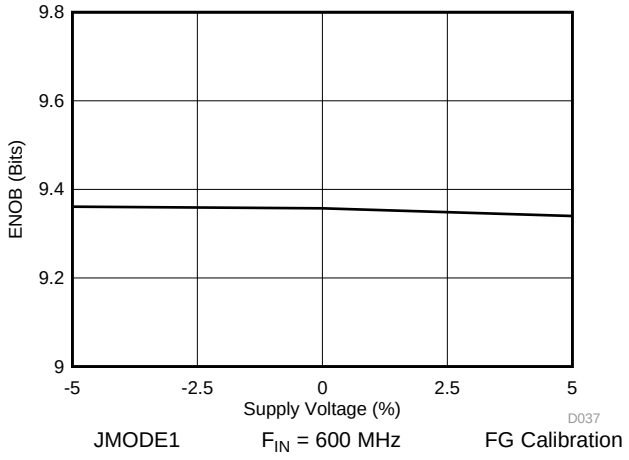


Figure 33. ENOB vs Supply Voltage

Typical Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.

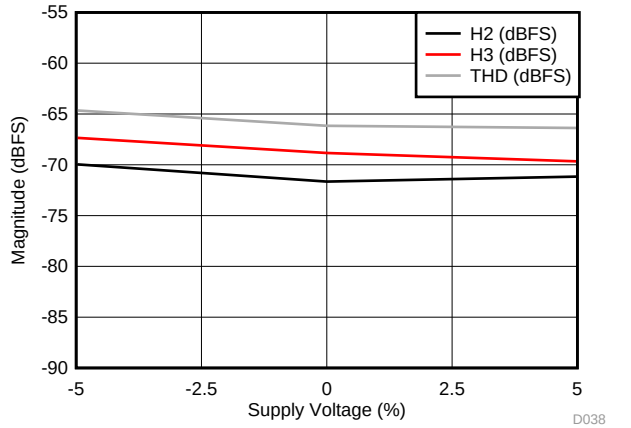


Figure 34. H2, H3, THD vs Supply Voltage

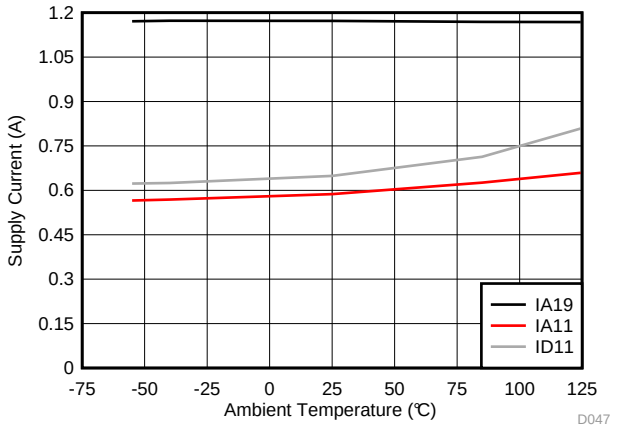


Figure 35. Supply Current vs Temperature

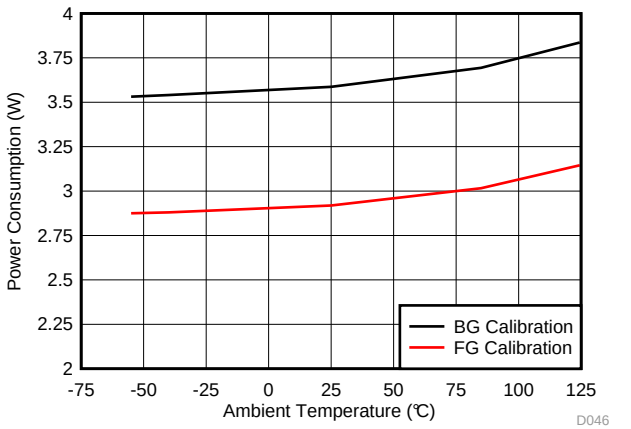


Figure 36. Power Consumption vs Temperature

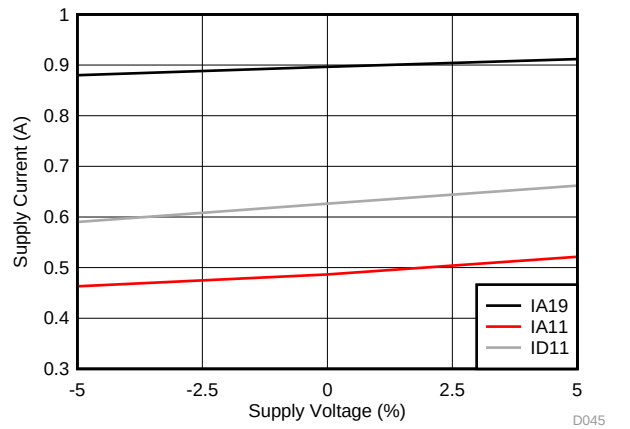


Figure 37. Supply Current vs Supply Voltage

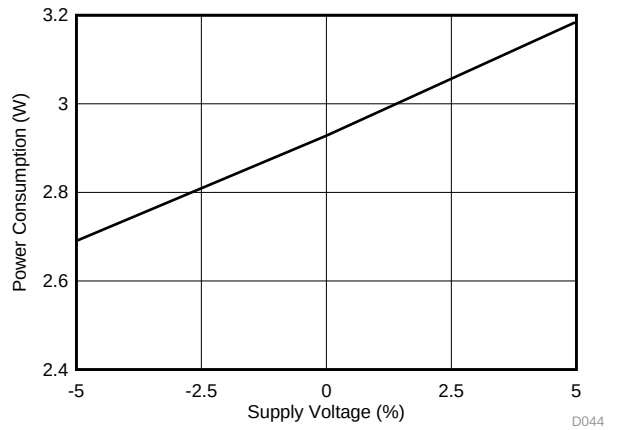


Figure 38. Power Consumption vs Supply Voltage

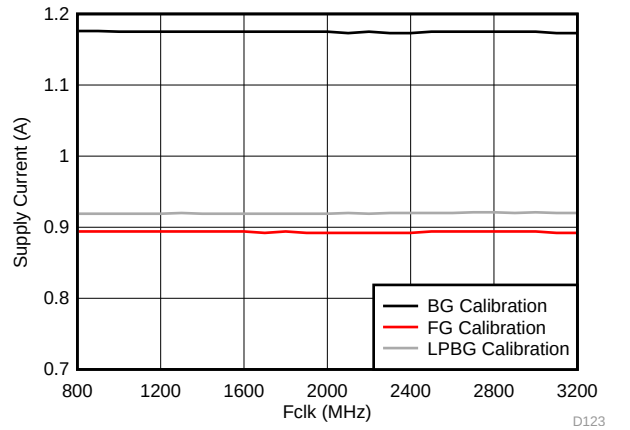
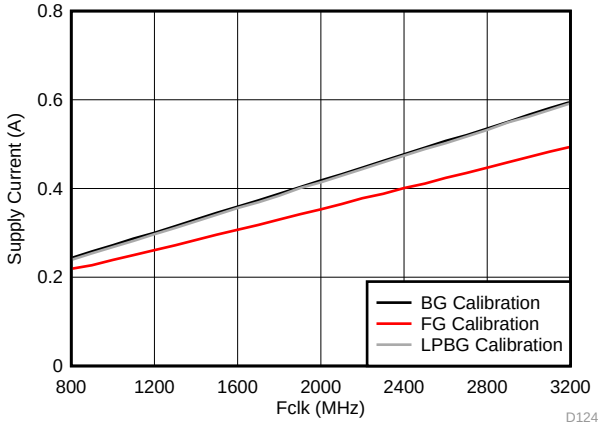


Figure 39. IA19 vs Clock Frequency

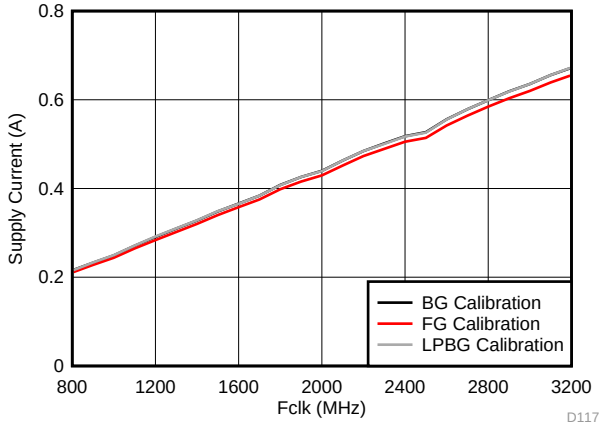
Typical Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.



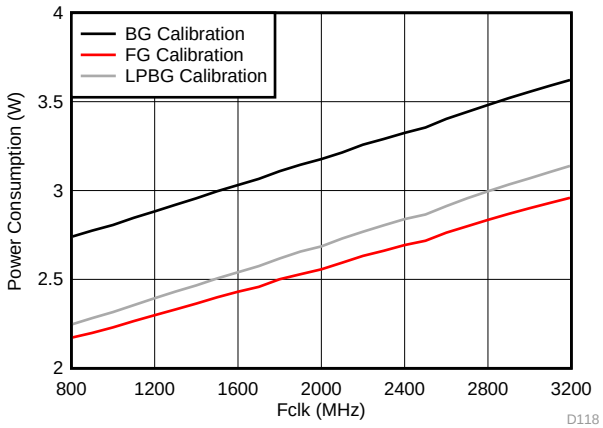
JMODE0 F_{IN} = 607 MHz

Figure 40. IA11 vs Clock Frequency



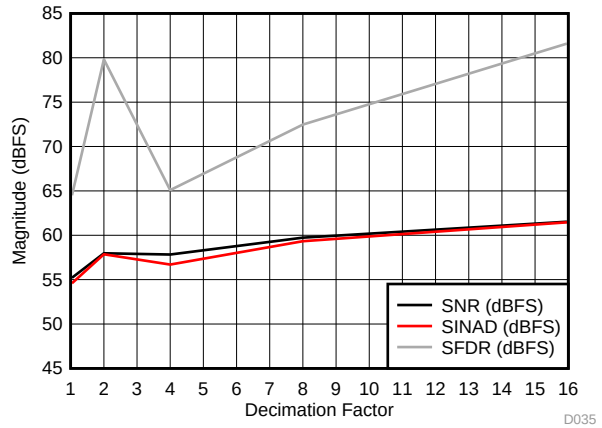
JMODE0 F_{IN} = 607 MHz

Figure 41. ID11 vs Clock Frequency



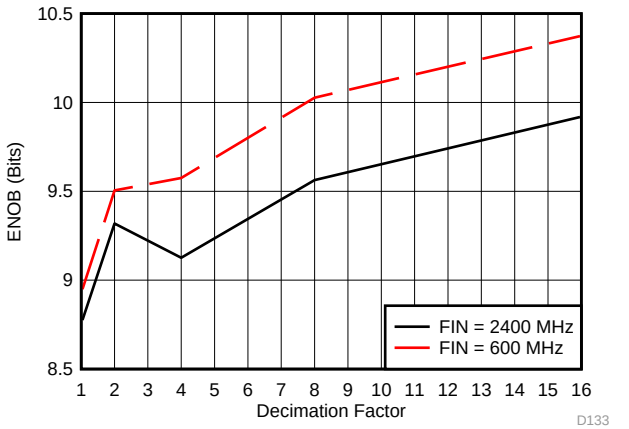
JMODE0 F_{IN} = 607 MHz

Figure 42. Power Consumption vs Clock Frequency



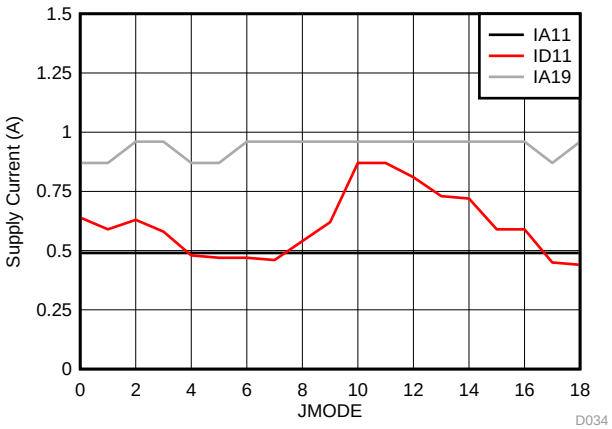
F_{CLK} = 3200 MHz F_{IN} = 2400 MHz FG Calibration

Figure 43. SNR, SINAD, SFDR vs DECIMATION FACTOR



F_{CLK} = 3200 MHz FG Calibration

Figure 44. ENOB vs DECIMATION FACTOR

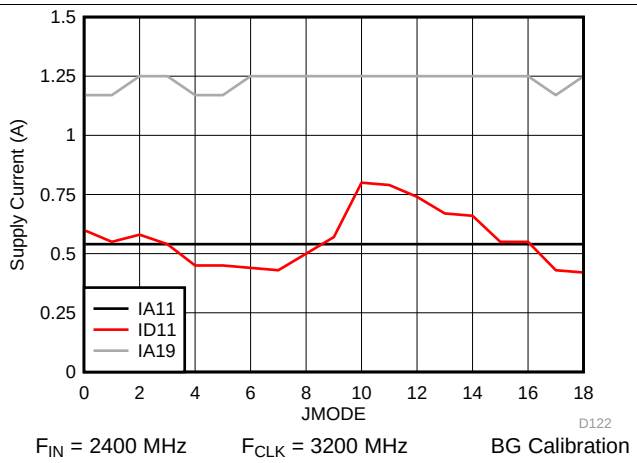


F_{IN} = 2400 MHz F_{CLK} = 3200 MHz FG Calibration

Figure 45. Supply Current vs JMODE

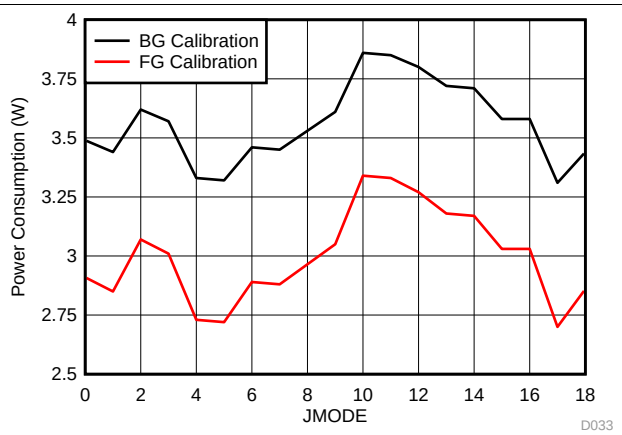
Typical Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.



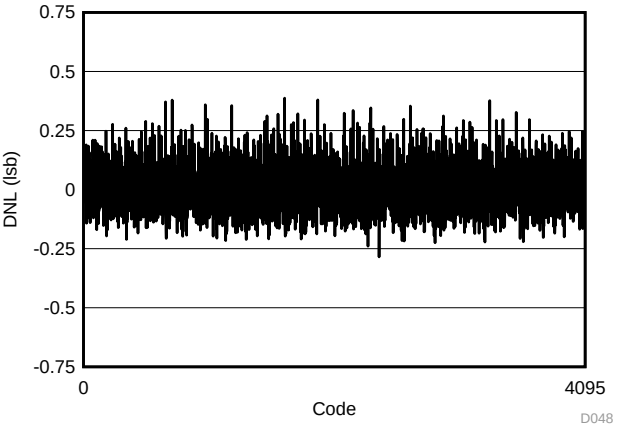
F_{IN} = 2400 MHz F_{CLK} = 3200 MHz BG Calibration

Figure 46. Supply Current vs JMODE



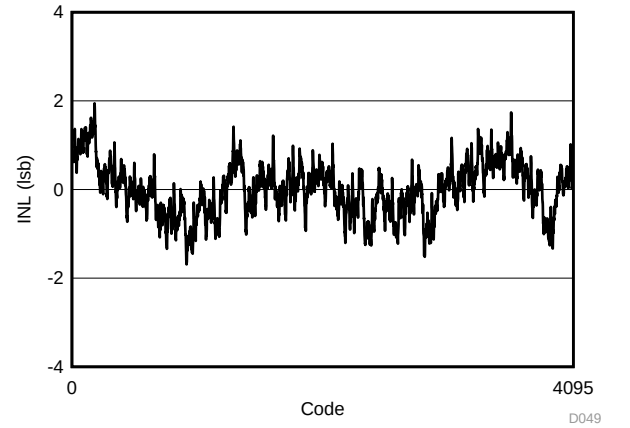
F_{IN} = 2400 MHz F_{CLK} = 3200 MHz

Figure 47. Power Consumption vs JMODE



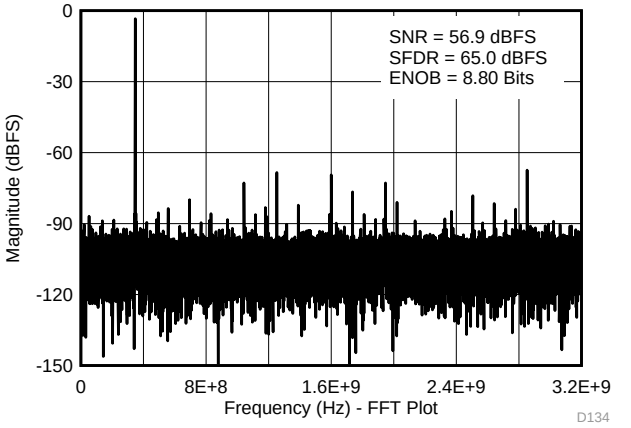
JMODE1 F_{CLK} = 3200 MHz FG Calibration

Figure 48. DNL vs Code



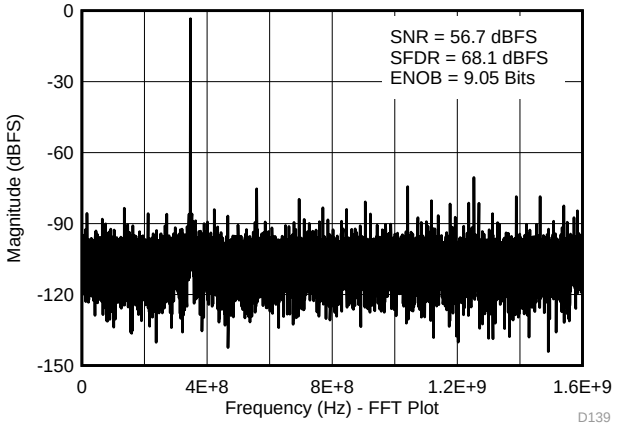
JMODE1 F_{CLK} = 3200 MHz FG Calibration

Figure 49. INL vs Code



JMODE1 F_{IN} = 350 MHz FG Calibration

Figure 50. Single Tone FFT at A_{IN} = -1dBFS



JMODE3 F_{IN} = 350 MHz FG Calibration

Figure 51. Single Tone FFT at A_{IN} = -1 dBFS

Typical Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.

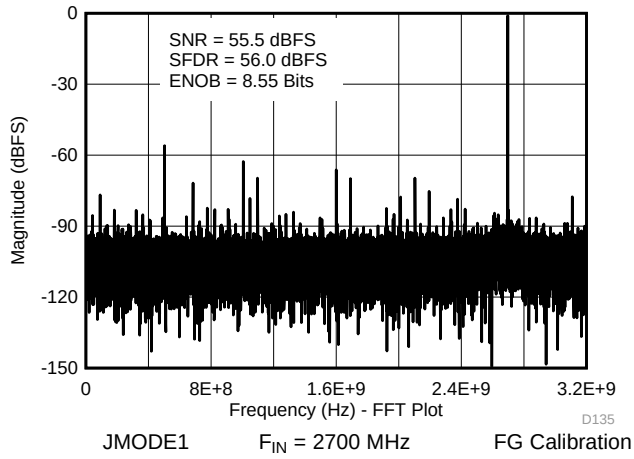


Figure 52. Single Tone FFT at A_{IN} = -1 dBFS

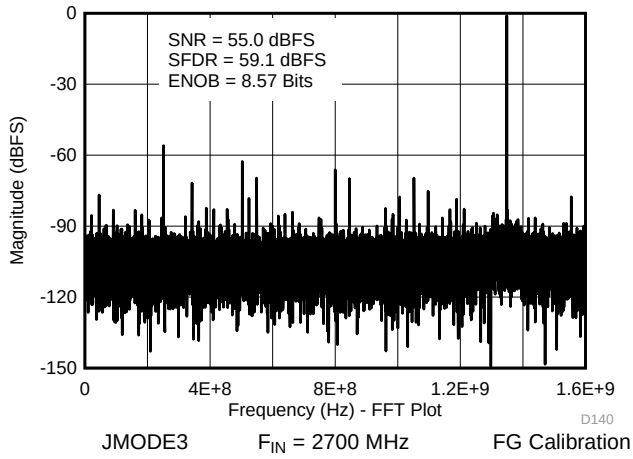


Figure 53. Single Tone FFT at A_{IN} = -1 dBFS

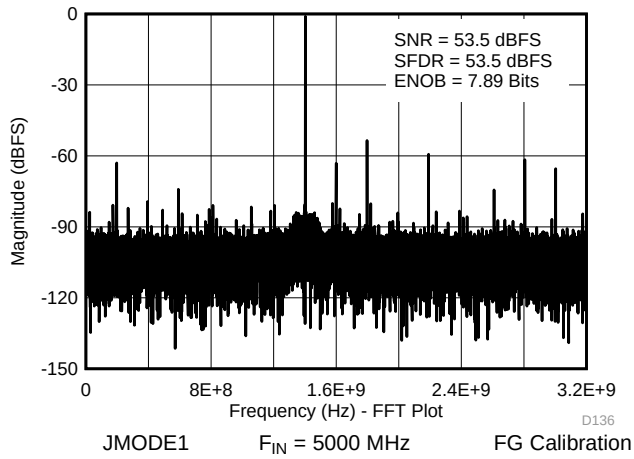


Figure 54. Single Tone FFT at A_{IN} = -1 dBFS

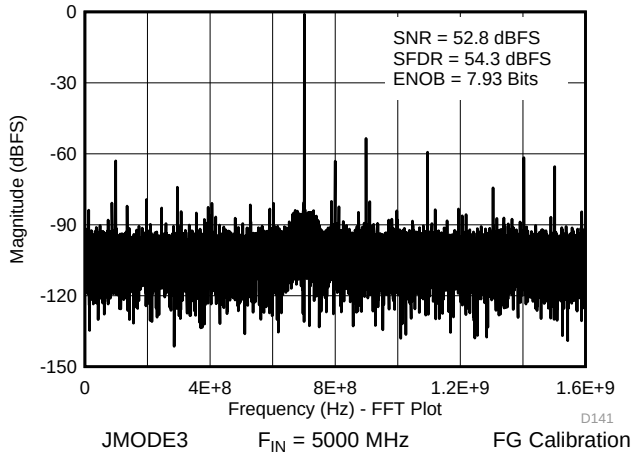


Figure 55. Single Tone FFT at A_{IN} = -1 dBFS

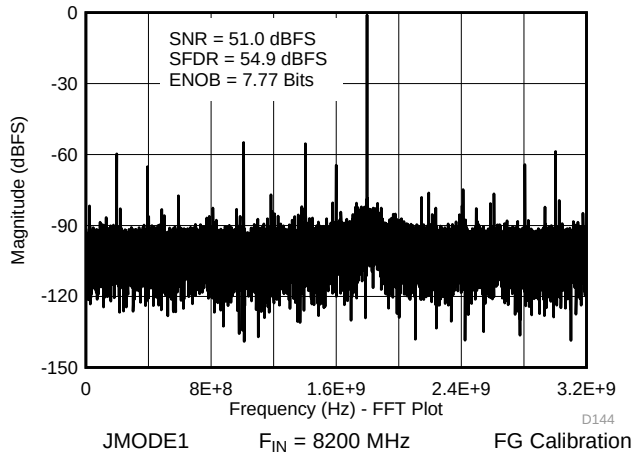


Figure 56. Single Tone FFT at A_{IN} = -1 dBFS

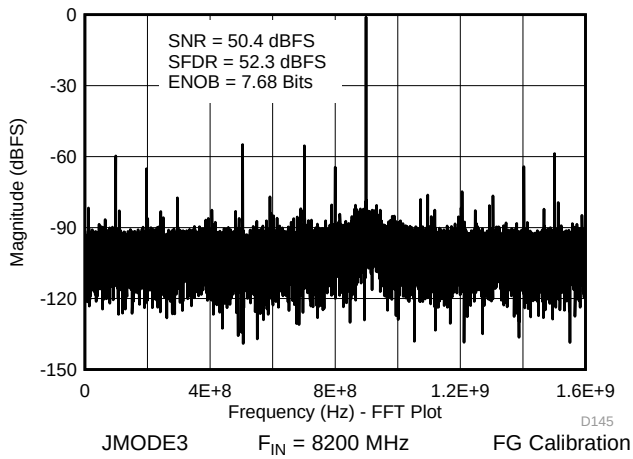
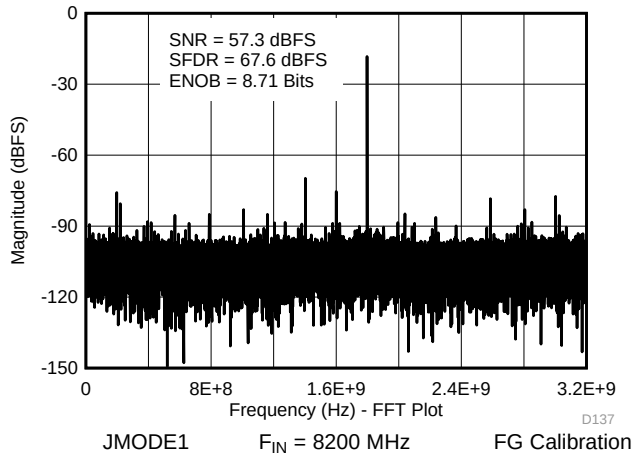


Figure 57. Single Tone FFT at A_{IN} = -1 dBFS

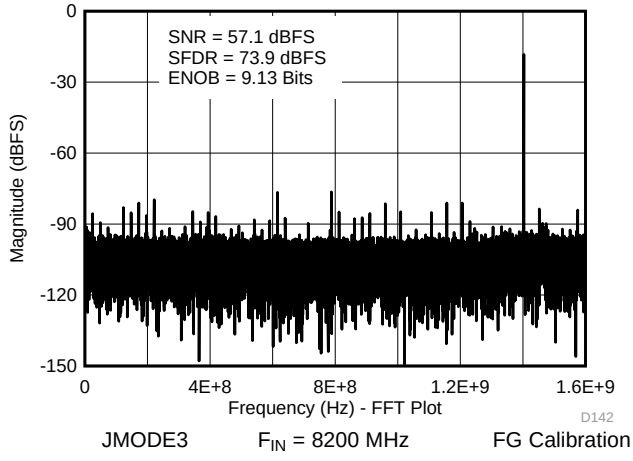
Typical Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.



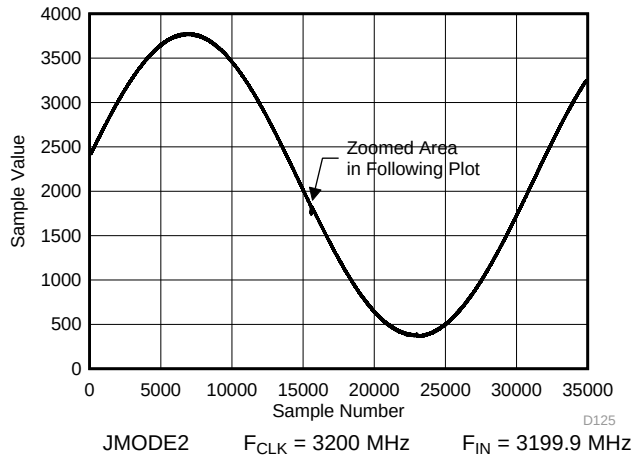
JMODE1 F_{IN} = 8200 MHz FG Calibration

Figure 58. Single Tone FFT at A_{IN} = -16 dBFS



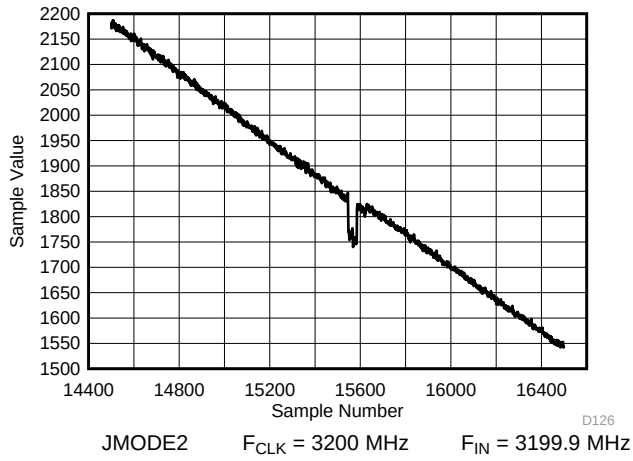
JMODE3 F_{IN} = 8200 MHz FG Calibration

Figure 59. Single Tone FFT at A_{IN} = -16 dBFS



JMODE2 F_{CLK} = 3200 MHz F_{IN} = 3199.9 MHz

Figure 60. Background Calibration Core Transition - AC Signal



JMODE2 F_{CLK} = 3200 MHz F_{IN} = 3199.9 MHz

Figure 61. Background Calibration Core Transition - AC Signal Zoomed

Typical Characteristics (continued)

Typical values at T_A = +25°C, VA19 = 1.9V, VA11 = VD11 = 1.1V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA+/- in single channel modes, f_{IN} = 347 MHz, A_{IN} = -1dBFS, f_{CLK} = maximum rated clock frequency, filtered, 1-Vpp sine-wave clock, JMODE=1, background calibration, unless otherwise noted. SNR results exclude DC, HD2 to HD9 and interleaving spurs. SINAD, ENOB and SFDR results exclude DC and fixed frequency interleaving spurs.

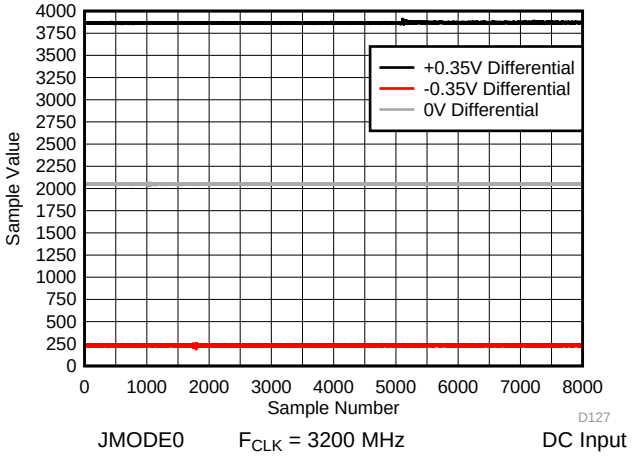


Figure 62. Background Calibration Core Transition - DC Signal

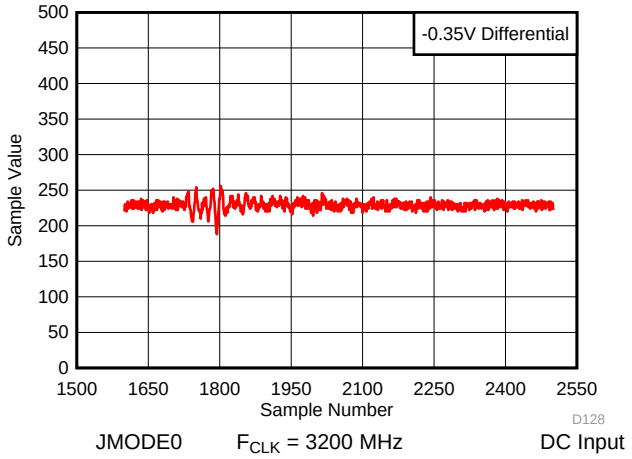


Figure 63. Background Calibration Core Transition - DC Signal Zoomed

7 Detailed Description

7.1 Overview

ADC12DJ3200 is an RF-sampling giga-sample ADC that can directly sample input frequencies from DC to above 10 GHz. In dual channel mode, ADC12DJ3200 can sample up to 3200-MSPS and in single channel mode up to 6400-MSPS. Programmable tradeoffs in channel count (dual channel mode) and Nyquist bandwidth (single channel mode) allow development of flexible hardware that meets the needs of both high channel count or wide instantaneous signal bandwidth applications. Full power input bandwidth (-3 dB) of 8.0 GHz, with usable frequencies exceeding the -3 dB point in both dual and single channel modes, allows direct RF sampling of L-band, S-band, C-band and X-band for frequency agile systems.

Time interleaving is achieved internally through 4 active cores. In dual channel mode, two cores are interleaved per channel to increase the sample rate to 2x the core sample rate. In single channel mode, all 4 cores are time interleaved to increase the sample rate to 4x the core sample rate. Either input can be used in single channel mode, however performance has been optimized for INA+/–. The user provides a clock at 2x the ADC core sample rate and the generation of the clocks for the interleaved cores is done internally for both single channel mode and dual channel mode. ADC12DJ3200 also provides foreground and background calibration options to match the gain and offset between cores to minimize spurious artifacts due to the interleaving.

ADC12DJ3200 uses a high speed JESD204B output interface with up to 16 serialized lanes and subclass-1 compliance for deterministic latency and multi-device synchronization. The serial output lanes support up to 12.8 Gbps and can be configured to trade-off bit rate and number of lanes. Innovative synchronization features, including noiseless aperture delay (T_{AD}) adjustment and SYSREF windowing, simplify system design for phased array radar and MIMO communications. Optional digital down converters (DDCs) in dual channel mode allow for reduction in interface rate (real and complex decimation modes) and digital mixing of the signal (complex decimation modes only).

7.2 Functional Block Diagrams

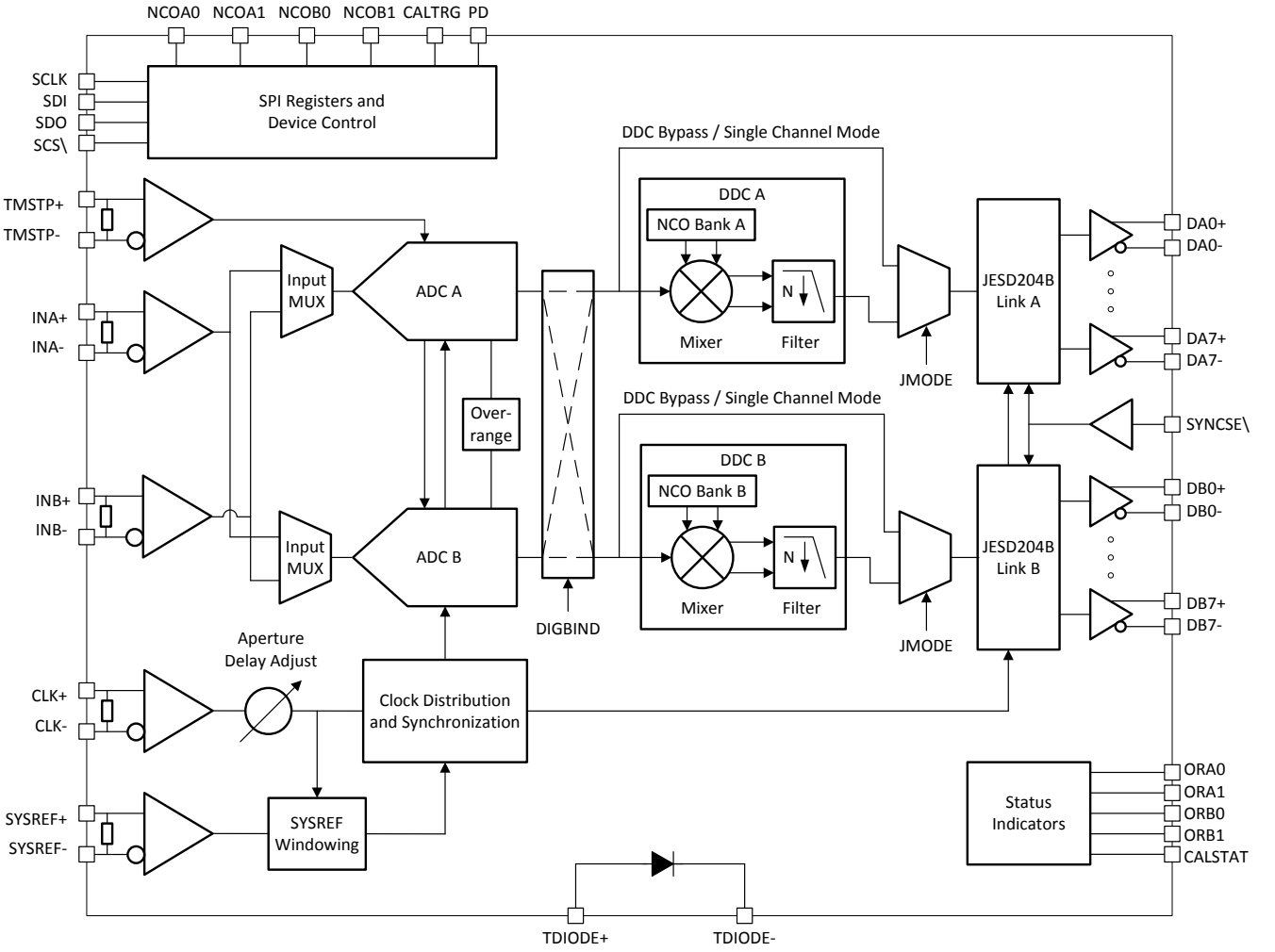


Figure 64. ADC12DJ3200 Functional Block Diagram

7.3 Feature Description

7.3.1 Analog Inputs

The analog inputs of ADC12DJ3200 have internal buffers to enable high input bandwidth and isolate sampling capacitor glitch noise from the input circuit. Analog inputs must be driven differentially since operation with a single-ended signal results in degraded performance. Both AC coupling and DC coupling of the analog inputs is supported. The analog inputs are designed for an input common mode voltage (V_{CMI}) of 0 V which is terminated internally through single-ended 50-Ω resistors to ground (GND) on each input pin. DC-coupled input signals must have a common mode voltage that meets the device input common mode requirements specified as V_{CMI} in *Recommended Operating Conditions*. The 0-V input common mode voltage simplifies the interface to split-supply fully differential amplifiers and to a variety of transformers and baluns. ADC12DJ3200 includes internal analog input protection to protect the ADC inputs during over-ranged input conditions (see Analog Input Protection). A simplified analog input model is shown in Figure 65.

Feature Description (continued)

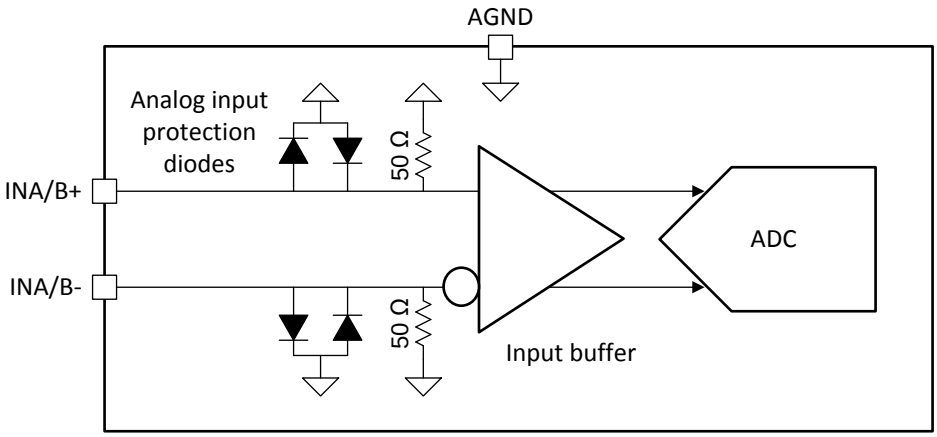


Figure 65. ADC12DJ3200 Analog Input Internal Termination and Protection

There is minimal degradation in analog input bandwidth when using single channel mode versus dual channel mode. In single channel mode it is strongly recommended that INA+/– be used as the input to the ADC since ADC performance has been optimized for INA+/–. However, either analog input (INA+ and INA– or INB+ and INB–) can be used. The use of INB+/– will result in degraded performance unless custom trim routines are used to optimize performance for INB+/– for each device. The desired input can be chosen using SINGLE_INPUT in *Input Mux Control Register (address = 0x060) [reset = 0x01]*.

NOTE

In single channel mode it is strongly recommended that INA+/– be used as the input to the ADC for optimized performance.

7.3.1.1 Analog Input Protection

The analog inputs are protected against over-drive conditions by internal clamping diodes that are capable of sourcing or sinking input currents during over-range conditions, see voltage and current limits in Absolute Maximum Ratings. The over-range protection is also defined for a peak RF input power in Absolute Maximum Ratings, which is frequency independent. Operation above the maximum conditions listed in Recommended Operating Conditions will result in an increase in failure-in-time (FIT) rate, so the system should correct the over-drive condition as quickly as possible. The analog input protection diodes are shown in Figure 65.

7.3.1.2 Full-Scale Voltage (V_{FS}) Adjustment

Input full-scale voltage (V_{FS}) adjustment is available, in fine increments, for each analog input through the FS_RANGE_A (*INA Full Scale Range Adjust Register (address = 0x030-0x031) [reset = 0xA000]*) register setting and FS_RANGE_B (*INB Full Scale Range Adjust Register (address = 0x032-0x033) [reset = 0xA000]*) register setting for INA+/– and INB+/–, respectively. The available adjustment range is specified in Electrical Characteristics - DC Specifications. Larger full-scale voltages improve SNR and noise floor (in dBFS/Hz) performance, but may degrade harmonic distortion. The full-scale voltage adjustment is useful for matching the full-scale range of multiple ADCs when developing a multi-converter system or for external interleaving of multiple ADC12DJ3200 to achieve higher sampling rates.

7.3.1.3 Analog Input Offset Adjust

The input offset voltage for each input can be adjusted through the OADJ_x_INy registers (registers 0x08A and 0x095), where x represents the ADC core (A, B, or C) and y represents the analog input (INA+/– or INB+/–). The adjustment range is approximately 28 mV to –28 mV differential. See Calibration Modes and Trimming for more information.

Feature Description (continued)

7.3.2 ADC Core

ADC12DJ3200 consists of a total of six ADC cores. The cores are interleaved for higher sampling rates and swapped on-the-fly for calibration as required by the operating mode. This section highlights the theory and key features of the ADC cores.

7.3.2.1 ADC Theory of Operation

The differential voltages at the analog inputs are captured by the rising edge of CLK+/– in dual channel mode or by the rising and falling edges of CLK+/– in single channel mode. After capturing the input signal, the ADC converts the analog voltage to a digital value by comparing the voltage to the internal reference voltage. If the voltage on INA– or INB– is higher than the voltage on INA+ or INB+, respectively, then the digital output will be a negative 2's complement value. If the voltage on INA+ or INB+ is higher than the voltage on INA– or INB–, respectively, then the digital output will be a positive 2's complement value. The differential voltage at the input pins can be calculated from the digital output by Equation 1 where Code is the signed decimation output code (e.g. –2048 to +2047), N is the ADC resolution and V_{FS} is the full-scale input voltage of the ADC as specified in Recommended Operating Conditions, including any adjustment performed by programming FS_RANGE_A or FS_RANGE_B.

$$V_{IN} = \frac{Code}{2^N} V_{FS} \quad (1)$$

7.3.2.2 ADC Core Calibration

ADC core calibration is required to optimize analog performance of the ADC cores. Calibration must be repeated as operating conditions change significantly, namely temperature, in order to maintain optimal performance. The ADC12DJ3200 family has a built in calibration routine that can be run as a foreground operation or a background operation. Foreground operation requires ADC downtime, where the ADC is no longer sampling the input signal, to complete the process. Background calibration can be used to overcome this limitation and allow constant operation of the ADC. See Calibration Modes and Trimming for detailed information on each mode.

7.3.2.3 ADC Over-Range Detection

To ensure that system gain management has the quickest-possible response time, a low-latency configurable over-range function is included. The over-range function works by monitoring the converted 12-bit samples at the ADC to quickly detect if the ADC is near saturation or already in an over-range condition. The absolute value of the upper 8 bits of the ADC data are checked against two programmable thresholds, OVR_T0 and OVR_T1. These thresholds apply to both channel A and channel B in dual channel mode. The following table lists how an ADC sample is converted to an absolute value for a comparison of the thresholds.

Table 1. Conversion of ADC Sample for Over-Range Comparison

ADC SAMPLE (OFFSET BINARY)	ADC SAMPLE (2's COMPLEMENT)	ABSOLUTE VALUE	UPPER 8 BITS USED FOR COMPARISON
1111 1111 1111 (4095)	0111 1111 1111 (+2047)	111 1111 1111 (2047)	1111 1111 (255)
1111 1111 0000 (4080)	0111 1111 0000 (+2032)	111 1111 0000 (2032)	1111 1110 (254)
1000 0000 0000 (2048)	0000 0000 0000 (0)	000 0000 0000 (0)	0000 0000 (0)
0000 0001 0000 (16)	1000 0001 0000 (–2032)	111 1111 0000 (2032)	1111 1110 (254)
0000 0000 0000 (0)	1000 0000 0000 (–2048)	111 1111 1111 (2047)	1111 1111 (255)

If the upper 8 bits of the absolute value equal or exceed the OVR_T0 or OVR_T1 thresholds during the monitoring period, then the over-range bit associated with the threshold is set to 1, otherwise the over-range bit is 0. In dual channel mode the over-range status can be monitored on the ORA0 and ORA1 pins for channel A and ORB0 and ORB1 pins for channel B, where ORx0 corresponds to the OVR_T0 threshold and ORx1 corresponds to the OVR_T1 threshold. In single channel mode the over-range status for threshold OVR_T0 is determined by monitoring both ORA0 and ORB0 outputs while the OVR_T1 threshold is determined by monitoring both ORA1 and ORB1 outputs. In single channel mode the two outputs for each threshold should be OR'd together to determine whether an over-range condition occurred. OVR_N can be used to set the output pulse duration from the last over-range event. Table 2 lists the over-range pulse lengths for the various OVR_N settings (*Over-range Configuration Register (address = 0x213) [reset = 0x07]*). In decimation modes (only in the

JMODEs where CS = 1 in Table 18), the over-range status is also embedded into the output data samples. For complex decimation modes the OVR_T0 threshold status is embedded as the LSB along with the upper 15 bits of every complex I sample and OVR_T1 threshold status is embedded as the LSB along with the upper 15 bits of every complex Q sample. For real decimation modes the OVR_T0 threshold status is embedded as the LSB of every even numbered sample and OVR_T1 threshold status is embedded as the LSB of every odd numbered sample. Table 3 lists the outputs, related data samples, threshold settings and the monitoring period equation. The embedded over-range bit will go high if the associated channel has exceeded the associated over-range threshold within the monitoring period set by OVR_N. The monitoring period can be calculated as shown in Table 3..

Table 2. Over-Range Monitoring Period for ORA0, ORA1, ORB0 and ORB1 Outputs

OVR_N	OVER-RANGE PULSE LENGTH SINCE LAST OVER-RANGE EVENT (DEVCLK CYCLES)
0	8
1	16
2	32
3	64
4	128
5	256
6	512
7	1024

Table 3. Threshold and Monitoring Period for Embedded Over-Range Indicators in Dual Channel Decimation Modes

OVER-RANGE INDICATOR	ASSOCIATED THRESHOLD	DECIMATION TYPE	OVER-RANGE STATUS EMBEDDED IN	MONITORING PERIOD (ADC SAMPLES)
ORA0	OVR_T0	Real Decimation (JMODE 9)	Channel A even numbered samples	2^{OVR_N+1} (1)
		Complex Down-Conversion (JMODE 10-16, except JMODE 12)	Channel A In-Phase (I) samples	2^{OVR_N} (1)
ORA1	OVR_T1	Real Decimation (JMODE 9)	Channel A odd numbered samples	2^{OVR_N+1} (1)
		Complex Down-Conversion (JMODE 10-16, except JMODE 12)	Channel A Quadrature (Q) samples	2^{OVR_N} (1)
ORB0	OVR_T0	Real Decimation (JMODE 9)	Channel B even numbered samples	2^{OVR_N+1} (1)
		Complex Down-Conversion (JMODE 10-16, except JMODE 12)	Channel B In-Phase (I) samples	2^{OVR_N} (1)
ORB1	OVR_T1	Real Decimation (JMODE 9)	Channel B odd numbered samples	2^{OVR_N+1} (1)
		Complex Down-Conversion (JMODE 10-16, except JMODE 12)	Channel B Quadrature (Q) samples	2^{OVR_N} (1)

(1) OVR_N is the monitoring period register setting.

Typically, the OVR_T0 threshold can be set near the full-scale value (228 for example). When the threshold is triggered, a typical system can turn down the system gain to avoid clipping. The OVR_T1 threshold can be set much lower. For example, the OVR_T1 threshold can be set to 64 (peak input voltage of −12 dBFS). If the input signal is strong, the OVR_T1 threshold is tripped occasionally. If the input is quite weak, the threshold is never tripped. The downstream logic device monitors the OVR_T1 bit. If OVR_T1 stays low for an extended period of time, then the system gain can be increased until the threshold is occasionally tripped (meaning the peak level of the signal is above −12 dBFS).

7.3.2.4 Code Error Rate (CER)

ADC cores can generate bit errors within a sample, often called code errors (CER) or referred to as sparkle codes, due to metastability caused by non-ideal comparator limitations. The ADC12DJ3200 uses a unique ADC architecture that inherently allows significant code error rate improvements from traditional pipelined flash or successive approximation register (SAR) ADCs. The code error rate of the ADC12DJ3200 is multiple orders of magnitude better than what can be achieved in alternative architectures at equivalent sampling rates providing significant signal reliability improvements.

7.3.3 Timestamp

TMSTP+ and TMSTP– differential input can be used as a time-stamp input to mark a specific sample based on the timing of an external trigger event relative to the sampled signal. TIMESTAMP_EN (*LSB Control Bit Output Register (address = 0x160) [reset = 0x00]*) must be set in order to use the timestamp feature and output the timestamp data. When enabled, the LSB of the 12-bit ADC digital output reports the status of the TMSTP+/– input. In effect, the 12-bit output sample consists of the upper 11-bits of the 12-bit converter and the LSB of the 12-bit output sample is the output of a parallel 1-bit converter (TMSTP+/–)with the same latency as the ADC core. In the 8-bit operating modes, the LSB of the 8-bit output sample is used to output the timestamp status. The trigger must be applied to the differential TMSTP+ and TMSTP– inputs. The trigger can be asynchronous to the ADC sampling clock and is sampled at approximately the same time as the analog input. Timestamp cannot be used when a JMODE with decimation is selected and instead SYSREF should be used to achieve synchronization through JESD204B's subclass-1 method for achieving deterministic latency.

7.3.4 Clocking

The clocking subsystem of ADC12DJ3200 has two input signals, device clock (CLK+, CLK–) and SYSREF (SYSREF+, SYSREF–). Within the clocking subsystem there is a noiseless aperture delay adjustment (t_{AD} Adjust), a clock duty cycle corrector and a SYSREF capture block. The clocking subsystem is shown in Figure 66.

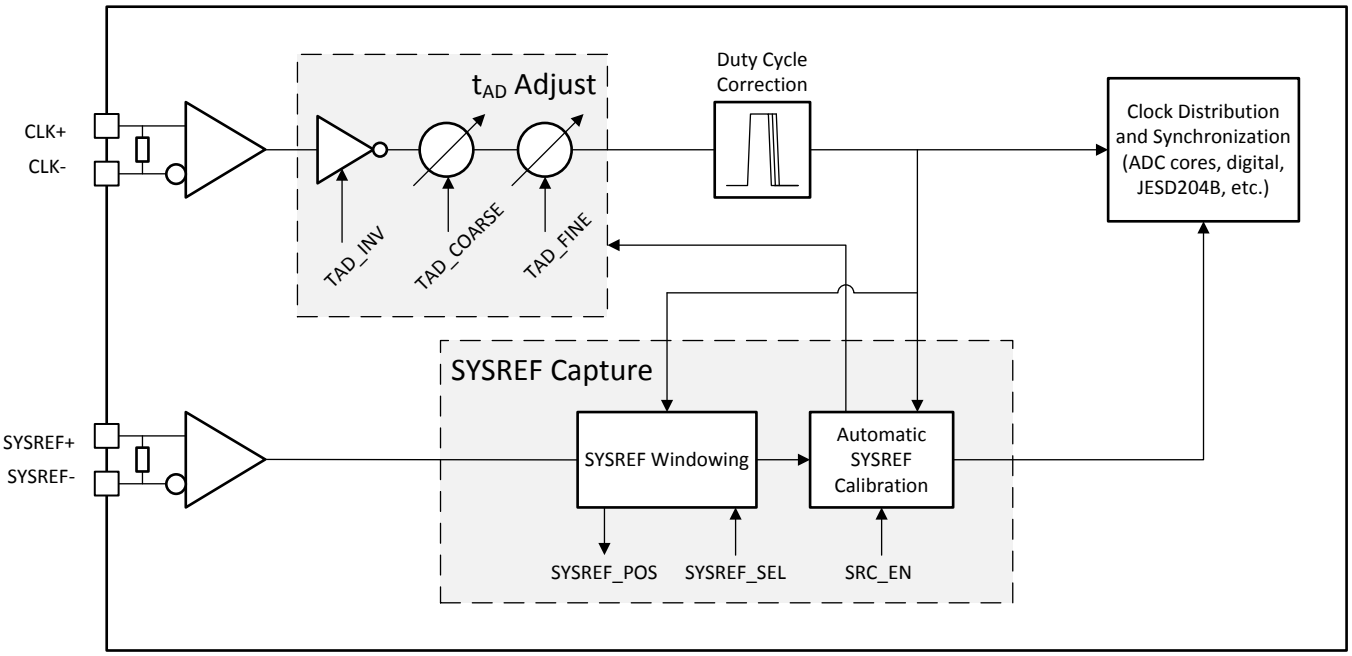


Figure 66. ADC12DJ3200 Clocking Subsystem

The device clock is used as the sampling clock for the ADC core as well as the clocking for the digital processing and serializer outputs. A low noise (low jitter) device clock should be used to maintain high signal-to-noise ratio (SNR) within the ADC. In dual channel mode the analog input signal for each input is sampled on the rising edge of the device clock. In single channel mode both the rising and falling edge of the device clock are used to capture the analog signal to reduce the max clock rate required by the ADC. A noiseless aperture delay adjustment (t_{AD} Adjust) allows the user to shift the sampling instance of the ADC in fine steps in order to synchronize multiple ADC12DJ3200 or to fine tune system latency. Duty cycle correction is implemented in ADC12DJ3200 to ease the requirements on the external device clock while maintaining high performance. Table 4 summarizes the device clock interface in dual channel mode and single channel mode.

Table 4. Device Clock vs. Mode of Operation

Mode of Operation	Sampling Rate vs. F_{CLK}	Sampling Instant
Dual channel mode	1 x F_{CLK}	Rising edge
Single channel mode	2 x F_{CLK}	Rising and falling edge

SYSREF is a system timing reference used for JESD204B subclass-1 implementations of deterministic latency. SYSREF is used to achieve deterministic latency and for multi-device synchronization. SYSREF must be captured by the correct device clock edge in order to achieve repeatable latency and synchronization. ADC12DJ3200 includes SYSREF Windowing and Automatic SYSREF Calibration to ease the requirements on the external clocking circuits and simplify the synchronization process. SYSREF can be implemented as a single pulse or as a periodic clock. In periodic implementations, SYSREF must be equal to, or an integer division of, the local multi-frame clock frequency. Valid SYSREF frequencies can be calculated using Equation 2 where R and F are set by the JMODE setting (see Table 18), f_{CLK} is the device clock frequency (CLK+/–), K is the programmed multi-frame length (see Table 18 for valid K settings) and n is any positive integer.

$$f_{SYSREF} = \frac{R \times f_{CLK}}{10 \times F \times K \times n} \tag{2}$$

7.3.4.1 Noiseless Aperture Delay Adjustment (t_{AD} Adjust)

ADC12DJ3200 contains a delay adjustment on the device clock (sampling clock) input path, called t_{AD} Adjust, that can be used to shift the sampling instance within the device in order to align sampling instances among multiple devices or for external interleaving of multiple ADC12DJ3200. Further, t_{AD} Adjust can be used for automatic SYSREF calibration to simplify synchronization (Automatic SYSREF Calibration). Aperture delay adjustment is implemented in a way that adds no additional noise to the clock path, however a slight degradation in aperture jitter (t_{AJ}) is possible at large values of TAD_COARSE due to internal clock path attenuation. The degradation in aperture jitter may result in minor SNR degradations at high input frequencies (see t_{AJ} in Switching Characteristics). The feature is programmed using TAD_INV, TAD_COARSE and TAD_FINE in *DEVCLK Aperture Delay Adjustment Register (address = 0x2B5 to 0x2B7) [reset = 0x000000]*. Setting TAD_INV inverts the input clock resulting in a delay equal to half the clock period. TAD_COARSE and TAD_FINE are variable analog delays with step sizes and ranges summarized in Table 5. All three delay options are independent and can be used in conjunction. All clocks within the device are shifted by the programmed t_{AD} Adjust amount, which results in a shift of the timing of the JESD204B serialized outputs and affects the capture of SYSREF.

Table 5. t_{AD} Adjust Adjustment Ranges

ADJUSTMENT PARAMETER	ADJUSTMENT STEP	DELAY SETTINGS	MAXIMUM DELAY
TAD_INV	1/(F_{CLK} * 2)	1	1/(F_{CLK} * 2)
TAD_COARSE	See $t_{TAD(STEP)}$ in Switching Characteristics	256	See $t_{TAD(MAX)}$ in Switching Characteristics
TAD_FINE	See $t_{TAD(STEP)}$ in Switching Characteristics	256	See $t_{TAD(MAX)}$ in Switching Characteristics

Please note that to maintain timing alignment between converters it is also important to provide stable and matched power supply voltages and device temperatures.

Aperture delay adjustment can be changed on-the-fly during normal operation but may result in brief upsets to the JESD204B data link. It is recommended to use TAD_RAMP to reduce the probability of the JESD204B link losing synchronization. See Aperture Delay Ramp Control (TAD_RAMP).

7.3.4.2 Aperture Delay Ramp Control (TAD_RAMP)

ADC12DJ3200 contains a function to gradually adjust the t_{AD} Adjust setting towards the newly written TAD_COARSE value. This will allow the t_{AD} Adjust setting to be adjusted with minimal glitching of the internal clock circuitry. The TAD_RAMP_RATE parameter allows either a slower (1 TAD_COARSE LSB per 256 t_{CLK} cycles) or faster ramp (4 TAD_COARSE LSBs per 256 t_{CLK} cycles) to be selected. The TAD_RAMP_EN parameter enables the ramp feature and any subsequent writes to TAD_COARSE initiate a new cramp.

7.3.4.3 SYSREF Capture for Multi-Device Synchronization and Deterministic Latency

The clocking subsystem is largely responsible for achieving multi-device synchronization and deterministic latency. ADC12DJ3200 uses the subclass-1 method of JESD204B to achieve deterministic latency and synchronization. Subclass 1 requires that the SYSREF signal be captured by a deterministic device clock (CLK+/-) edge at each system power on and at each device in the system. This requirement imposes setup and hold constraints on SYSREF relative to CLK+/- which can be difficult to meet at giga-sample clock rates over all system operating conditions. ADC12DJ3200 includes a number of features to simplify this synchronization process and relax system timing constraints.

- ADC12DJ3200 uses dual-edge sampling (DES) in single-channel mode to reduce the CLK+/- input frequency by half and double the timing window for SYSREF (see Table 4)
- A SYSREF position detector (relative to CLK+/-) and selectable SYSREF sampling position aid the user in meeting setup and hold times over all conditions (see SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing))
- Easy-to-use automatic SYSREF calibration uses the aperture timing adjust block (t_{AD} Adjust) to shift the ADC sampling instance based on the phase of SYSREF (rather than adjusting SYSREF based on the phase of the ADC sampling instance) (see Automatic SYSREF Calibration)

7.3.4.3.1 SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing)

The SYSREF windowing block is used to first detect the position of SYSREF relative to the CLK+/- rising edge and then to select a desired SYSREF sampling instance, which is a delay version of CLK+/-, to maximize setup and hold timing margins. In many cases a single SYSREF sampling position (SYSREF_SEL) is sufficient to meet timing for all systems (part-to-part variation) and conditions (temperature and voltage variations). However, the feature can also be used by the system to expand the timing window by tracking the movement of SYSREF as operating conditions change or to remove system-to-system variation at production test by finding a unique optimal value at nominal conditions for each system.

Use of the SYSREF windowing block is as follows. First, the device clock and SYSREF should be applied to the device. The location of SYSREF relative to the device clock cycle is determined and stored in SYSREF_POS in Figure 98. Each bit of SYSREF_POS represents a potential SYSREF sampling position. If a bit in SYSREF_POS is set to '1', then the corresponding SYSREF sampling position has a potential setup or hold violation. Upon determining the valid SYSREF sampling positions (the positions of SYSREF_POS that are set to '0') the desired sampling position can be chosen by setting SYSREF_SEL in Clock Control Register 0 (address = 0x029) [reset = 0x00] to the value corresponding to that SYSREF_POS position. In general the middle sampling position between two setup and hold instances should be chosen. Ideally, SYSREF_POS and SYSREF_SEL should be performed at the system's nominal operating conditions (temperature and supply voltage) to provide maximum margin for operating condition variations. This process can be performed at final test and the optimal SYSREF_SEL setting can be stored for use at every system power up. Further, SYSREF_POS can be used to characterize the skew between CLK+/– and SYSREF+/– over operating conditions for a system by sweeping the system temperature and supply voltages. For systems that have large variations in CLK+/– to SYSREF+/– skew this characterization can be used to track the optimal SYSREF sampling position as system operating conditions change. In general, a single value can be found that meets timing over all conditions for well matched systems, such as those where CLK+/– and SYSREF+/– come from a single clocking device.

NOTE

SYSREF_SEL should be set to '0' when using Automatic SYSREF Calibration (Automatic SYSREF Calibration).

The step size between each SYSREF_POS sampling position can be adjusted using SYSREF_ZOOM. When SYSREF_ZOOM is set to '0', the delay steps are more coarse. When SYSREF_ZOOM is set to '1', the delay steps finer steps. See Switching Characteristics for delay step sizes when SYSREF_ZOOM is enabled and disabled. In general, SYSREF_ZOOM should always be used (SYSREF_ZOOM = 1) unless a transition region (defined by 1's in SYSREF_POS) is not seen, such as could be the case for low clock rates. Bits 0 and 23 of SYSREF_POS will always be set to '1' since it cannot be determined if these settings are close to a timing violation, although the actual valid window could extend beyond these sampling positions. The value programmed into SYSREF_SEL is the decimal number representing the desired bit location in SYSREF_POS. Table 6 shows some example SYSREF_POS readings and the optimal SYSREF_SEL settings. Although 24 sampling positions are provided by the SYSREF_POS status register, SYSREF_SEL only allows selection of the first 16 sampling positions, corresponding to SYSREF_POS bits 0 to 15. The additional SYSREF_POS status bits are intended only to provide additional knowledge of the SYSREF valid window. In general, lower values of SYSREF_SEL should be selected due to variation of the delays over supply voltage, however in the fourth example a value of 15 provides additional margin and may be selected instead.

Table 6. Examples of SYSREF_POS Readings and SYSREF_SEL Selections

SYSREF_POS[23:0]			OPTIMAL SYSREF_SEL SETTING
0x02E[7:0] (Largest Delay)	0x02D[7:0]	0x02C[7:0] (Smallest Delay)	
b10000000	b01100000	b00011001	8 or 9
b10011000	b00000000	b00110001	12
b10000000	b01100000	b00000001	6 or 7
b10000000	b00000011	b00000001	4 or 15
b10001100	b01100011	b00011001	6

7.3.4.3.2 Automatic SYSREF Calibration

ADC12DJ3200 has an automatic SYSREF calibration feature to alleviate the often challenging setup and hold times associated with capturing SYSREF for giga-sample data converters. Automatic SYSREF Calibration uses the t_{AD} Adjust feature to shift the device clock to maximize the SYSREF setup and hold times or align the sampling instance based on the SYSREF rising edge.

ADC12DJ3200 must have a proper device clock applied and be programmed for normal operation before starting Automatic SYSREF Calibration. When ready to initiate Automatic SYSREF Calibration a continuous SYSREF signal should be applied. Note that SYSREF must be a continuous (periodic) signal when using Automatic SYSREF Calibration. Start the calibration process by setting SRC_EN high in Figure 173 after configuring Automatic SYSREF Calibration using the SRC_CFG register. Upon setting SRC_EN high ADC12DJ3200 searches for the optimal t_{AD} Adjust setting until the device clock falling edge is internally aligned to the SYSREF rising edge. TAD_DONE in Figure 175 can be monitored to ensure that SYSREF calibration has finished. By aligning the device clock falling edge with the SYSREF rising edge Automatic SYSREF Calibration maximizes the internal SYSREF setup and hold times relative to the device clock while also setting the sampling instant based on the SYSREF rising edge. After Automatic SYSREF Calibration finishes the rest of the startup procedure can be performed to finish bringing up the system.

For multi-device synchronization the timing of the SYSREF rising edge should be matched at all devices and therefore trace lengths should be matched from a common SYSREF source to each ADC12DJ3200. Any skew between the SYSREF rising edge at each device will result in additional error in the sampling instance between devices, however repeatable deterministic latency from system startup to startup through each device should still be achieved. No other design requirements are needed in order to achieve multi-device synchronization as long as a proper elastic buffer release point is chosen in the receiver.

A timing diagram of the SYSREF calibration procedure is shown in Figure 67. The optimized setup and hold times are shown as $t_{SU(OPT)}$ and $t_{H(OPT)}$, respectively. Device clock and SYSREF are referred to as "internal" in this diagram since the phase of the internal signals are aligned within the device and not to the external (applied) phase of device clock or SYSREF.

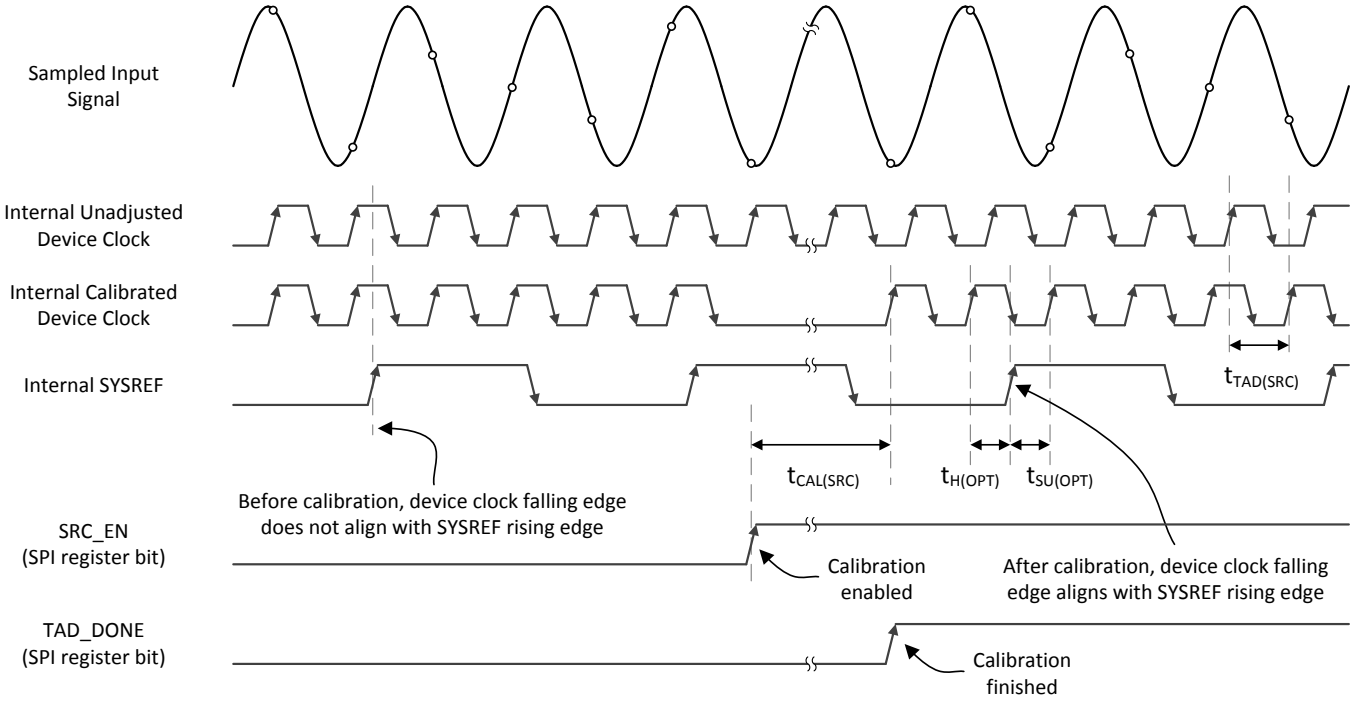


Figure 67. SYSREF Calibration Timing Diagram

Once finished, the t_{AD} Adjust setting found by Automatic SYSREF Calibration can be read from SRC_TAD in Figure 175. After calibration, the system will continue to use the calibrated t_{AD} Adjust setting for operation until the system is powered down. However, if desired, the user can then disable SYSREF calibration and fine-tune the t_{AD} Adjust setting according to the systems needs. Alternatively, the use of Automatic SYSREF Calibration can be done at product test (or periodic re-calibration) of the optimal t_{AD} Adjust setting for each system. This value can be stored and written to the TAD register (TAD_INV, TAD_COARSE and TAD_FINE) upon system startup.

SYSREF calibration should not be run while ADC calibration (foreground or background) is running. If background calibration is the desired use case, it should be disabled while SYSREF calibration is used, then reenabled after TAD_DONE goes high. SYSREF_SEL in Clock Control Register 0 (address = 0x029) [reset = 0x00] must be set to 0 when using SYSREF calibration.

SYSREF calibration will search the TAD_COARSE delays using both non-inverted (TAD_INV = 0) and inverted clock polarity (TAD_INV = 1) to minimize the required TAD_COARSE setting in order to minimize loss on the clock path to reduce aperture jitter (t_{AJ}).

7.3.5 Digital Down Converters (Dual Channel Mode Only)

After converting the analog voltage to a digital value, the digitized sample can either be sent directly to the JESD204B interface block (DDC bypass) or it can be sent to the digital down conversion (DDC) block for frequency conversion and decimation (in dual channel mode only). Frequency conversion and decimation allow a specific frequency band to be selected and output in the digital data stream while reducing the effective data rate and interface speed or width. The DDC is designed such that the digital processing does not degrade the noise spectral density (NSD) performance of the ADC. The digital down converter for channel A of the ADC12DJ3200 is shown in Figure 68. Channel B has the same structure with the input data selected by DIG_BIND_B and the NCO selection mux controlled by pins NCOB[1:0] or through CSELB[1:0].

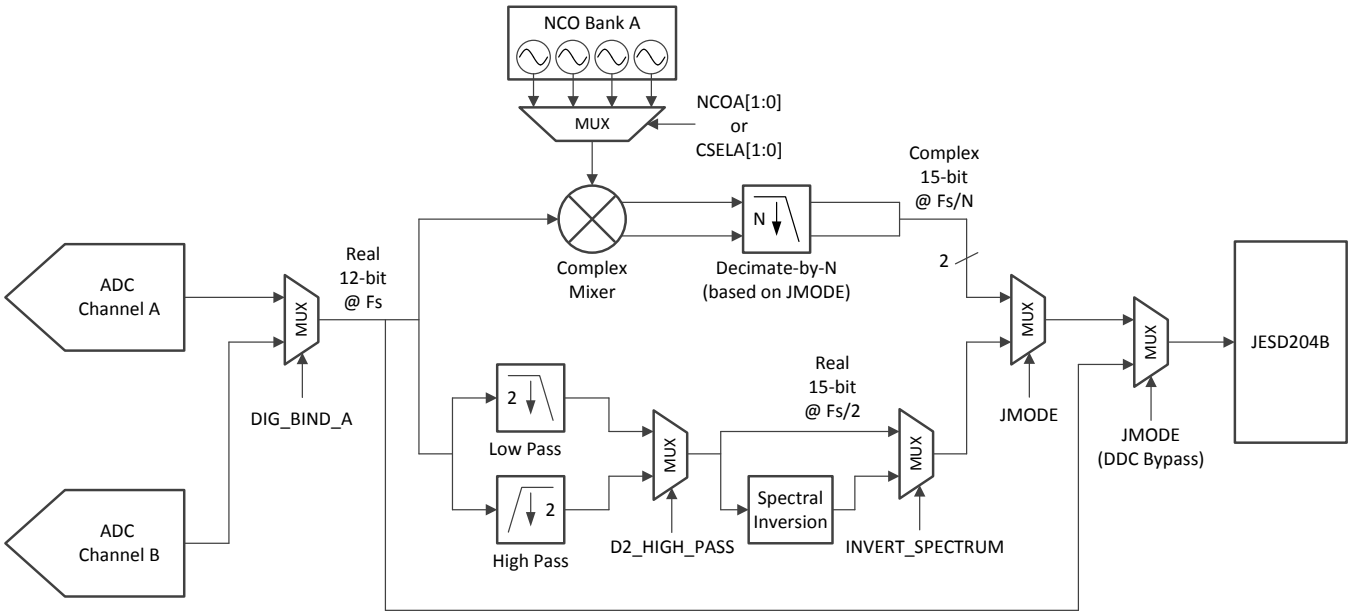


Figure 68. Channel A Digital Down Conversion Block (Dual Channel Mode Only)

7.3.5.1 Numerically Controlled Oscillator and Complex Mixer

The DDC contains a complex numerically-controlled oscillator (NCO) and a complex mixer. The oscillator generates a complex exponential sequence as shown in Equation 3.

$$x[n] = e^{j\omega n} \quad (3)$$

The frequency (ω) is specified by a 32-bit register setting. The complex exponential sequence is multiplied by the real input from the ADC to mix the desired carrier to a frequency equal to $f_{IN}+f_{NCO}$, where f_{IN} is the analog input frequency after aliasing (in undersampling systems) and f_{NCO} is the programmed NCO frequency.

7.3.5.1.1 NCO Fast Frequency Hopping (FFH)

Fast frequency hopping (FFH) is made possible by each DDC having four independent NCOs that can be controlled by the NCOA0 and NCOA1 pins for DDC A and NCOB0 and NCOB1 pins for DDC B. Each NCO has independent frequency settings (Basic NCO Frequency Setting Mode) and initial phase settings (NCO Phase Offset Setting) that can be set independently. Further, all NCOs have independent phase accumulators that continue to run when the specific NCO is not selected, allowing the NCOs to maintain their phase between selection so that downstream processing does not need to perform carrier recovery after each hop, for instance.

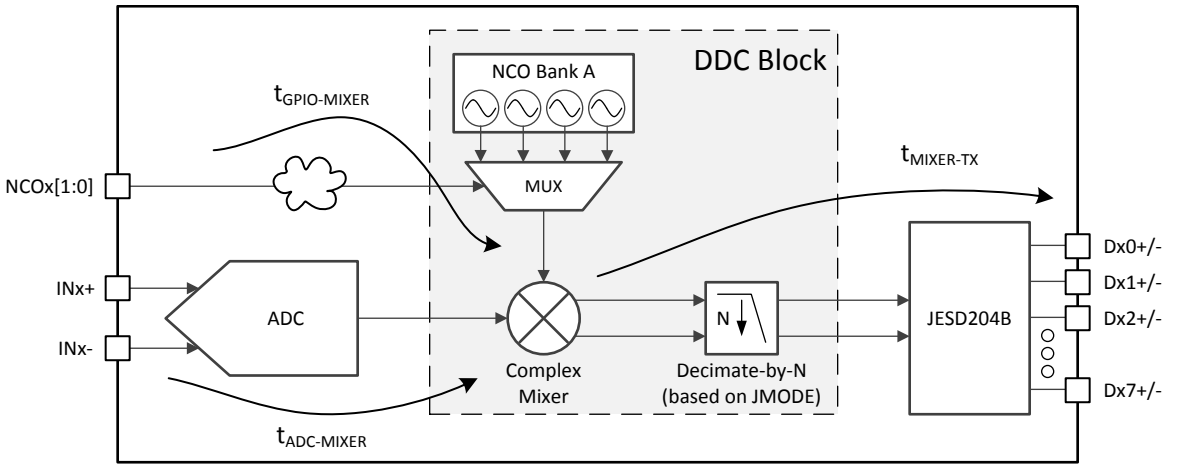


Figure 69. NCO Fast Frequency Hopping Latency Diagram

NCO hopping occurs when the NCO GPIO pins change state. The pins are controlled asynchronously and therefore synchronous switching is not possible. Associated latencies are demonstrated in Figure 69, where t_{TX} and t_{ADC} are provided in Switching Characteristics. All latencies in Table 7 are approximations only.

Table 7. NCO Fast Frequency Hopping Latency Definitions

Latency Parameter	Value or Calculation	Units
$t_{GPIO-MIXER}$	~36 to ~40	t_{CLK} cycles
$t_{ADC-MIXER}$	~36	t_{CLK} cycles
$t_{MIXER-TX}$	$(t_{TX} + t_{ADC}) - t_{ADC-MIXER}$	t_{CLK} cycles

7.3.5.1.2 NCO Selection

Within each channel's DDC, four different frequency and phase settings are available for use. Each of the four settings uses a different phase accumulator within the NCO. Since all four phase accumulators are independent and continuously running, rapid switching between different NCO frequencies is possible allowing for phase coherent frequency hopping.

The specific frequency-phase pair used for each channel is selected through the NCOA[1:0] or NCOB[1:0] input pins when CMODE is set to 1. Alternatively, the selected NCO can be chosen through SPI by CSELA for DDC A and CSELB for DDC B by setting CMODE to 0 (default). The logic table for NCO selection is provided in Table 8 for both GPIO and SPI selection options.

Table 8. Logic Table for NCO Selection using GPIO or SPI

NCO Selection	CMODE	NCOx1	NCOx0	CSELx[1]	CSELx[0]
NCO 0 using GPIO	1	0	0	X	X
NCO 1 using GPIO	1	0	1	X	X
NCO 2 using GPIO	1	1	0	X	X
NCO 3 using GPIO	1	1	1	X	X
NCO 0 using SPI	0	X	X	0	0
NCO 1 using SPI	0	X	X	0	1
NCO 2 using SPI	0	X	X	1	0
NCO 3 using SPI	0	X	X	1	1

The frequency for each phase accumulator is programmed independently through the FREQAx, FREQBx (x=0 to 3) and, optionally, NCO_RDIV register settings. The phase offset for each accumulator is programmed independently through the PHASEAx and PHASEBx (x=0 to 3) register settings.

7.3.5.1.3 Basic NCO Frequency Setting Mode

In basic NCO frequency-setting mode (NCO_RDIV = 0x0000), the NCO frequency setting is set by the 32-bit register value, FREQAx and FREQBx (x = 0 to 3). The NCO frequency for DDC A can be calculated using Equation 4, where FREQAx can be replaced by FREQBx to calculate the NCO frequency for DDC B.

$$f_{(NCO)} = \text{FREQAx} \times 2^{-32} \times f_{(DEVCLK)} \text{ (x = 0 – 3)} \quad (4)$$

NOTE

Changing the FREQAx and FREQBx register settings results in non-deterministic NCO phase. If deterministic phase is required the NCOs must be resynchronized. See NCO Phase Synchronization.

7.3.5.1.4 Rational NCO Frequency Setting Mode

In basic NCO frequency mode, the frequency step size is very small and many frequencies can be synthesized, but sometimes an application requires very specific frequencies that fall between two frequency steps. For example with f_S equal to 2457.6 MHz and a desired $f_{(NCO)}$ equal to 5.02 MHz the value for FREQAx is 8773085.867. Truncating the fractional portion results in an $f_{(NCO)}$ equal to 5.0199995 MHz, which is not the desired frequency.

To produce the desired frequency, the NCO_RDIV parameter is used to force the phase accumulator to arrive at specific frequencies without error. First, select a frequency step size ($f_{(STEP)}$) that is appropriate for the NCO frequency steps required. The typical value of $f_{(STEP)}$ is 10 kHz. Next, program the NCO_RDIV value according to Equation 5.

$$\text{NCO\_RDIV} = \frac{\left(f_{\text{DEVCLK}} \,/\, f_{\text{STEP}}\right)}{64} \quad (5)$$

The result of Equation 5 must be an integer value. If the value is not an integer, adjust either of the parameters until the result is an integer value.

For example, select a value of 1920 for NCO_RDIV.

NOTE

NCO_RDIV values larger than 8192 can degrade the NCO SFDR performance and are not recommended.

Now use Equation 6 to calculate the FREQAx register value.

$$\text{FREQAx} = \text{round}\left(2^{32} \times f_{\text{NCO}} \,/\, f_{\text{DEVCLK}}\right) \quad (6)$$

Alternatively, the following equations can be used:

$$\text{N} = \frac{f_{(NCO)}}{f_{(STEP)}} \quad (7)$$

$$\text{FREQAx} = \text{round}\left(2^{26} \times \text{N} \,/\, \text{NCO\_RDIV}\right) \quad (8)$$

Table 9. Common NCO_RDIV Values (For 10-kHz Frequency Steps)

$f_{(DEVCLK)}$ (MHz)	NCO_RDIV
3200	5000
3072	4800
2949.12	4608
2457.6	3840

Table 9. Common NCO_RDIV Values (For 10-kHz Frequency Steps) (continued)

$f_{(DEVCLK)}$ (MHz)	NCO_RDIV
1966.08	3072
1600	2500
1474.56	2304
1228.8	1920

7.3.5.1.5 NCO Phase Offset Setting

The NCO phase-offset setting for each NCO is set by the 16-bit register value PHASEAx and PHASEBx (where x = 0 to 3). The value is left-justified into a 32-bit field and then added to the phase accumulator.

Use Equation 9 to calculate the phase offset in radians.

$$\Phi(\text{rad}) = \text{PHASEA/Bx} \times 2^{-16} \times 2 \times \pi \text{ (x=0 to 3)} \quad (9)$$

7.3.5.1.6 NCO Phase Synchronization

The NCOs must be synchronized after setting or changing the value of FREQAx or FREQBx. NCO synchronization is performed when the JESD204B link is initialized or by SYSREF, based on the settings of NCO_SYNC_ILA and NCO_SYNC_NEXT. The procedures are given below for the JESD204B initialization procedure and the SYSREF procedure for both DC coupled and AC coupled SYSREF signals.

NCO synchronization using JESD204B SYNC signal ($\overline{\text{SYNCSE}}$ or TMSTP+/–):

1. Device must be programmed for normal operation
2. Set NCO_SYNC_ILA to 1
3. Set JESD_EN to 0
4. Program FREQAx, FREQBx, PHASEAx and PHASEBx to the desired settings
5. In JESD204B receiver (logic device) deassert $\overline{\text{SYNC}}$ signal by setting it high
6. Set JESD_EN to 1
7. Assert $\overline{\text{SYNC}}$ signal by setting it low in JESD204B receiver to start CGS process
8. After achieving CGS, deassert $\overline{\text{SYNC}}$ signal by setting it high at the same time for all ADCs that are to be synchronized and verify that SYNC setup and hold times are met (specified in Timing Requirements)

NCO synchronization using SYSREF (DC coupled):

1. Device must be programmed for normal operation
2. Set JESD_EN to 1 to start JESD204B link (SYNC signal can respond as normal during CGS process)
3. Program FREQAx, FREQBx, PHASEAx and PHASEBx to the desired settings
4. Verify that SYSREF is disabled (held low)
5. Arm NCO synchronization by setting NCO_SYNC_NEXT to 1
6. Issue a single SYSREF pulse to all ADCs to synchronize NCOs within all devices

NCO synchronization using SYSREF (AC coupled):

1. Device must be programmed for normal operation
2. Set JESD_EN to 1 to start JESD204B link (SYNC signal can respond as normal during CGS process)
3. Program FREQAx, FREQBx, PHASEAx and PHASEBx to the desired settings
4. Run SYSREF continuously
5. Arm NCO synchronization by setting NCO_SYNC_NEXT to 1 at the same time at all ADCs by timing the rising edge of SCLK for the last data bit (LSB) at the end of the SPI write so that it occurs after a SYSREF rising edge and early enough before the next SYSREF rising edge so that the trigger is armed before the next SYSREF rising edge (long SYSREF period is recommended)
6. NCOs in all ADCs will be synchronized by the next SYSREF rising edge

7.3.5.2 Decimation Filters

The decimation filters are arranged to provide a programmable overall decimation of 2, 4, 8 or 16. All filter outputs have a resolution of 15 bits. The decimate-by-2 filter has a real output, while the decimate-by-4, decimate-by-8, and decimate-by-16 filters have complex outputs. Table 10 lists the effective output sample rates, available signal bandwidths, output formats and stop-band attenuation for each decimation mode. Note that the available bandwidths of the complex output modes are higher than expected for the given decimation factor or output sample rate due to the pair I/Q nature of the output data. This results in the Decimate-by-2 real and Decimate-by-4 complex modes having approximately the same useful output bandwidth.

Table 10. Output Sample Rates and Signal Bandwidths

DECIMATION SETTING	$f_{(DEVCLK)}$				OUTPUT FORMAT
	OUTPUT RATE (MSPS)	MAX ALIAS PROTECTED SIGNAL BANDWIDTH (MHz)	STOP-BAND ATTENUATION	PASS-BAND RIPPLE	
No decimation	$f_{(DEVCLK)}$	$f_{(DEVCLK)}$ / 2	n/a	< +/– 0.001 dB	Real signal, 12-bit data
Decimate-by-2	$f_{(DEVCLK)}$ / 2	0.4 x $f_{(DEVCLK)}$ / 2	> 89 dB	< +/– 0.001 dB	Real signal, 15-bit data
Decimate-by-4 (D4_AP87 = 0)	$f_{(DEVCLK)}$ / 4	0.8 x $f_{(DEVCLK)}$ / 4	> 90 dB	< +/– 0.001 dB	Complex signal, 15-bit data
Decimate-by-4 (D4_AP87 = 1)	$f_{(DEVCLK)}$ / 4	0.875 x $f_{(DEVCLK)}$ / 4	> 66 dB	< +/– 0.005 dB	Complex signal, 15-bit data
Decimate-by-8	$f_{(DEVCLK)}$ / 8	0.8 x $f_{(DEVCLK)}$ / 8	> 90 dB	< +/– 0.001 dB	Complex signal, 15-bit data
Decimate-by-16	$f_{(DEVCLK)}$ / 16	0.8 x $f_{(DEVCLK)}$ / 16	> 90 dB	< +/– 0.001 dB	Complex signal, 15-bit data

The composite decimation filter responses are given in the figures below. The passband section (black trace) shows the alias protected region of the response. The transition band (red trace) shows the transition region of the response, or the regions that alias into the transition region, which is not alias protected and therefore no desired signals should be within this band. The aliasing band (blue trace) shows the attenuation applied to the bands that alias back into the passband after decimation and are sufficiently low to prevent undesired signals from showing up in the passband. Analog input filtering should be used for addition attenuation of the aliasing band or to prevent harmonics, interleaving spurs or other undesired spurious signals from folding into the desired signal band before the decimation filter.

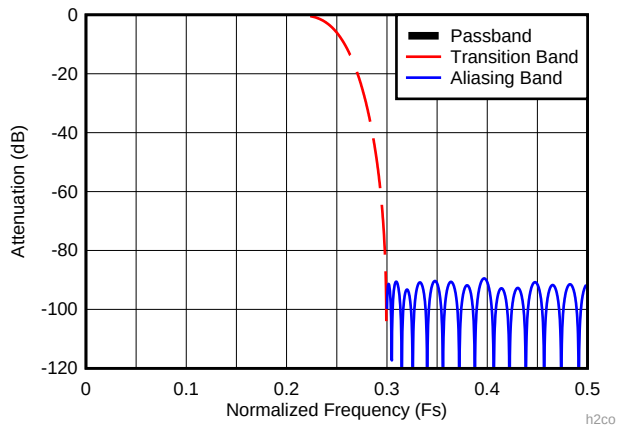


Figure 70. Decimate-by-2 Composite Response (D2_HIGH_PASS = 0)

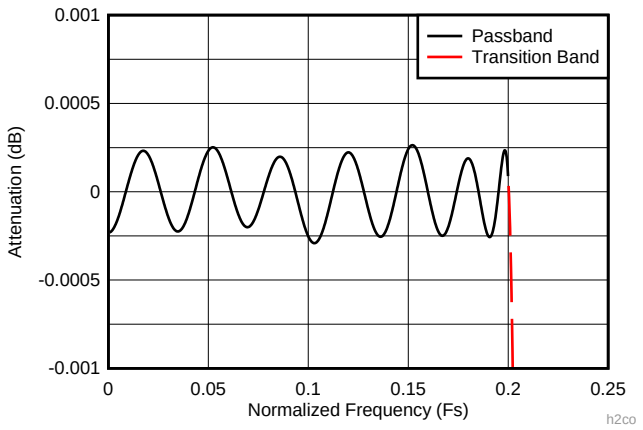


Figure 71. Decimate-by-2 Composite Zoomed Passband Response (D2_HIGH_PASS = 0)

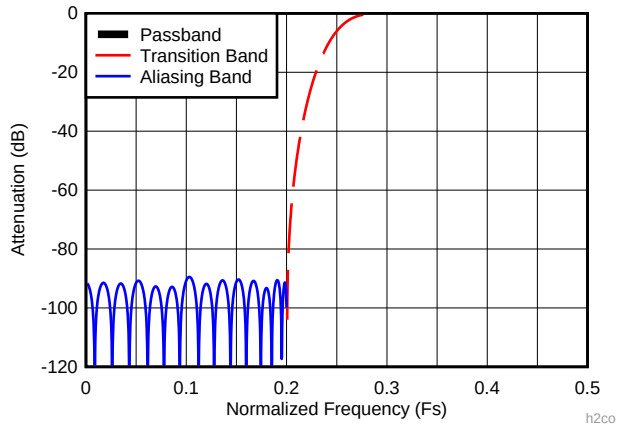


Figure 72. Decimate-by-2 Composite Response (D2_HIGH_PASS = 1)

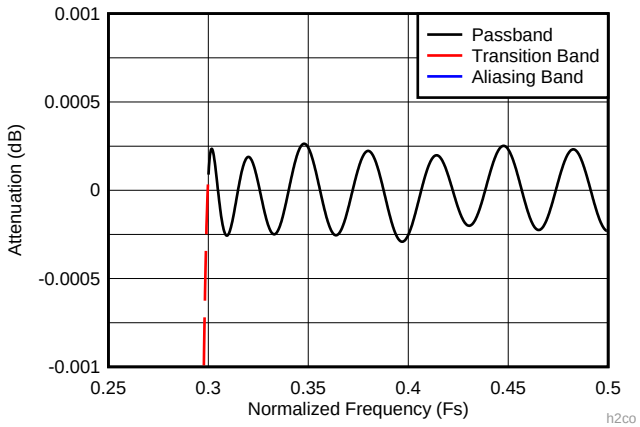


Figure 73. Decimate-by-2 Composite Zoomed Passband Response (D2_HIGH_PASS = 1)

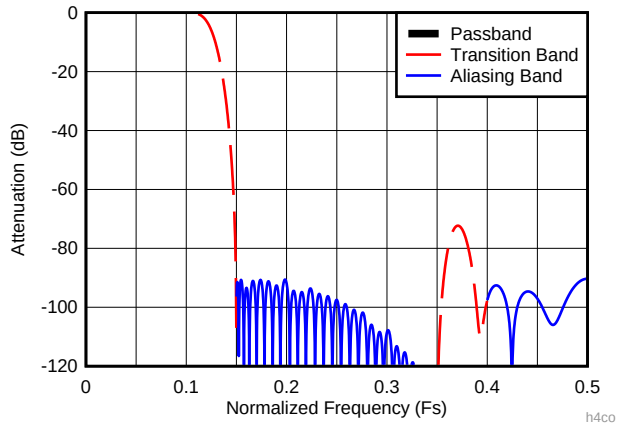


Figure 74. Decimate-by-4 Composite Response (D4_AP87 = 0)

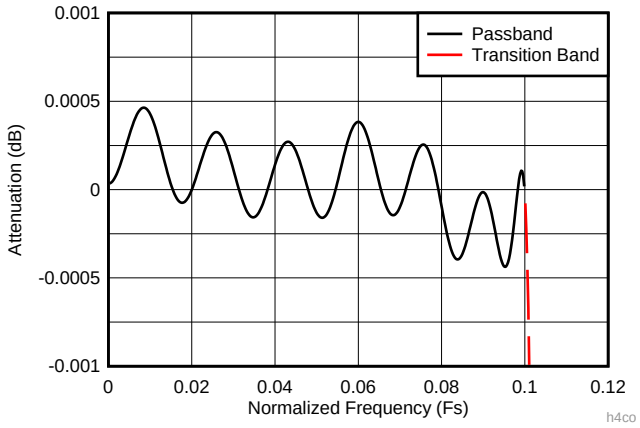


Figure 75. Decimate-by-4 Composite Zoomed Passband Response (D4_AP87 = 0)

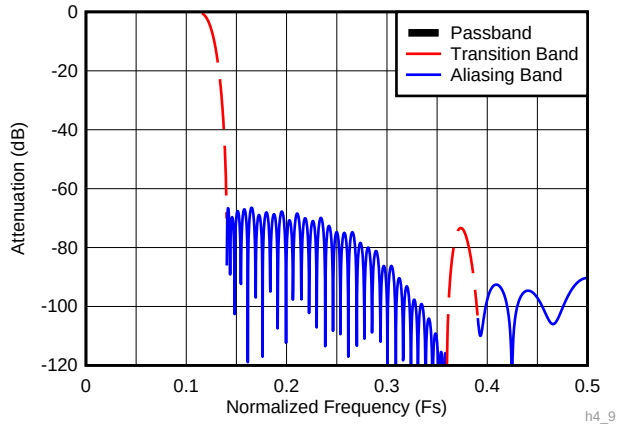


Figure 76. Decimate-by-4 Composite Response (D4_AP87 = 1)

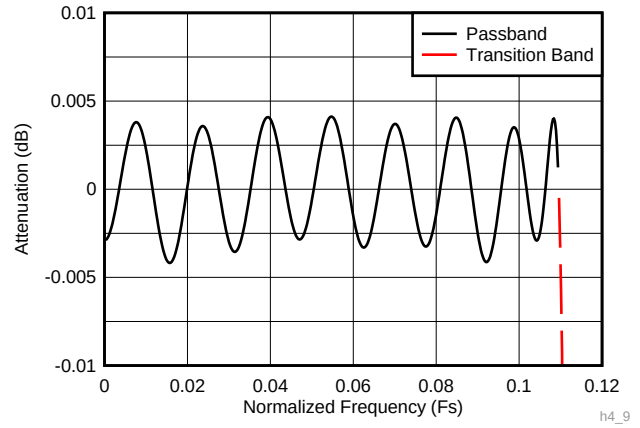


Figure 77. Decimate-by-4 Composite Zoomed Passband Response (D4_AP87 = 1)

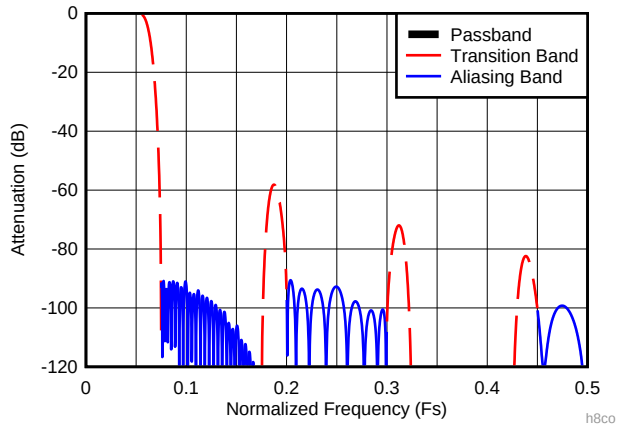


Figure 78. Decimate-by-8 Composite Response

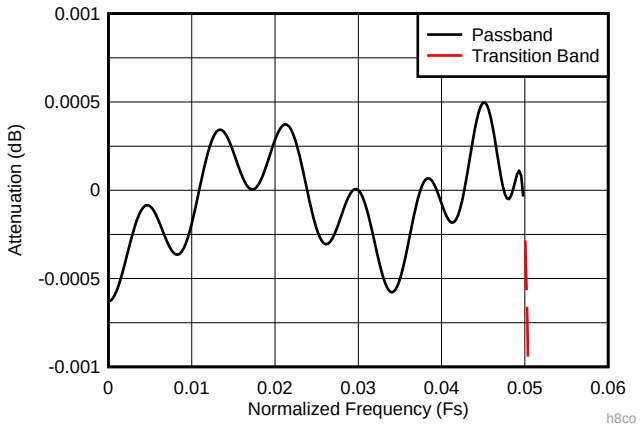


Figure 79. Decimate-by-8 Composite Zoomed Passband Response

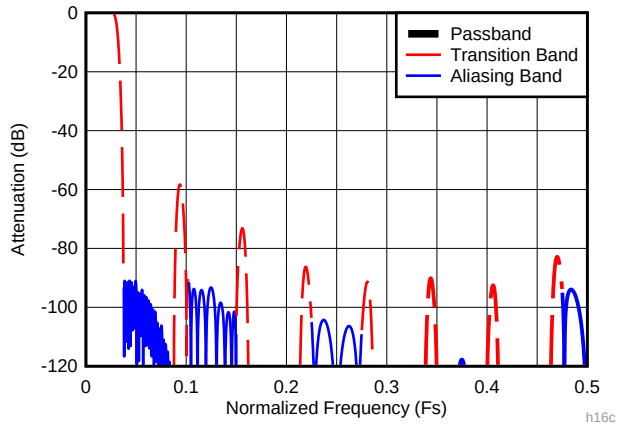


Figure 80. Decimate-by-16 Composite Response

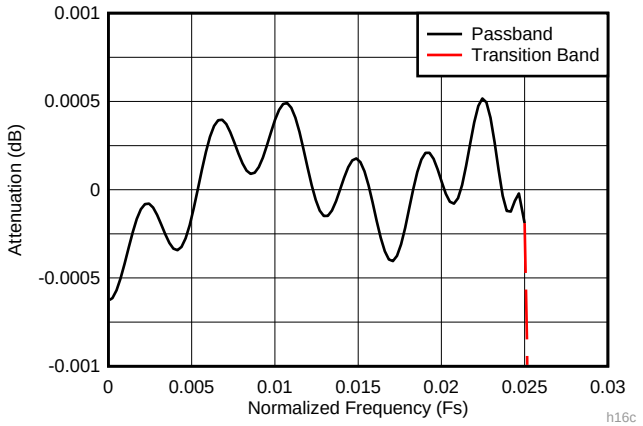


Figure 81. Decimate-by-16 Composite Zoomed Passband Response

For maximum efficiency a group of high speed filter blocks are implemented with specific blocks used for each decimation setting to achieve the composite responses shown in the previous figures. Table 11 describes the combination of filter blocks used for each decimation setting and Table 12 lists the coefficient details and decimation factor of each filter block. The coefficients are symmetric with the center tap indicated by bold text.

Table 11. Decimation Mode Filter Usage

Decimation Setting	Filter Blocks Used
2	CS80
4 (D4_AP87 = 0)	CS45, CS80
4 (D4_AP87 = 1)	CS45, CS87
8	CS20, CS40, CS80
16	CS10, CS20, CS40, CS80

Table 12. Filter Coefficient Details

Filter Coefficient Set (Decimation Factor of Filter)											
CS10 (2)		CS20 (2)		CS40 (2)		CS45 (2)		CS80 (2)		CS87 (2)	
–65	–65	109	109	–327	–327	56	56	–37	–37	–15	–15
0	0	0	0	0	0	0	0	0	0	0	0
577	577	–837	–837	2231	2231	–401	–401	118	118	23	23
1024		0	0	0	0	0	0	0	0	0	0
		4824	4824	–8881	–8881	1596	1596	–291	–291	–40	–40
		8192		0	0	0	0	0	0	0	0
				39742	39742	–4979	–4979	612	612	64	64
				65536		0	0	0	0	0	0
						20113	20113	–1159	–1159	–97	–97
						32768		0	0	0	0
								2031	2031	142	142
								0	0	0	0
								–3356	–3356	–201	–201
								0	0	0	0
								5308	5308	279	279
								0	0	0	0
								–8140	–8140	–380	–380
								0	0	0	0
								12284	12284	513	513
								0	0	0	0
								–18628	–18628	–690	–690
								0	0	0	0
								29455	29455	939	939
								0	0	0	0
								–53191	–53191	–1313	–1313
								0	0	0	0
								166059	166059	1956	1956
								262144		0	0
										–3398	–3398
										0	0
										10404	10404
										16384	

7.3.5.3 Output Data Format

The DDC output data varies depending on the selected JMODE. Real decimate-by-2 mode (JMODE 9) consists of 15-bit real output data. Complex decimation modes (JMODE 10 to 16), except for JMODE 12, consist of 15–bit complex data plus the two over-range threshold-detection control bits. JMODE 12 output data consists of 12-bit complex data, but does not include the two over-range threshold-detection control bits which should instead be monitored using the ORA0/1 and ORB0/1 output pins. The following table lists the data format:

Table 13. Real Decimation (JMODE 9) Output Sample Format

DDC CHANNEL	ODD/ EVEN SAMPLE	16-BIT OUTPUT WORD															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	EVEN	DDC A even numbered sample 15-bit output data															OVR_T0
A	ODD	DDC A odd numbered sample 15-bit output data															OVR_T1
B	EVEN	DDC B even numbered sample 15-bit output data															OVR_T0
B	ODD	DDC B odd numbered sample 15-bit output data															OVR_T1

Table 14. Complex Decimation Output Sample Format (Except JMODE 12)

I/Q SAMPLE	16-BIT OUTPUT WORD															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I	DDC in-phase (I) 15-bit output data															OVR_T0
Q	DDC quadrature (Q) 15-bit output data															OVR_T1

7.3.5.4 Decimation Settings

7.3.5.4.1 Decimation Factor

The decimation setting is adjustable over the following settings and is set by the JMODE parameter. See Table 18 for the available JMODE values and the corresponding decimation settings.

- DDC Bypass: No decimation, real output
- Decimate-by-2: Real output (JMODE 9)
- Decimate-by-4: Complex output (JMODE 10 to 12)
- Decimate-by-8: Complex output (JMODE 13 to 14)
- Decimate-by-16: Complex output (JMODE 15 to 16)

7.3.5.4.2 DDC Gain Boost

The DDC gain boost (*DDC Configuration Register (address = 0x210) [reset = 0x00]*) provides additional gain through the DDC block. Setting BOOST to 1 sets the total decimation filter chain gain to 6.02-dB. With a setting of 0, the total decimation filter chain has a 0-dB gain. This setting should only be used when the negative image of the input signal is filtered out by the decimation filters, otherwise clipping may occur. There is no reduction in analog performance when gain boost is enabled or disabled, but care should be taken to understand the reference output power for proper performance calculations.

7.3.6 JESD204B Interface

ADC12DJ3200 uses the JESD204B high-speed serial interface for data converters to transfer data from the ADC to the receiving logic device. ADC12DJ3200 serialized lanes are capable of operating up to 12.8 Gbps, slightly above the JESD204B max lane rate. A maximum of sixteen lanes can be used to allow lower lane rates for interfacing with speed limited logic devices. Figure 82 shows a simplified block diagram of the JESD204B interface protocol.

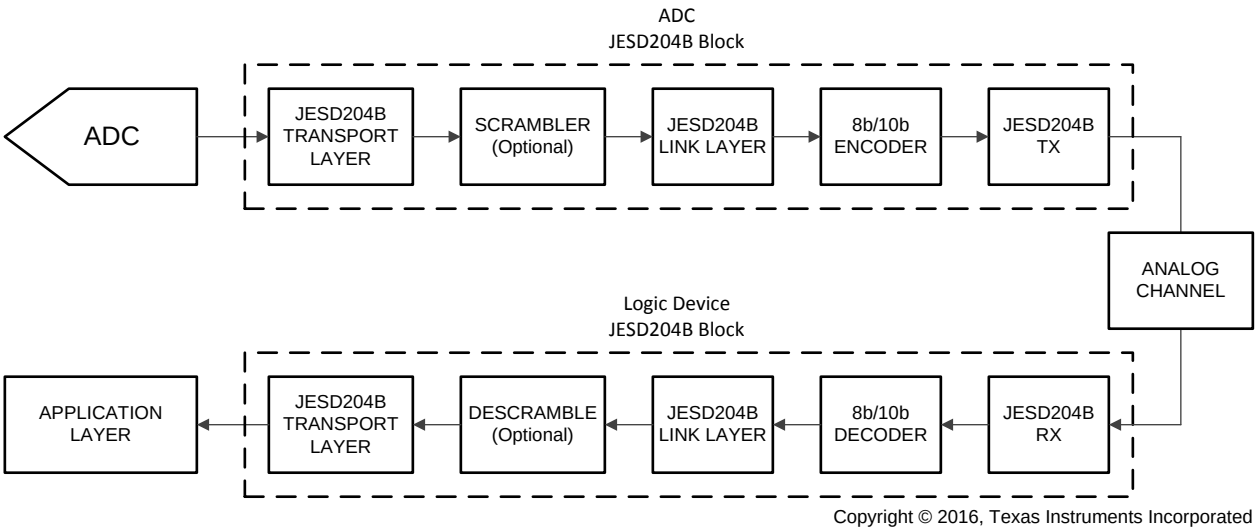


Figure 82. Simplified JESD204B Interface Diagram

The various signals used in the JESD204B interface and the associated ADC12DJ3200 pin names are summarized briefly in Table 15 for reference.

Table 15. Summary of JESD204B Signals

Signal Name	ADC12DJ3200 Pin Names	Description
Data	DA0+...DA7+, DA0–...DA7–, DB0+...DB7+, DB0–...DB7–	High-speed serialized data after 8b/10b encoding
$\overline{\text{SYNC}}$	$\overline{\text{SYNCSE}}$, TMSTP+, TMSTP–	Link initialization signal (handshake), toggles low to start code group synchronization (CGS) process
Device Clock	CLK+, CLK–	ADC sampling clock, also used for clocking digital logic and output serializers
SYSREF	SYSREF+, SYSREF–	System timing reference used to deterministically reset the internal local multiframe counters in each JESD204B device

7.3.6.1 Transport Layer

The transport layer takes samples from the ADC output (in decimation bypass mode) or from the DDC output and maps the samples into octets, frames, multiframes and lanes. Sample mapping is defined by the JESD204B mode that is used, defined by parameters such as L, M, F, S, N, N', CF, etc. There are a number of predefined transport layer modes in the ADC12DJ3200 which are defined in Table 18. The high level configuration parameters for the transport layer in ADC12DJ3200 are described in *Table 16*. For simplicity, the transport layer mode is chosen by simply setting the JMODE parameter and the desired K value. For reference, the various configuration parameters for JESD204B are defined in Table 17.

7.3.6.2 Scrambler

An optional data scrambler can be used to scramble the octets before transmission across the channel. Scrambling is recommended in order to remove the possibility of spectral peaks in the transmitted data. The JESD204B receiver automatically synchronizes its descrambler to the incoming scrambled data stream. The initial lane alignment sequence (ILA) is never scrambled. Scrambling can be enabled by setting SCR (*JESD204B Control Register (address = 0x204) [reset = 0x02]*).

7.3.6.3 Link Layer

The link layer serves multiple purposes in JESD204B, including establishing the code boundaries (Code Group Synchronization (CGS)), initializing the link (Initial Lane Alignment Sequence (ILAS)), encoding the data (8b/10b Encoding) and monitoring the health of the link (Frame and Multiframe Monitoring).

7.3.6.3.1 Code Group Synchronization (CGS)

The first step in initializing the JESD204B link, after SYSREF is processed, is to achieve code group synchronization. The receiver first asserts the SYNC signal when ready to initialize the link. The transmitter responds to the request by sending a stream of K28.5 characters. The receiver then aligns its character clock to the K28.5 character sequence. Code group synchronization is achieved after receiving four K28.5 characters successfully. The receiver deasserts SYNC on the next local multi-frame clock (LMFC) edge after CGS is achieved and waits for the transmitter to start the initial lane alignment sequence.

7.3.6.3.2 Initial Lane Alignment Sequence (ILAS)

After the transmitter sees the SYNC signal deassert it waits until its next LMFC edge to start sending the initial lane alignment sequence. The ILAS consists of four multiframes each containing a predetermined sequence. The receiver looks for the start of the ILAS to determine the frame and multiframe boundaries. As the ILAS reaches the receiver for each lane, the lane starts to buffer its data until all receivers have received the ILAS and subsequently release the ILAS from all lanes at the same time in order to align the lanes. The second multiframe of the ILAS contains configuration parameters for the JESD204B that can be used by the receiver to verify that the transmitter and receiver configurations match.

7.3.6.3.3 8b/10b Encoding

The data link layer converts the 8-bit octets from the transport layer into 10-bit characters for transmission across the link using 8b/10b encoding. 8b/10b encoding provides DC balance for AC coupling of the serdes links and a sufficient number of edge transitions for the receiver to reliably recover the data clock. 8b/10b also provides some amount of error detection where a single bit error in a character will likely result in either not being able to find the 10-bit character in the 8b/10b decoder lookup table or incorrect character disparity.

7.3.6.3.4 Frame and Multiframe Monitoring

ADC12DJ3200 supports frame and multiframe monitoring for verifying the health of the JESD204B link. If the last octet of a frame matches the last octet of the previous frame, then the second frame's last octet is replaced with a /F/ (/K28.7/) character. If the second frame is the last frame of a multiframe then a /A/ (/K28.3/) character is used instead. When scrambling is enabled, if the last octet of a frame is 0xFC then the transmitter replaces it with a /F/ (/K28.7/) character. With scrambling, if the last octet of a multiframe is 0x7C then the transmitter replaces it with a /A/ (/K28.3/) character. When the receiver sees a /F/ or /A/ character, it checks to see if it occurs at the end of a frame or multiframe, and replaces it with the appropriate data character. The receiver can report an error if the alignment characters occur in the incorrect place and trigger a link realignment.

7.3.6.4 Physical Layer

The JESD204B physical layer consists of a current mode logic (CML) output driver and receiver. The receiver consists of a clock detection and recovery (CDR) unit to extract the data clock from the serialized data stream and may contain an equalizer to correct for the low pass response of the physical transmission channel. Likewise, the transmitter may contain pre-equalization to account for frequency dependent losses across the channel. The total reach of the serdes links depends on the data rate, board material, connectors, equalization, noise and jitter, and required bit-error performance. The serdes lanes do not have to be matched in length as the receiver will align the lanes during the initial lane alignment sequence.

7.3.6.4.1 Serdes Pre-Emphasis

ADC12DJ3200 high-speed output drivers can pre-equalize the transmitted data stream by using pre-emphasis in order to compensate for the low pass response of the transmission channel. Configurable pre-emphasis settings allow the output drive waveform to be optimized for different PCB materials and signal transmission distances. The pre-emphasis setting is adjusted through the serializer pre-emphasis setting SER_PE (*Serializer Pre-Emphasis Control Register (address = 0x048) [reset = 0x00]*). Higher values will increase the pre-emphasis to compensate for more lossy PCB materials. This adjustment is best used in conjunction with an eye-diagram analysis capability in the receiver. The pre-emphasis setting should be adjusted to optimize the eye-opening for the specific hardware configuration and line rates needed.

7.3.6.5 JESD204B Enable

The JESD204B interface must be disabled through JESD_EN (*JESD204B Enable Register (address = 0x200) [reset = 0x01]*) while any of the other JESD204B parameters are being changed. While JESD_EN is set to 0 the block is held in reset and the serializers are powered down. The clocks for this section are also gated off to further save power. When the parameters have been set as desired the JESD204B block can be enabled (JESD_EN is set to 1).

7.3.6.6 Multi-Device Synchronization and Deterministic Latency

JESD204B subclass 1 outlines a method to achieve deterministic latency across the serial link. If two devices achieve the same deterministic latency then they can be considered synchronized. This latency must be achieved from system startup to startup to be deterministic. There are two key requirements to achieve deterministic latency. The first is proper capture of SYSREF for which ADC12DJ3200 provides a number of features to simplify this requirement at giga-sample clock rates (see SYSREF Capture for Multi-Device Synchronization and Deterministic Latency for more information).

The second requirement is to choose a proper elastic buffer release point in the receiver. Since ADC12DJ3200 is an ADC it is the transmitter (TX) in the JESD204B link and the logic device will be the receiver (RX). The elastic buffer is the key block for achieving deterministic latency. It does so by absorbing variations in the propagation delays of the serialized data as it travels from the transmitter to the receiver. A proper release point is one that provides sufficient margin against variations in the delays. An incorrect release point will result in a latency

variation of one LMFC period. Choosing a proper release point requires knowing the average arrival time of data at the elastic buffer, referenced to an LMFC edge, and the total expected delay variation for all devices. With this information the region of invalid release points within the LMFC period can be defined, which stretches from the minimum to maximum delay for all lanes. Essentially, the designer must guarantee that the data for all lanes arrives at all devices before the release point occurs.

It is easier to demonstrate this requirement by using a timing diagram as illustrated in Figure 83. Here, the data for two ADCs is shown. The second ADC has a longer routing distance (t_{PCB}) and results in a longer link delay. First, the invalid region of the LMFC period is marked off as determined by the data arrival times for all devices. Then, the release point is set by using the release buffer delay (RBD) parameter to shift the release point an appropriate number of frame clocks from the LMFC edge so that it occurs within the valid region of the LMFC cycle. In the case of Figure 2, the LMFC edge (RBD = 0) is a good choice for the release point due to sufficient margin on each side.

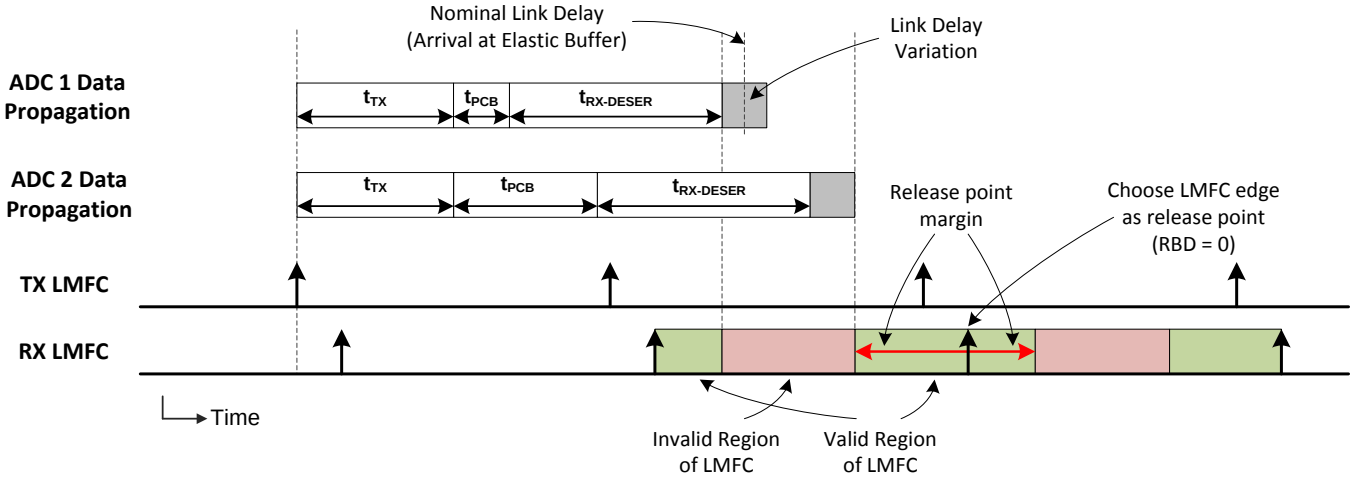


Figure 83. Definition of valid region of LMFC for elastic buffer release point selection

Note that the TX and RX LMFCs do not necessarily need to be phase aligned, but knowledge of their phase is important for proper elastic buffer release point selection. Also, the elastic buffer release point occurs within every LMFC cycle, but the buffers only release once all lanes have arrived. Therefore, the total link delay can exceed a single LMFC period. See JESD204B multi-device synchronization: Breaking down the requirements for more information.

7.3.6.7 Operation in Subclass 0 Systems

The ADC12DJ3200 can operate with Subclass 0 compatibility provided that multi-ADC synchronization and deterministic latency are not required. With those limitations the device can operate without the application of SYSREF. The internal Local Multi-Frame Clock will be automatically self-generated with unknown timing. SYNC will be used as normal to initiate CGS and ILA.

7.3.7 Alarm Monitoring

A number of built in alarms are available to monitor internal events. Several types of alarms/upsets are detected by this feature:

1. Serializer PLL not locked
2. JESD204B link not transmitting data (not in the data transmission state)
3. SYSREF caused internal clocks to be realigned
4. An upset that impacts the NCO
5. An upset that impacts the internal clocks

When an alarm occurs, a bit for each specific alarm is set in ALM_STATUS. Each alarm bit remains set until the host system writes a 1 to clear it. If the alarm type is not masked (see ALM_MASK), then the alarm is also indicated by the ALARM register. The CALSTAT output pin can be configured as an alarm output that will go high when an alarm occurs. See CAL_STATUS_SEL.

7.3.7.1 NCO Upset Detection

The NCO_ALM register bit indicates if the NCO in channel A or B may have been upset. The NCO phase accumulators in channel A are continuously compared to channel B. If they differ for even one clock cycle, the NCO_ALM register bit is set and remains set until cleared by the host system by writing a 1. This feature requires the phase and frequency words for each NCO accumulator in DDC A (PHASEAx, FREQAx) to be set to the same values as the NCO accumulators in DDC B (PHASEBx, FREQBx). For example, PHASEA0 must be the same as PHASEB0 and FREQA0 must be the same as FREQB0, however PHASEA1 can be set to a different value than PHASEA0. This ultimate reduces the number of NCO frequencies available for phase coherent frequency hopping from four to two for each DDC. Note that DDC B can use a different NCO frequency than DDC A by setting the NCOB[1:0] pins to a different value than NCOA[1:0]. This detection is only valid after the NCOs have been synchronized by either SYSREF or the start of the ILA sequence (as determined by NCO_SYNC). For NCO upset detection to work properly, follow this usage model:

1. Program JESD_EN=0
2. Ensure the part is configured to utilize both channels (PD_ACH=0, PD_BCH=0)
3. Select a JMODE that utilizes the NCO
4. Program all NCO frequencies and phases the same for channel A and B, for example FREQA0=FREQB0, FREQA1=FREQB1, FREQA2=FREQB2, FREQA3=FREQB3).
5. If desired, utilize the CMODE and CSEL registers or the NCOA[1:0] and NCOB[1:0] pins to choose a unique frequency for channel A and channel B
6. Program JESD_EN=1
7. Synchronize the NCOs (using the ILA or using SYSREF). See NCO_SYNC register.
8. Write a ‘1’ to the NCO_ALM register bit to clear it
9. Monitor the NCO_ALM status bit or the CALSTAT output pin if CAL_STATUS_SEL is properly configured
10. If the frequency or phase registers are changed while the NCO is enabled, the NCOs can get out of synchronization. Repeat steps 7-9.
11. If the device enters and exits global power down, repeat steps 7-9.

7.3.7.2 Clock Upset Detection

The CLK_ALM register bit indicates if the internal clocks may have been upset. The clocks in channel A are continuously compared to channel B. If they differ for even one DEVCLK/2 cycle, the CLK_ALM register bit is set and remains set until cleared by the host system by writing a ‘1’. For the CLK_ALM register bit to function properly, follow this usage model:

1. Program JESD_EN=0
2. Ensure the part is configured to utilize both channels (PD_ACH=0, PD_BCH=0)
3. Program JESD_EN=1
4. Write CLK_ALM=1 to clear CLK_ALM
5. Monitor the CLK_ALM status bit or the CALSTAT output pin if CAL_STATUS_SEL is properly configured
6. When exiting global power-down (via MODE or the PD pin), the CLK_ALM status bit may be set and should be cleared by writing a '1' to CLK_ALM

7.3.8 Temperature Monitoring Diode

A built-in thermal monitoring diode is made available on the TDIODE+ and TDIODE– pins. This diode facilitates temperature monitoring and characterization of the device in higher ambient temperature environments. While the on-chip diode is not highly characterized, the diode can be used effectively by performing a baseline measurement (offset) at a known ambient or board temperature and creating a linear equation with the diode voltage slope provided in Electrical Characteristics - DC Specifications. Offset measurement should be done with the device unpowered or with the PD pin asserted to minimize device self-heating. PD pin should be asserted only long enough to take the offset measurement. Recommended monitoring ICs include the LM95233 device and similar remote-diode temperature monitoring products from Texas Instruments.

7.3.9 Analog Reference Voltage

The reference voltage for ADC12DJ3200 is derived from an internal bandgap reference. A buffered version of the reference voltage is available at the BG pin for user convenience. This output has an output-current capability of ±100 μA. The BG output must be buffered if more current is required. No provision exists for the use of an external reference voltage, but the full-scale input voltage can be adjusted through the full-scale-range register settings. In unique cases, the VA11 supply voltage can act as the reference voltage by setting BG_BYPASS (*Internal Reference Bypass Register (address = 0x038) [reset = 0x00]*).

7.4 Device Functional Modes

ADC12DJ3200 can be configured to operate in a number of functional modes. These modes are described in this section.

7.4.1 Dual Channel Mode

ADC12DJ3200 can be used as a dual channel ADC where the sampling rate is equal to the clock frequency ($F_S = F_{CLK}$) provided at the CLK+ and CLK- pins. The two inputs, AIN+/- and BIN+/-, serve as the respective inputs for each channel in this mode. This mode is chosen simply by setting JMODE to the appropriate setting for the desired configuration as described in Table 18. The analog inputs can be swapped by setting DUAL_INPUT (*Input Mux Control Register (address = 0x060) [reset = 0x01]*)

7.4.2 Single Channel Mode (DES Mode)

ADC12DJ3200 can also be used as a single channel ADC where the sampling rate is equal to two times the clock frequency ($F_S = 2xF_{CLK}$) provided at the CLK+ and CLK– pins. This mode effectively interleaves the two ADC channels together to form a single channel ADC at twice the sampling rate. This mode is chosen simply by setting JMODE to the appropriate setting for the desired configuration as described in Table 18. Either analog input, INA+/– or INB+/–, can serve as the input to the ADC, however INA+/– is recommended for best performance. The analog input can be selected using SINGLE_INPUT (*Input Mux Control Register (address = 0x060) [reset = 0x01]*). The digital down-converters cannot be used in single channel mode.

NOTE

In single channel mode it is strongly recommended that INA+/– be used as the input to the ADC for optimized performance.

7.4.3 JESD204B Modes

ADC12DJ3200 can be programmed as a single channel or dual channel ADC, with or without decimation, and a number JESD204B output formats. Table 16 summarizes the basic operating mode configuration parameters and whether they are user configured or derived.

NOTE

Power down of the high speed data outputs (DA0+/– ... DA7+/–, DB0+/– ... DB7+/–) for extended times may reduce performance of the output serializers, especially at high data rates. Please see note beneath Recommended Operating Conditions for more information.

Table 16. ADC12DJ3200 Operating Mode Configuration Parameters

Parameter	Description	User configured or Derived	Value
JMODE	JESD204B operating mode, automatically derives the rest of the JESD204B parameters, single channel or dual channel mode and the decimation factor	User	Set by JMODE (*JESD204B Mode Register (address = 0x201) [reset = 0x02]*)
D	Decimation factor	Derived	See Table 18
DES	1 = single channel mode, 0 = dual channel mode	Derived	See Table 18

Device Functional Modes (continued)

Table 16. ADC12DJ3200 Operating Mode Configuration Parameters (continued)

Parameter	Description	User configured or Derived	Value
R	Number of bits transmitted per lane per DEVCLK cycle. The JESD204B linerate is the DEVCLK frequency times R. This parameter sets the SERDES PLL multiplication factor or controls bypassing of the SERDES PLL.	Derived	See Table 18
Links	Number of JESD204B links used	Derived	See Table 18
K	Number of frames per multi-frame	User Configured	Set by KM1 (*JESD204B K Parameter Register (address = 0x202) [reset = 0x1F]*), see allowed values in Table 18

There are a number of parameters required to define the JESD204B format, all of which are sent across the link during the initial lane alignment sequence. In the ADC12DJ3200, most of the parameters are automatically derived based on the selected JMODE; however, a few are configured by the user. These parameters are described in Table 17.

Table 17. JESD204B Initial Lane Alignment Sequence Parameters

Parameter	Description	User configured or Derived	Value
ADJCNT	LMFC adjustment amount (not applicable)	Derived	Always 0
ADJDIR	LMFC adjustment direction (not applicable)	Derived	Always 0
BID	Bank ID	Derived	Always 0
CF	Number of control words per frame	Derived	Always 0
CS	Control bits per sample	Derived	Always set to 0 in ILAS, see Table 18 for actual usage
DID	Device identifier, used to identify the link	User	Set by DID (*JESD204B DID Parameter Register (address = 0x206) [reset = 0x00]*), see Table 19
F	Number of octets (bytes) per frame (per lane)	Derived	See Table 18
HD	High density format (samples split between lanes)	Derived	Always 0
JESDV	JESD204 standard revision	Derived	Always 1
K	Number of frames per multi-frame	User	Set by KM1 register, *JESD204B K Parameter Register (address = 0x202) [reset = 0x1F]*
L	Number of serial output lanes per link	Derived	See Table 18
LID	Lane identifier for each lane	Derived	See Table 19
M	Number of converters used to determine lane bit packing; may not match number of ADC channels in the device	Derived	See Table 18
N	Sample resolution (before adding control and tail bits)	Derived	See Table 18
N'	Bits per sample after adding control and tail bits	Derived	See Table 18
S	Number of samples per converter (M) per frame	Derived	See Table 18
SCR	Scrambler enabled	User	Set by SCR register

Table 17. JESD204B Initial Lane Alignment Sequence Parameters (continued)

Parameter	Description	User configured or Derived	Value
SUBCLASSV	Device subclass version	Derived	Always 1
RES1	Reserved field 1	Derived	Always 0
RES2	Reserved field 2	Derived	Always 0
CHKSUM	Checksum for ILAS checking (sum of all above parameters modulo 256)	Derived	Computed based on above parameters

Configuring the ADC12DJ3200 is made easy by use of a single configuration parameter called JMODE (*JESD204B Mode Register (address = 0x201) [reset = 0x02]*). Using Table 18, the correct JMODE value can be found for the desired operating mode. The modes shown in Table 18 are the only available operating modes. The table also gives a range and allowable step size for the K parameter (set by KM1, see *JESD204B K Parameter Register (address = 0x202) [reset = 0x1F]*), which sets the multi-frame length in number of frames.

Table 18. ADC12DJ3200 Operating Modes

ADC12DJ3200 Operating Mode	User Specified Parameter		Derived Parameters											Input Clock Range (MHz)
	JMODE	K [Min:Step:Max]	D	DES	Links	N	CS	N'	L (per link)	M (per link)	F	S	R (Fbit/Fclk)	
12-bit, Single Channel, 8 lanes	0	3:1:32	1	1	2	12	0	12	4	4 (1)	8	5	4	800-3200
12-bit, Single Channel, 16 lanes	1	3:1:32	1	1	2	12	0	12	8	8 (1)	8	5	2	800-3200
12-bit, Dual Channel, 8 lanes	2	3:1:32	1	0	2	12	0	12	4	4 (1)	8	5	4	800-3200
12-bit, Dual Channel, 16 lanes	3	3:1:32	1	0	2	12	0	12	8	8 (1)	8	5	2	800-3200
8-bit, Single Channel, 4 lanes	4	18:2:32	1	1	2	8	0	8	2	1	1	2	5	800-2560
8-bit, Single Channel, 8 lanes	5	18:2:32	1	1	2	8	0	8	4	1	1	4	2.5	800-3200
8-bit, Dual Channel, 4 lanes	6	18:2:32	1	0	2	8	0	8	2	1	1	2	5	800-2560
8-bit, Dual Channel, 8 lanes	7	18:2:32	1	0	2	8	0	8	4	1	1	4	2.5	800-3200
RESERVED	8	-	-	-	-	-	-	-	-	-	-	-	-	-
15-bit, Real Data, Decimate-by-2, 8 lanes	9	9:1:32	2	0	2	15	1 (2)	16	4	1	2	4	2.5	800-3200
15-bit, Decimate-by-4, 4 lanes	10	9:1:32	4	0	2	15	1 (2)	16	2	2	2	1	5	800-2560
15-bit, Decimate-by-4, 8 lanes	11	9:1:32	4	0	2	15	1 (2)	16	4	2	2	2	2.5	800-3200
12-bit, Decimate-by-4, 16 lanes	12	3:1:32	4	0	2	12	0	12	8	8 (1)	8	5	1	1000-3200
15-bit, Decimate-by-8, 2 lanes	13	5:1:32	8	0	2	15	1 (2)	16	1	2	4	1	5	800-2560
15-bit, Decimate-by-8, 4 lanes	14	9:1:32	8	0	2	15	1 (2)	16	2	2	2	1	2.5	800-3200
15-bit, Decimate-by-16, 1 lane	15	3:1:32	16	0	1	15	1 (2)	16	1	4	8	1	5	800-2560
15-bit, Decimate-by-16, 2 lanes	16	5:1:32	16	0	2	15	1 (2)	16	1	2	4	1	2.5	800-3200
8-bit, Single Channel, 16 lanes	17	18:2:32	1	1	2	8	0	8	8	1	1	8	1.25	800-3200
8-bit, Dual Channel, 16 lanes	18	18:2:32	1	0	2	8	0	8	8	1	1	8	1.25	800-3200

(1) M equals L in these modes to allow the samples to be sent in time-order over L lanes. The M parameter does not represent the actual number of converters. The M sample streams from each link should be interleaved in the receiver to produce the correct sample data. See mode diagrams for more details.
(2) CS is always reported as 0 in the initial lane alignment sequence (ILAS) for ADC12DJ3200.

ADC12DJ3200 has a total of sixteen high-speed output drivers which are grouped into two eight lane JESD204B links. Most of the operating modes use two links with up to eight lanes per link. The lanes and their derived configuration parameters are described in Table 19. For a specified JMODE, the lowest indexed lanes for each link are used while the higher indexed lanes for each link are automatically powered down. Always route the lowest indexed lanes to the logic device.

Table 19. ADC12DJ3200 Lane Assignment and Parameters

Device Pin Designation	Link	DID (User Configured)	LID (Derived)
DA0+/–	A	Set by DID (*JESD204B DID Parameter Register (address = 0x206) [reset = 0x00]*), the effective DID is equal to the DID register setting (DID)	0
DA1+/–			1
DA2+/–			2
DA3+/–			3
DA4+/–			4
DA5+/–			5
DA6+/–			6
DA7+/–			7
DB0+/–	B	Set by DID (*JESD204B DID Parameter Register (address = 0x206) [reset = 0x00]*), the effective DID is equal to the DID register setting plus 1 (DID+1)	0
DB1+/–			1
DB2+/–			2
DB3+/–			3
DB4+/–			4
DB5+/–			5
DB6+/–			6
DB7+/–			7

7.4.3.1 JESD204B Output Data Formats

Output data is formatted in a specific optimized fashion for each JMODE setting. When the DDC is not used (Decimation = 1) the 12-bit offset binary values are mapped into octets. For the DDC mode the 16-bit values (15-bit complex data plus 1 over-range bit) are mapped into octets. The following tables show the specific mapping formats for a single frame. In all mappings the tail bits (T) are 0 (zero). In the tables below, the single channel format samples are defined as Sn, where n is the sample number within the frame. In the dual channel real output formats (DDC bypass and Dec-by-2), the samples are defined as An and Bn, where An are samples from channel A and Bn are samples from channel B. In the complex output formats (Dec-by-4, Dec-by-8, Dec-by-16), the samples are defined as AIn, AQn, BIn and BQn, where AIn and AQn are the in-phase and quadrature-phase samples of channel A and BIn and BQn are the in-phase and quadrature-phase samples of channel B. All samples are formatted as MSB first, LSB last.

Table 20. JMODE 0 (12-bit, Dec-by-1, Single Channel, 8 lanes)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	S0		S8		S16		S24		S32							T
DA1	S2		S10		S18		S26		S34							T
DA2	S4		S12		S20		S28		S36							T
DA3	S6		S14		S22		S30		S38							T
DB0	S1		S9		S17		S25		S33							T
DB1	S3		S11		S19		S27		S35							T
DB2	S5		S13		S21		S29		S37							T
DB3	S7		S15		S23		S31		S39							T

Table 21. JMODE 1 (12-bit, Dec-by-1, Single Channel, 16 lanes)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	S0		S16		S32		S48		S64							T
DA1	S2		S18		S34		S50		S66							T
DA2	S4		S20		S36		S52		S68							T
DA3	S6		S22		S38		S54		S70							T
DA4	S8		S24		S40		S56		S72							T
DA5	S10		S26		S42		S58		S74							T
DA6	S12		S28		S44		S60		S76							T
DA7	S14		S30		S46		S62		S78							T
DB0	S1		S17		S33		S49		S65							T
DB1	S3		S19		S35		S51		S67							T
DB2	S5		S21		S37		S53		S69							T
DB3	S7		S23		S39		S55		S71							T
DB4	S9		S25		S41		S57		S73							T
DB5	S11		S27		S43		S59		S75							T
DB6	S13		S29		S45		S61		S77							T
DB7	S15		S31		S47		S63		S79							T

Table 22. JMODE 2 (12-bit, Dec-by-1, Dual Channel, 8 lanes)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	A0		A4		A8		A12		A16							T
DA1	A1		A5		A9		A13		A17							T
DA2	A2		A6		A10		A14		A18							T
DA3	A3		A7		A11		A15		A19							T
DB0	B0		B4		B8		B12		B16							T
DB1	B1		B5		B9		B13		B17							T
DB2	B2		B6		B10		B14		B18							T
DB3	B3		B7		B11		B15		B19							T

Table 23. JMODE 3 (12-bit, Dec-by-1, Dual Channel, 16 lanes)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	A0		A8		A16		A24		A32							T
DA1	A1		A9		A17		A25		A33							T
DA2	A2		A10		A18		A26		A34							T
DA3	A3		A11		A19		A27		A35							T
DA4	A4		A12		A20		A28		A36							T
DA5	A5		A13		A21		A29		A37							T
DA6	A6		A14		A22		A30		A38							T
DA7	A7		A15		A23		A31		A39							T
DB0	B0		B8		B16		B24		B32							T
DB1	B1		B9		B17		B25		B33							T
DB2	B2		B10		B18		B26		B34							T
DB3	B3		B11		B19		B27		B35							T
DB4	B4		B12		B20		B28		B36							T
DB5	B5		B13		B21		B29		B37							T
DB6	B6		B14		B22		B30		B38							T
DB7	B7		B15		B23		B31		B39							T

Table 24. JMODE 4 (8-bit, Dec-by-1, Single Channel, 4 lanes)

Octet	0	
Nibble	0	1
DA0	S0	
DA1	S2	
DB0	S1	
DB1	S3	

Table 25. JMODE 5 (8-bit, Dec-by-1, Single Channel, 8 lanes)

Octet	0	
Nibble	0	1
DA0	S0	
DA1	S2	
DA2	S4	
DA3	S6	
DB0	S1	
DB1	S3	
DB2	S5	
DB3	S7	

Table 26. JMODE 6 (8-bit, Dec-by-1, Dual Channel, 4 lanes)

Octet	0	
Nibble	0	1
DA0	A0	
DA1	A1	
DB0	B0	
DB1	B1	

Table 27. JMODE 7 (8-bit, Dec-by-1, Dual Channel, 8 lanes)

Octet	0	
Nibble	0	1
DA0	A0	
DA1	A1	
DA2	A2	
DA3	A3	
DB0	B0	
DB1	B1	
DB2	B2	
DB3	B3	

Table 28. JMODE 9 (15-bit, Dec-by-2, Dual Channel, 8 lanes)

Octet	0		1	
Nibble	0	1	2	3
DA0	A0			
DA1	A1			
DA2	A2			
DA3	A3			
DB0	B0			
DB1	B1			
DB2	B2			
DB3	B3			

Table 29. JMODE 10 (15-bit, Dec-by-4, Dual Channel, 4 lanes)

Octet	0		1	
Nibble	0	1	2	3
DA0	AI0			
DA1	AQ0			
DB0	BI0			
DB1	BQ0			

Table 30. JMODE 11 (15-bit, Dec-by-4, Dual Channel, 8 lanes)

Octet	0		1	
Nibble	0	1	2	3
DA0	AI0			
DA1	AI1			
DA2	AQ0			
DA3	AQ1			
DB0	BI0			
DB1	BI1			
DB2	BQ0			
DB3	BQ1			

Table 31. JMODE 12 (12-bit, Dec-by-4, Dual Channel, 16 lanes)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	AI0		AI4		AI8		AI12		AI16							T
DA1	AQ0		AQ4		AQ8		AQ12		AQ16							T
DA2	AI1		AI5		AI9		AI13		AI17							T
DA3	AQ1		AQ5		AQ9		AQ13		AQ17							T
DA4	AI2		AI6		AI10		AI14		AI18							T
DA5	AQ2		AQ6		AQ10		AQ14		AQ218							T
DA6	AI3		AI7		AI11		AI15		AI19							T
DA7	AQ3		AQ7		AQ11		AQ15		AQ19							T
DB0	BI0		BI4		BI8		BI12		BI16							T
DB1	BQ0		BQ4		BQ8		BQ12		BQ16							T
DB2	BI1		BI5		BI9		BI13		BI17							T
DB3	BQ1		BQ5		BQ9		BQ13		BQ17							T
DB4	BI2		BI6		BI10		BI14		BI18							T
DB5	BQ2		BQ6		BQ10		BQ14		BQ218							T
DB6	BI3		BI7		BI11		BI15		BI19							T
DB7	BQ3		BQ7		BQ11		BQ15		BQ19							T

Table 32. JMODE 13 (15-bit, Dec-by-8, Dual Channel, 2 lanes)

Octet	0		1		2		3	
Nibble	0	1	2	3	4	5	6	7
DA0	AI0				AQ0			
DB0	BI0				BQ0			

Table 33. JMODE 14 (15-bit, Dec-by-8, Dual Channel, 4 lanes)

Octet	0		1	
Nibble	0	1	2	3
DA0	AI0			
DA1	AQ0			
DB0	BI0			
DB1	BQ0			

Table 34. JMODE 15 (15-bit, Dec-by-16, Dual Channel, 1 lane)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	AI0				AQ0				BI0				BQ0			

Table 35. JMODE 16 (15-bit, Dec-by-16, Dual Channel, 2 lanes)

Octet	0		1		2		3	
Nibble	0	1	2	3	4	5	6	7
DA0	AI0				AQ0			
DB0	BI0				BQ0			

Table 36. JMODE 17 (8-bit, Dec-by-1, Single Channel, 16 lanes)

Octet	0	
Nibble	0	1
DA0	S0	
DA1	S2	
DA2	S4	
DA3	S6	
DA4	S8	
DA5	S10	
DA6	S12	
DA7	S14	
DB0	S1	
DB1	S3	
DB2	S5	
DB3	S7	
DB4	S9	
DB5	S11	
DB6	S13	
DB7	S15	

Table 37. JMODE 18 (8-bit, Dec-by-1, Dual Channel, 16 lanes)

Octet	0	
Nibble	0	1
DA0	A0	
DA1	A1	
DA2	A2	
DA3	A3	
DA4	A4	
DA5	A5	
DA6	A6	
DA7	A7	
DB0	B0	
DB1	B1	
DB2	B2	
DB3	B3	
DB4	B4	
DB5	B5	
DB6	B6	
DB7	B7	

7.4.3.2 Dual DDC and Redundant Data Mode

When operating in dual channel mode the data from one channel can be routed to both digital down-converter blocks by using DIG_BIND_A or DIG_BIND_B (*Digital Channel Binding Register (address = 0x216) [reset = 0x02]*). This enables down-conversion of two separate captured bands from a single ADC channel. The second ADC can be powered down in this mode by setting PD_ACH or PD_BCH (Device Configuration Register (address = 0x002) [reset = 0x00]).

Additionally, DIG_BIND_A or DIG_BIND_B can be used to provide redundant data to separate digital processors by routing data from one ADC channel to both JESD204B links. Redundant data mode is available for all JMODE modes except for the single channel modes. Both dual DDC mode and redundant data mode are demonstrated in Figure 84 where the data for ADC channel A is routed to both DDCs and then transmitted to a single processor or two processors (for redundancy).

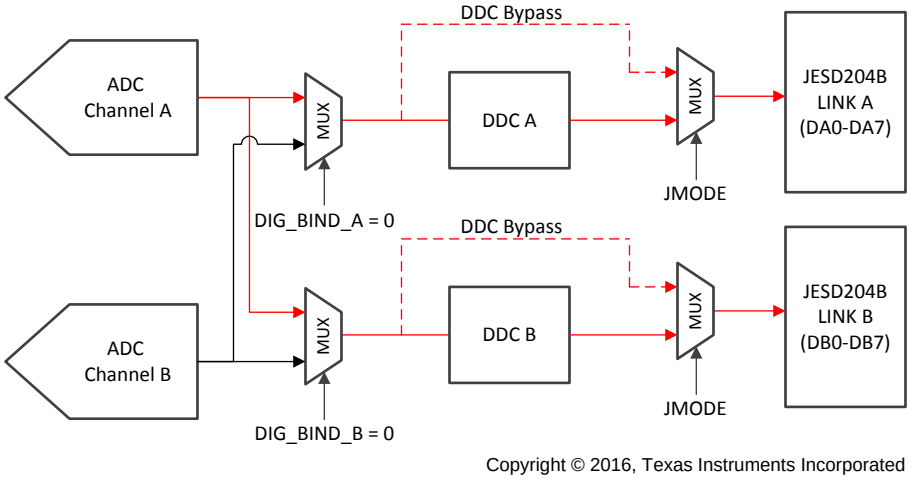


Figure 84. Dual DDC Mode or Redundant Data Mode for Channel A

7.4.4 Power Down Modes

NOTE

Power down of the high speed data outputs (DA0+/– ... DA7+/–, DB0+/– ... DB7+/–) for extended times may reduce performance of the output serializers, especially at high data rates. Please see note beneath Recommended Operating Conditions for more information.

The PD input pin allows the ADC12DJ3200 devices to be entirely powered down. Power down can also be controlled by MODE (*Device Configuration Register (address = 0x002) [reset = 0x00]*). The serial data output drivers are disabled when PD is high. When the device returns to normal operation, the JESD204 link must be re-established, and the ADC pipeline contain meaningless information so the system must wait a sufficient time for the data to be flushed. If power down for power savings is desired the system should power down the supply voltages regulators for VA19, VA11 and VD11 rather than make use of the PD input or MODE settings.

7.4.5 Test Modes

A number of device test modes are available. These modes insert known patterns of information into the device data path for assistance with system debug, development, or characterization.

7.4.5.1 Serializer Test-Mode Details

Test modes are enabled by setting JTEST (*JESD204B Test Pattern Control Register (address = 0x205) [reset = 0x00]*) to the desired test mode. Each test mode is described in detail in the following sections. Regardless of the test mode, the serializer outputs are powered up based on JMODE. The test modes should only be enabled while the JESD204B link is disabled.

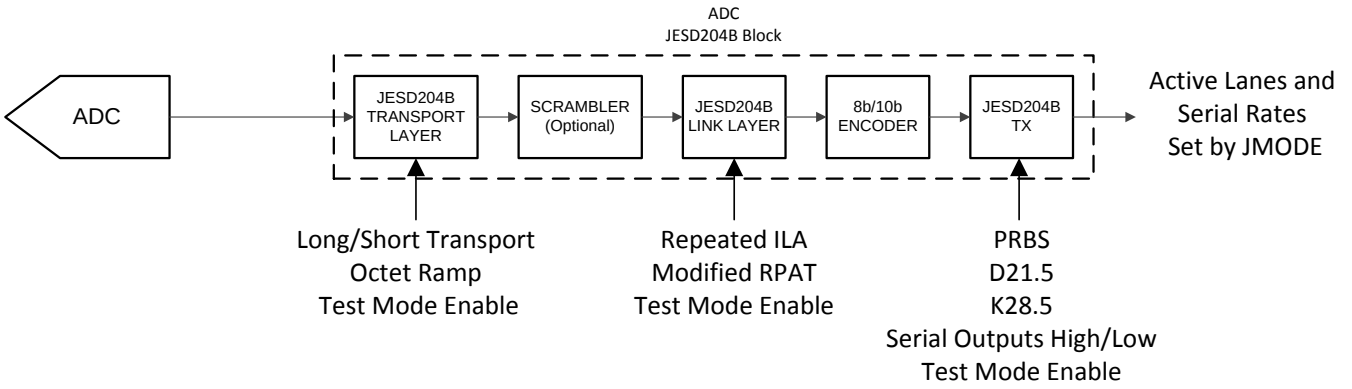


Figure 85. Test-Mode Insertion Points

7.4.5.2 PRBS Test Modes

The PRBS test modes bypass the 8b/10b encoder. These test modes produce pseudo-random bit streams that comply with the ITU-T O.150 specification. These bit streams are used with lab test equipment that can self-synchronize to the bit pattern and therefore the initial phase of the pattern is not defined.

The sequences are defined by a recursive equation. For example, the PRBS7 sequence is defined as shown in Equation 10.

$$y[n] = y[n - 6] \oplus y[n - 7] \quad (10)$$

where bit n is the XOR of bit [n – 6] and bit [n – 7] which are previously transmitted bits

Table 38. PBRS Mode Equations

PRBS TEST MODE	SEQUENCE	SEQUENCE LENGTH (bits)
PRBS7	$y[n] = y[n - 6] \oplus y[n - 7]$	127
PRBS15	$y[n] = y[n - 14] \oplus y[n - 15]$	32767
PRBS23	$y[n] = y[n - 18] \oplus y[n - 23]$	8388607

The initial phase of the pattern is unique for each lane.

7.4.5.3 Ramp Test Mode

In the ramp test mode, the JESD204B link layer operates normally, but the transport layer is disabled and the input from the formatter is ignored. After the ILA sequence, each lane transmits an identical octet stream that increments from 0x00 to 0xFF and repeats.

7.4.5.4 Short and Long Transport Test Mode

JESD204B defines both short and long transport test modes to verify that the transport layers in the transmitter and receiver are operating correctly. ADC12DJ3200 has three different transport layer test patterns depending on the N' value of the specified JMODE (Table 18).

7.4.5.4.1 Short Transport Test Pattern

Short transport test patterns send a predefined octet format that repeats every frame. In the ADC12DJ32000, all of the JMODE configurations that have an N' value of 8 or 12 use the short transport test pattern. Table 39 and Table 40 define the short transport test patterns for N' values of 8 and 12. All applicable lanes are shown, however only the enabled lanes (lowest indexed) for the configured JMODE are used.

Table 39. Short Transport Test Pattern for N' = 8 Modes (Length = 2 Frames)

Frame:	0	1
DA0	0x00	0xFF

Table 39. Short Transport Test Pattern for N' = 8 Modes (Length = 2 Frames) (continued)

Frame:	0	1
DA1	0x01	0xFE
DA2	0x02	0xFD
DA3	0x03	0xFC
DB0	0x00	0xFF
DB1	0x01	0xFE
DB2	0x02	0xFD
DB3	0x03	0xFC

Table 40. Short Transport Test Pattern for N' = 12 Modes (Length = 1 Frame)

Octet	0		1		2		3		4		5		6		7	
Nibble	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	0xF01		0xF02		0xF03		0xF04		0xF05							T
DA1	0xE11		0xE12		0xE13		0xE14		0xE15							T
DA2	0xD21		0xD22		0xD23		0xD24		0xD25							T
DA3	0xC31		0xC32		0xC33		0xC34		0xC35							T
DA4	0xB41		0xB42		0xB43		0xB44		0xB45							T
DA5	0xA51		0xA52		0xA53		0xA54		0xA55							T
DA6	0x961		0x962		0x963		0x964		0x965							T
DA7	0x871		0x872		0x873		0x874		0x875							T
DB0	0xF01		0xF02		0xF03		0xF04		0xF05							T
DB1	0xE11		0xE12		0xE13		0xE14		0xE15							T
DB2	0xD21		0xD22		0xD23		0xD24		0xD25							T
DB3	0xC31		0xC32		0xC33		0xC34		0xC35							T
DB4	0xB41		0xB42		0xB43		0xB44		0xB45							T
DB5	0xA51		0xA52		0xA53		0xA54		0xA55							T
DB6	0x961		0x962		0x963		0x964		0x965							T
DB7	0x871		0x872		0x873		0x874		0x875							T

7.4.5.4.2 Long Transport Test Pattern

The long-transport test mode is used in all of the JMODE modes where N' equals 16. Patterns are generated in accordance with the JESD204B standard and are different for each output format as defined in Table 18. The rules for the pattern are defined below. The length of the test pattern is given by Equation 11. The long transport test pattern is the same for link A and link B, where DAx lanes belong to link A and DBx lanes belong to link B.

Long Test Pattern Length (Frames) = K * ceil((M*S+2) / K) (11)

- Sample Data:
  - Frame 0: Each sample contains N bits, with all samples set to the converter id (CID) plus 1 (CID + 1). CID is defined based on the converter number within the link; note that two links are used in all modes except JMODE 15. Within a link, the converters are numbered by channel (A or B) and in-phase (I) and quadrature-phase (Q) and reset between links. For instance, in JMODE 10, two links are used so channel A and B data is separated into separate links and the in-phase component for each channel has CID = 0 and the quadrature-phase component has CID = 1. In JMODE 15, one link is used, so channel A and B are within the same link and AI has CID = 0, AQ has CID = 1, BI has CID = 2, and BQ has CID = 3.
  - Frame 1: Each sample contains N bits, with each sample (for each converter) set as its individual sample ID (SID) within the frame plus 1 (SID + 1)
  - Frame 2 +: Each sample contains N bits, with the data set to 2^{N-1} for all samples, for example if N is 15, then 2^{N-1} = 16384
- Control Bits (if CS > 0):
  - Frame 0 to M*S–1: The control bit belonging to sample mod(i,S) of converter floor(i,S) set to "1" and all others set to "0", where i is the frame index (i=0 is the first frame of the pattern). Essentially, the control bit

"walks" from the lowest indexed sample to the highest indexed sample and from the lowest indexed converter to highest indexed converter, changing position every frame.

– Frame M*S +: All control bits set to 0

Table 41. Example Long Transport Test Pattern - JMODE = 10, K = 10

TIME →																					Pattern Repeats →	
OCTET NUM.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
DA0	0x0003		0x0002		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x0003	
DA1	0x0004		0x0003		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x0004	
DB0	0x0003		0x0002		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x0003	
DB1	0x0004		0x0003		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x0004	
	Frame n		Frame n + 1		Frame n + 2		Frame n + 3		Frame n + 4		Frame n + 5		Frame n + 6		Frame n + 7		Frame n + 8		Frame n + 9		Frame n + 10	

The pattern starts at the end of the initial lane alignment sequence (ILAS) and repeats indefinitely as long as the link remains running. For more details see JESD204B, section 5.1.6.3.

7.4.5.5 D21.5 Test Mode

In this test mode, the controller transmits a continuous stream of D21.5 characters (alternating 0s and 1s).

7.4.5.6 K28.5 Test Mode

In this test mode, the controller transmits a continuous stream of K28.5 characters.

7.4.5.7 Repeated ILA Test Mode

In this test mode, the JESD204B link layer operates normally, except that the ILA sequence (ILAS) repeats indefinitely instead of starting the data phase. Whenever the receiver issues a synchronization request, the transmitter will initiate code group synchronization. Upon completion of code group synchronization, the transmitter will repeatedly transmit the ILA sequence.

7.4.5.8 Modified RPAT Test Mode

A 12-octet repeating pattern is defined in INCITS TR-35-2004. The purpose of this pattern is to generate white spectral content for JESD204B compliance and jitter testing. Table 42 lists the pattern before and after 8b10b encoding.

Table 42. Modified RPAT Pattern Values

OCTET NUMBER	Dx.y NOTATION	8-BIT INPUT TO 8b10b ENCODER	20b OUTPUT OF 8b10b ENCODER (2 CHARACTERS)
0	D30.5	0xBE	0x86BA6
1	D23.6	0xD7	
2	D3.1	0x23	0xC6475
3	D7.2	0x47	
4	D11.3	0x6B	0xD0E8D
5	D15.4	0x8F	
6	D19.5	0xB3	0xCA8B4
7	D20.0	0x14	
8	D30.2	0x5E	0x7949E
9	D27.7	0xFB	
10	D21.1	0x35	0xAA665
11	D25.2	0x59	

7.4.6 Calibration Modes and Trimming

ADC12DJ3200 has two calibration modes available, foreground calibration and background calibration. When foreground calibration is initiated the ADCs are automatically taken offline and the output data becomes midcode (0x000 in 2's complement) while calibration is occurring. Background calibration allows the ADC to continue normal operation while the ADC cores are calibrated in the background by swapping in a different ADC core to take its place. Additional offset calibration features are available in both Foreground and Background calibration modes. Further, a number of ADC parameters can be trimmed to optimize performance in a user's system.

ADC12DJ3200 consists of a total of six sub-ADCs, each referred to as a "bank", with two banks forming an ADC core. The banks sample out of phase so that each ADC core is two-way interleaved. The six banks form three ADC cores, referred to as ADC A, ADC B and ADC C. In foreground calibration mode, ADC A samples INA+/– and ADC B samples INB+/– in dual channel mode and both ADC A and ADC B sample INA+/– (or INB+/–) in single channel mode. In background calibration modes, the third ADC core, ADC C, is swapped in periodically for ADC A and ADC B so that they can be calibrated without disrupting operation. Figure 86 shows a diagram of the calibration system including labeling of the banks that make up each ADC core. When calibration is performed the linearity, gain and offset voltage for each bank are calibrated to an internally generated calibration signal. The analog inputs can be driven during calibration, both foreground and background, except that when offset calibration (OS_CAL or BGOS_CAL) is used there should be no signals (or aliased signals) near DC for proper estimation of the offset (see Offset Calibration).

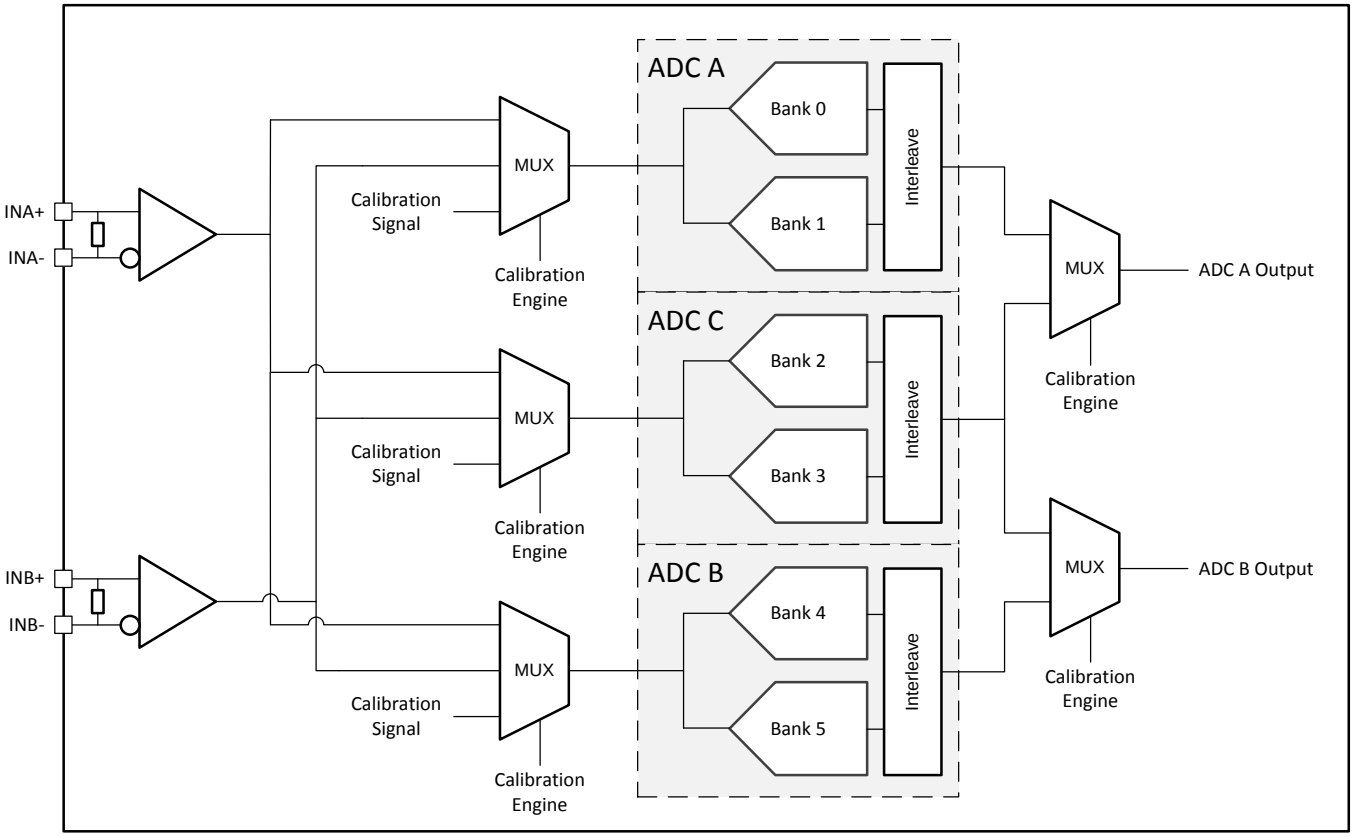


Figure 86. ADC12DJ3200 Calibration System Block Diagram

In addition to calibration, a number of ADC parameters are user controllable to allowing trimming for optimal performance. These include input offset voltage, ADC gain, interleaving timing and input termination resistance. The default trim values are programmed at the factory to unique values for each device which are determined to be optimal at the test system's operating conditions. The user can read the factory programmed values from the trim registers and adjusted as desired. The register fields that control the trimming are labeled according to the

input that is being sampled (INA+/– or INB+/–), the bank that is being trimmed or the ADC core that is being trimmed. It is not expected that the user must change the trim values as operating conditions change, however optimal performance may be obtained by doing so. Any custom trimming must be done on a per device basis due to process variations, meaning that there is no global optimal setting for all parts. See Trimming for information about the available trim parameters and associated registers.

7.4.6.1 Foreground Calibration Mode

Foreground calibration requires the ADC to stop converting the analog input signals during the procedure. Foreground calibration always runs on power up and the user must wait a sufficient time before programming the device to guarantee that the calibration is finished. Foreground calibration can be initiated by triggering the calibration engine. The trigger source can be either the CAL_TRIG pin or CAL_SOFT_TRIG (*Calibration Software Trigger Register (address = 0x06C) [reset = 0x01]*) and is chosen by setting CAL_TRIG_EN (*Calibration Pin Configuration Register (address = 0x06B) [reset = 0x00]*).

7.4.6.2 Background Calibration Mode

Background calibration mode allows the ADC to continuously operate, with no interruption of data. This is accomplished by activating an extra ADC core which is calibrated and then takes over operation for one of the other previously active ADC cores. Once that ADC core is taken off-line it is then calibrated and can in turn take over to allow the next ADC to be calibrated. This process operates continuously, ensuring the ADC cores are always providing the optimum performance regardless of system operating condition changes. Due to the additional active ADC core, Background calibration mode has increased power consumption in comparison to Foreground calibration mode. The low-power background calibration (LPBG) mode discussed next provides reduced average power consumption in comparison with the standard background calibration mode. Background calibration can be enabled by setting CAL_BG (*Calibration Configuration 0 Register (address = 0x062) [reset = 0x01]*). CAL_TRIG_EN should be set to 0 and CAL_SOFT_TRIG should be set to 1.

Great care has been taken to minimize effects on converted data as the core switching process occurs, however, small brief glitches may still be seen on the converter data as the cores are swapped. Please refer to the Typical Characteristic section of the datasheet for examples of the possible glitches in sine-wave and DC signals.

7.4.6.3 Low-Power Background Calibration (LPBG) Mode

Low-power background calibration (LPBG) mode reduces the power-overhead of enabling additional ADC cores. Off-line cores are powered down until ready to be calibrated and put on-line. Set LP_EN=1 to enable the low-power background calibration feature. LP_SLEEP_DLY is used to adjust the amount of time an ADC sleeps before waking up for calibration (if LP_EN=1 and LP_TRIG=0). LP_WAKE_DLY sets how long the core is allowed to stabilize before calibration and being put on-line. LP_TRIG is used to select between an automatic switching process or one that is controlled by the user via CAL_SOFT_TRIG or CAL_TRIG. In this mode there is an increase in power consumption during the ADC core calibration. The power consumption will roughly alternate between the power consumption in foreground calibration when the spare ADC core is sleeping to the power consumption in background calibration when the spare ADC is being calibrated. The power supply network should be designed to be able to handle the transient power requirements for this mode.

7.4.7 Offset Calibration

Foreground calibration and background calibration modes inherently calibrate the offsets of the ADC cores, however the input buffers sits outside of the calibration loop and therefore their offsets are not calibrated by the standard calibration process. In both dual channel mode and single channel mode uncalibrated input buffer offsets result in a shift in the mid-code output (DC offset) with no input. Further, in single channel mode uncalibrated input buffer offsets can result in a fixed spur at $F_S/2$. A separate calibration is provided to correct the input buffer offsets.

There must be no signals at or near DC or aliased signals that fall at or near DC in order to properly calibration the offsets, requiring the system to guarantee this condition during normal operation or have the ability to mute the input signal during calibration. Foreground offset calibration is enabled via CAL_OS and only performs the calibration once as part of the foreground calibration procedure. Background offset calibration is enabled via CAL_BGOS and will continue to correct the offset as part of the background calibration routine to account for operating condition changes. When CAL_BGOS is set the system must guarantee that there are no DC or near DC signals or aliased signals that fall at or near DC during normal operation. Offset calibration can be performed as a foreground operation when using background calibration by setting CAL_OS to 1 before setting CAL_EN, but it will not correct for variations as operating conditions change.

The offset calibration correction uses the input offset voltage trim registers (see Table 43) to correct the offset and therefore must not be written by the user when offset calibration is used. The user can read the calibrated values by reading the OADJ_x_VINy registers, where x is the ADC core and y is the input (INA+/– or INB+/–), after calibration is completed. The values should only be read when FG_DONE is read as 1 when using foreground offset calibration (CAL_OS = 1) and should not be read when using background offset calibration (CAL_BGOS = 1).

7.4.8 Trimming

The parameters that can be trimmed and the associated registers are summarized in Table 43.

Table 43. Trim Register Descriptions

Trim Parameter	Trim Register	Notes
Bandgap reference	BG_TRIM	Measure on BG output pin.
Input termination resistance	RTRIM_x Where x = A for INA+/– or B for INB+/–)	Device must be powered on with a clock applied.
Input offset voltage	OADJ_x_VINy Where x = ADC core (A, B or C) and y = A for INA+/– or B for INB+/–)	A different trim value is allowed for each ADC core (A, B or C) to allow more consistent offset performance in background calibration mode.
INA+/– and INB+/– gain	GAIN_TRIM_x Where x = A for INA+/– or B for INB+/–)	FS_RANGE_A and FS_RANGE_B should be set to default values before trimming the input. FS_RANGE_A and FS_RANGE_B should be used to adjust the full scale input voltage.
INA+/– and INB+/– full scale input voltage	FS_RANGE_x Where x = A for INA+/– or B for INB+/–)	Full scale input voltage adjustment for each input. The default value is effected by GAIN_TRIM_x (x = A or B). GAIN_TRIM_x should be trimmed with FS_RANGE_x set to the default value. FS_RANGE_x can then be used to trim the full scale input voltage.
Intra-ADC core timing (bank timing)	Bx_TIME_y Where x = bank number (0–5) and y = 0° or –90° clock phase	Trims the timing between the two banks of an ADC core (ADC A, B or C) for two clock phases, either 0° or –90°. The –90° clock phase is used in single channel mode only.
Inter-ADC core timing (dual channel mode)	TADJ_A, TADJ_B, TADJ_CA, TADJ_CB	The suffix letter (A, B, CA or CB) indicates the ADC core that is being trimmed. CA indicates that this is the timing trim in background calibration mode for ADC C when it is standing in for ADC A, whereas CB is timing trim for ADC C when it is standing in for ADC B.

Table 43. Trim Register Descriptions (continued)

Trim Parameter	Trim Register	Notes
Inter-ADC core timing (single channel mode)	TADJ_A_FG90, TADJ_B_FG0, TADJ_A_BG90, TADJ_C_BG0, TADJ_C_BG90, TADJ_B_BG0	The middle letter (A, B or C) indicates the ADC core that is being trimmed. FG indicates that it is a trim for foreground calibration while BG indicates background calibration. The suffix of 0 or 90 indicates the clock phase applied to the ADC core. 0 indicates a 0° clock and is sampling in-phase with the clock input. 90 indicates a 90° clock and therefore is sampling out-of-phase with the clock input. These timings must be trimmed for optimal performance if the user prefers to use INB+/– in single channel mode. They are trimmed for INA+/– at the factory.

7.4.9 Offset Filtering

The ADC12DJ3200 has an additional feature which can be enabled to reduce offset related interleaving spurs at Fs/2 and Fs/4 (single input mode only). Offset filtering is enabled via CAL_OSFILT. The OSFILT_BW and OSFILT_SOAK parameters can be adjusted to tradeoff offset spur reduction with potential impact on information in the mission mode signal being processed. These two parameters should be set to the same value under most situations. The DC_RESTORE setting is used to either retain or filter out all DC related content in the signal.

7.5 Programming

7.5.1 Using the Serial Interface

The serial interface is accessed using the following four pins: serial clock (SCLK), serial-data in (SDI), serial-data out (SDO), and serial-interface chip-select ($\overline{SCS}$). Registers access is enabled through the $\overline{SCS}$ pin.

7.5.1.1 $\overline{SCS}$

This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

7.5.1.2 SCLK

Serial data input is accepted at the rising edge of this signal. SCLK has no minimum frequency requirement.

7.5.1.3 SDI

Each register access requires a specific 24-bit pattern at this input. This pattern consists of a read-and-write (R/W) bit, register address, and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed (see *Timing Requirements*).

7.5.1.4 SDO

The SDO signal provides the output data requested by a read command. This output is high impedance during write bus cycles and during the read bit and register address portion of read bus cycles.

Each register access consists of 24 bits, as shown in Figure 87. The first bit is high for a read and low for a write.

The next 15 bits are the address of the register that is to be written to. During write operations, the last 8 bits are the data written to the addressed register. During read operations, the last 8 bits on SDI are ignored, and, during this time, the SDO outputs the data from the addressed register. The serial protocol details are illustrated in Figure 87.

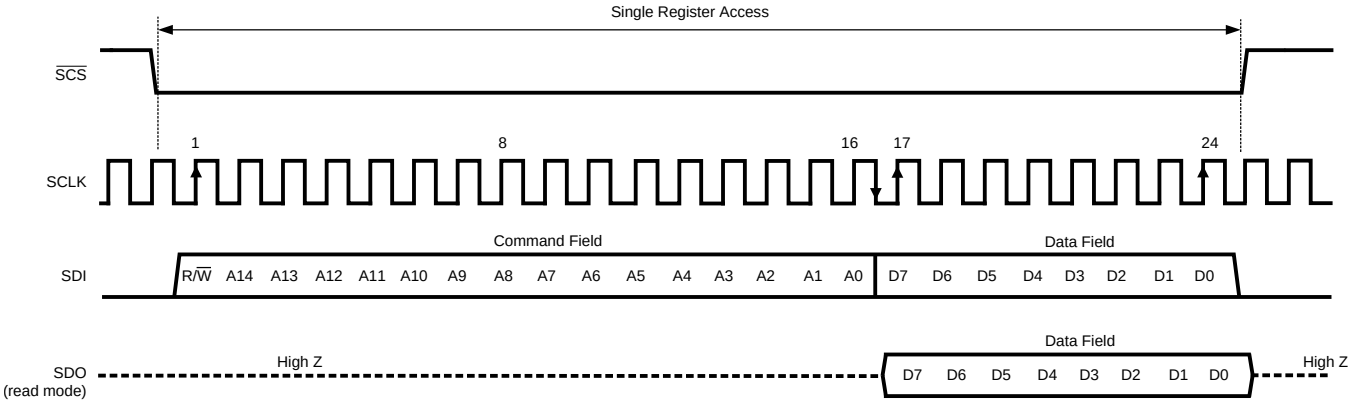


Figure 87. Serial Interface Protocol - Single Read / Write

7.5.1.5 Streaming Mode

The serial interface supports streaming reads and writes. In this mode, the initial 24 bits of the transaction specifics the access type, register address, and data value as normal. Additional clock cycles of write or read data are immediately transferred, as long as the $\overline{SCS}$ input is maintained in the asserted (logic low) state. The register address auto increments (default) or decrements for each subsequent 8 bit transfer of the streaming transaction. The ADDR_ASC bit (register 000h, bits 5 and 2) controls whether the address value ascends (increments) or descends (decrements). Streaming mode can be disabled by setting the ADDR_HOLD bit (*User SPI Configuration Register (address = 0x010) [reset = 0x00]*). The streaming mode transaction details are shown in Figure 88.

Programming (continued)

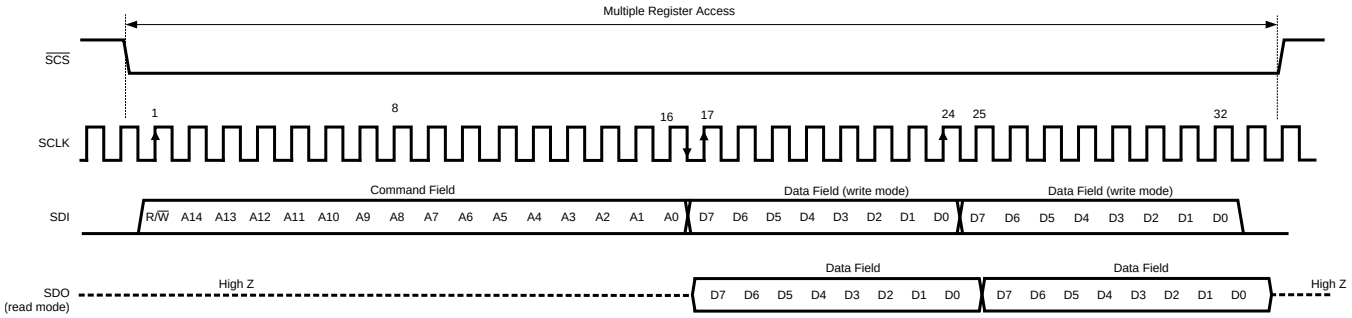


Figure 88. Serial Interface Protocol - Streaming Read / Write

See the *Register Maps* section for detailed information regarding the registers.

NOTE

The serial interface must not be accessed during calibration of the ADC. Accessing the serial interface during this time impairs the performance of the device until the device is calibrated correctly. Writing or reading the serial registers also reduces dynamic performance of the ADC for the duration of the register access time.

7.6 Register Maps

Memory Map

Address	Reset	Acronym	Type	Register Name
Standard SPI-3.0 (0x000 to 0x00F)				
0x000	0x30	CONFIG_A	R/W	Configuration A Register
0x001	Undefined	RESERVED	R	RESERVED
0x002	0x00	DEVICE_CONFIG	R/W	Device Configuration Register
0x003	0x03	CHIP_TYPE	R	Chip Type Register
0x004-0x005	0x0020	CHIP_ID	R	Chip ID Registers
0x006	0x0A	CHIP_VERSION	R	Chip Version Register
0x007-0x00B	Undefined	RESERVED	R	RESERVED
0x00C-0x00D	0x0451	VENDOR_ID	R	Vendor Identification Register
0x00E-0x00F	Undefined	RESERVED	R	RESERVED
User SPI Configuration (0x010 to 0x01F)				
0x010	0x00	USR0	R/W	User SPI Configuration Register
0x011-0x01F	Undefined	RESERVED	R	RESERVED
Miscellaneous Analog Registers (0x020 to 0x047)				
0x020-0x028	Undefined	RESERVED	R	RESERVED
0x029	0x00	CLK_CTRL0	R/W	Clock Control Register 0
0x02A	0x20	CLK_CTRL1	R/W	Clock Control Register 1
0x02B	Undefined	RESERVED	R	RESERVED
0x02C-0x02E	Undefined	SYSREF_POS	R	SYSREF Capture Position Register
0x02F	Undefined	RESERVED	R	RESERVED
0x030-0x031	0xA000	FS_RANGE_A	R/W	INA Full Scale Range Adjust Register
0x032-0x033	0xA000	FS_RANGE_B	R/W	INB Full Scale Range Adjust Register
0x034-0x037	Undefined	RESERVED	R	RESERVED
0x038	0x00	BG_BYPASS	R/W	Internal Reference Bypass Register

Register Maps (continued)

Memory Map (continued)

Address	Reset	Acronym	Type	Register Name
0x039-0x03A	Undefined	RESERVED	R	RESERVED
0x03B	0x00	TMSTP_CTRL	R/W	TMSTP+/- Control Register
0x03C-0x047	Undefined	RESERVED	R	RESERVED
Serializer Registers (0x048 to 0x05F)				
0x048	0x00	SER_PE	R/W	Serializer Pre-Emphasis Control Register
0x049-0x05F	Undefined	RESERVED	R	RESERVED
Calibration Registers (0x060 to 0x0FF)				
0x060	0x01	INPUT_MUX	R/W	Input Mux Control Register
0x061	0x01	CAL_EN	R/W	Calibration Enable Register
0x062	0x01	CAL_CFG0	R/W	Calibration Configuration 0 Register
0x063-0x069	Undefined	RESERVED	R	RESERVED
0x06A	Undefined	CAL_STATUS	R	Calibration Status Register
0x06B	0x00	CAL_PIN_CFG	R/W	Calibration Pin Configuration Register
0x06C	0x01	CAL_SOFT_TRIG	R/W	Calibration Software Trigger Register
0x06D	Undefined	RESERVED	R	RESERVED
0x06E	0x88	CAL_LP	R/W	Low-Power Background Calibration Register
0x06F	Undefined	RESERVED	R	RESERVED
0x070	0x00	CAL_DATA_EN	R/W	Calibration Data Enable Register
0x071	Undefined	CAL_DATA	R/W	Calibration Data Register
0x072-0x079	Undefined	RESERVED	R	RESERVED
0x07A	Undefined	GAIN_TRIM_A	R/W	Channel A Gain Trim Register
0x07B	Undefined	GAIN_TRIM_B	R/W	Channel B Gain Trim Register
0x07C	Undefined	BG_TRIM	R/W	Band-Gap Reference Trim Register
0x07D	Undefined	RESERVED	R	RESERVED
0x07E	Undefined	RTRIM_A	R/W	VINA Input Resistor Trim Register
0x07F	Undefined	RTRIM_B	R/W	VINB Input Resistor Trim Register
0x080	Undefined	TADJ_A_FG90	R/W	Timing Adjustment for A-ADC, Single Channel Mode, Foreground Calibration Register
0x081	Undefined	TADJ_B_FG0	R/W	Timing Adjustment for B-ADC, Single Channel Mode, Foreground Calibration Register
0x082	Undefined	TADJ_A_BG90	R/W	Timing Adjustment for A-ADC, Single Channel Mode, Background Calibration Register
0x083	Undefined	TADJ_C_BG0	R/W	Timing Adjustment for C-ADC, Single Channel Mode, Background Calibration Register
0x084	Undefined	TADJ_C_BG90	R/W	Timing Adjustment for C-ADC, Single Channel Mode, Background Calibration Register
0x085	Undefined	TADJ_B_BG0	R/W	Timing Adjustment for B-ADC, Single Channel Mode, Background Calibration Register
0x086	Undefined	TADJ_A	R/W	Timing Adjustment for A-ADC, Dual Channel Mode Register
0x087	Undefined	TADJ_CA	R/W	Timing Adjustment for C-ADC acting for A-ADC, Dual Channel Mode Register
0x088	Undefined	TADJ_CB	R/W	Timing Adjustment for C-ADC acting for B-ADC, Dual Channel Mode Register
0x089	Undefined	TADJ_B	R/W	Timing Adjustment for B-ADC, Dual Channel Mode Register
0x08A-0x08B	Undefined	OADJ_A_INA	R/W	Offset Adjustment for A-ADC and INA Register
0x08C-0x08D	Undefined	OADJ_A_INB	R/W	Offset Adjustment for A-ADC and INB Register
0x08E-0x08F	Undefined	OADJ_C_INA	R/W	Offset Adjustment for C-ADC and INA Register
0x090-0x091	Undefined	OADJ_C_INB	R/W	Offset Adjustment for C-ADC and INB Register

Register Maps (continued)

Memory Map (continued)

Address	Reset	Acronym	Type	Register Name
0x092-0x093	Undefined	OADJ_B_INA	R/W	Offset Adjustment for B-ADC and INA Register
0x094-0x095	Undefined	OADJ_B_INB	R/W	Offset Adjustment for B-ADC and INB Register
0x096	Undefined	RESERVED	R	RESERVED
0x097	0x00	OSFILT0	R/W	Offset Filtering Control 0
0x098	0x33	OSFILT1	R/W	Offset Filtering Control 1
0x099-0x0FF	Undefined	RESERVED	R	RESERVED
ADC Bank Registers (0x100 to 0x15F)				
0x100-0x101	Undefined	RESERVED	R	RESERVED
0x102	Undefined	B0_TIME_0	R/W	Timing Adjustment for Bank 0 (0° Clock) Register
0x103	Undefined	B0_TIME_90	R/W	Timing Adjustment for Bank 0 (-90° Clock) Register
0x104-0x111	Undefined	RESERVED	R	RESERVED
0x112	Undefined	B1_TIME_0	R/W	Timing Adjustment for Bank 1 (0° Clock) Register
0x113	Undefined	B1_TIME_90	R/W	Timing Adjustment for Bank 1 (-90° Clock) Register
0x114-0x121	Undefined	RESERVED	R	RESERVED
0x122	Undefined	B2_TIME_0	R/W	Timing Adjustment for Bank 2 (0° Clock) Register
0x123	Undefined	B2_TIME_90	R/W	Timing Adjustment for Bank 2 (-90° Clock) Register
0x124-0x131	Undefined	RESERVED	R	RESERVED
0x132	Undefined	B3_TIME_0	R/W	Timing Adjustment for Bank 3 (0° Clock) Register
0x133	Undefined	B3_TIME_90	R/W	Timing Adjustment for Bank 3 (-90° Clock) Register
0x134-0x141	Undefined	RESERVED	R	RESERVED
0x142	Undefined	B4_TIME_0	R/W	Timing Adjustment for Bank 4 (0° Clock) Register
0x143	Undefined	B4_TIME_90	R/W	Timing Adjustment for Bank 4 (-90° Clock) Register
0x144-0x151	Undefined	RESERVED	R	RESERVED
0x152	Undefined	B5_TIME_0	R/W	Timing Adjustment for Bank 5 (0° Clock) Register
0x153	Undefined	B5_TIME_90	R/W	Timing Adjustment for Bank 5 (-90° Clock) Register
0x154-0x15F	Undefined	RESERVED	R	RESERVED
LSB Control Registers (0x160 to 0x1FF)				
0x160	0x00	ENC_LSB	R/W	LSB Control Bit Output Register
0x161-0x1FF	Undefined	RESERVED	R	RESERVED
JESD204B Registers (0x200 to 0x20F)				
0x200	0x01	JESD_EN	R/W	JESD204B Enable Register
0x201	0x02	JMODE	R/W	JESD204B Mode (JMODE) Register
0x202	0x1F	KM1	R/W	JESD204B K Parameter Register
0x203	0x01	JSYNC_N	R/W	JESD204B Manual SYNC Request Register
0x204	0x02	JCTRL	R/W	JESD204B Control Register
0x205	0x00	JTEST	R/W	JESD204B Test Pattern Control Register
0x206	0x00	DID	R/W	JESD204B DID Parameter Register
0x207	0x00	FCHAR	R/W	JESD204B Frame Character Register
0x208	Undefined	JESD_STATUS	R/W	JESD204B / System Status Register
0x209	0x00	PD_CH	R/W	JESD204B Channel Power Down
0x20A	0x00	JEXTRA_A	R/W	JESD204B Extra Lane Enable (Link A)
0x20B	0x00	JEXTRA_B	R/W	JESD204B Extra Lane Enable (Link B)
0x20C-0x20F	Undefined	RESERVED	R	RESERVED
Digital Down Converter Registers (0x210-0x2AF)				
0x210	0x00	DDC_CFG	R/W	DDC Configuration Register
0x211	0xF2	OVR_T0	R/W	Over-range Threshold 0 Register

Register Maps (continued)

Memory Map (continued)

Address	Reset	Acronym	Type	Register Name
0x212	0xAB	OVR_T1	R/W	Over-range Threshold 1 Register
0x213	0x07	OVR_CFG	R/W	Over-range Configuration Register
0x214	0x00	CMODE	R/W	DDC Configuration Preset Mode Register
0x215	0x00	CSEL	R/W	DDC Configuration Preset Select Register
0x216	0x02	DIG_BIND	R/W	Digital Channel Binding Register
0x217-0x218	0x0000	NCO_RDIV	R/W	Rational NCO Reference Divisor Register
0x219	0x02	NCO_SYNC	R/W	NCO Synchronization Register
0x21A-0x21F	Undefined	RESERVED	R	RESERVED
0x220-0x223	0xC0000000	FREQA0	R/W	NCO Frequency (DDC A Preset 0)
0x224-0x225	0x0000	PHASEA0	R/W	NCO Phase (DDC A Preset 0)
0x226-0x227	Undefined	RESERVED	R	RESERVED
0x228-0x22B	0xC0000000	FREQA1	R/W	NCO Frequency (DDC A Preset 1)
0x22C-0x22D	0x0000	PHASEA1	R/W	NCO Phase (DDC A Preset 1)
0x22E-0x22F	Undefined	RESERVED	R	RESERVED
0x230-0x233	0xC0000000	FREQA2	R/W	NCO Frequency (DDC A Preset 2)
0x234-0x235	0x0000	PHASEA2	R/W	NCO Phase (DDC A Preset 2)
0x236-0x237	Undefined	RESERVED	R	RESERVED
0x238-0x23B	0xC0000000	FREQA3	R/W	NCO Frequency (DDC A Preset 3)
0x23C-0x23D	0x0000	PHASEA3	R/W	NCO Phase (DDC A Preset 3)
0x23E-0x23F	Undefined	RESERVED	R	RESERVED
0x240-0x243	0xC0000000	FREQB0	R/W	NCO Frequency (DDC B Preset 0)
0x244-0x245	0x0000	PHASEB0	R/W	NCO Phase (DDC B Preset 0)
0x246-0x247	Undefined	RESERVED	R	RESERVED
0x248-0x24B	0xC0000000	FREQB1	R/W	NCO Frequency (DDC B Preset 1)
0x24C-0x24D	0x0000	PHASEB1	R/W	NCO Phase (DDC B Preset 1)
0x24E-0x24F	Undefined	RESERVED	R	RESERVED
0x250-0x253	0xC0000000	FREQB2	R/W	NCO Frequency (DDC B Preset 2)
0x254-0x255	0x0000	PHASEB2	R/W	NCO Phase (DDC B Preset 2)
0x256-0x257	Undefined	RESERVED	R	RESERVED
0x258-0x25B	0xC0000000	FREQB3	R/W	NCO Frequency (DDC B Preset 3)
0x25C-0x25D	0x0000	PHASEB3	R/W	NCO Phase (DDC B Preset 3)
0x25E-0x296	Undefined	RESERVED	R	RESERVED
0x297	Undefined	SPIN_ID	R	Spin Identification Value
0x298-0x2AF	Undefined	RESERVED	R	RESERVED
SYSREF Calibration Registers (0x2B0 to 0x2BF)				
0x2B0	0x00	SRC_EN	R/W	SYSREF Calibration Enable Register
0x2B1	0x05	SRC_CFG	R/W	SYSREF Calibration Configuration Register
0x2B2-0x2B4	Undefined	SRC_STATUS	R	SYSREF Calibration Status
0x2B5-0x2B7	0x00	TAD	R/W	DEVCLK Aperture Delay Adjustment Register
0x2B8	0x00	TAD_RAMP	R/W	DEVCLK Timing Adjust Ramp Control Register
0x2B9-0x2BF	Undefined	RESERVED	R	RESERVED
Alarm Registers (0x2C0 to 0x2C2)				
0x2C0	Undefined	ALARM	R	Alarm Interrupt Status Register
0x2C1	0x1F	ALM_STATUS	R/W	Alarm Status Register
0x2C2	0x1F	ALM_MASK	R/W	Alarm Mask Register

7.6.1 Register Descriptions

7.6.1.1 Standard SPI-3.0 (0x000 to 0x00F)

Table 44. Standard SPI-3.0 Registers

Address	Reset	Acronym	Register Name	Section
0x000	0x30	CONFIG_A	Configuration A Register	Configuration A Register (address = 0x000) [reset = 0x30]
0x001	Undefined	RESERVED	RESERVED	
0x002	0x00	DEVICE_CONFIG	Device Configuration Register	Device Configuration Register (address = 0x002) [reset = 0x00]
0x003	0x03	CHIP_TYPE	Chip Type Register	Chip Type Register (address = 0x003) [reset = 0x03]
0x004-0x005	0x0020	CHIP_ID	Chip ID Registers	Chip ID Register (address = 0x004 to 0x005) [reset = 0x0020]
0x006	0x0A	CHIP_VERSION	Chip Version Register	Chip Version Register (address = 0x006) [reset = 0x01]
0x007-0x00B	Undefined	RESERVED	RESERVED	
0x00C-0x00D	0x0451	VENDOR_ID	Vendor Identification Register	Vendor Identification Register (address = 0x00C to 0x00D) [reset = 0x0451]
0x00E-0x00F	Undefined	RESERVED	RESERVED	

7.6.1.1.1 Configuration A Register (address = 0x000) [reset = 0x30]

Figure 89. Configuration A Register (CONFIG_A)

7	6	5	4	3	2	1	0
SOFT_RESET	RESERVED	ADDR_ASC	SDO_ACTIVE	RESERVED			
R/W-0	R-0	R/W-1	R-1	R-0000			

Table 45. CONFIG_A Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RESET	R/W	0	Setting this bit results in full reset of the device. This bit is self-clearing. After writing this bit, the device may take up to 750 ns to reset. During this time, do not perform any SPI transactions.
6	RESERVED	R	0	RESERVED
5	ADDR_ASC	R/W	1	0: descend – decrement address while streaming reads/writes 1: ascend – increment address while streaming reads/writes (default)
4	SDO_ACTIVE	R	1	Always returns 1 indicating that device always uses 4-wire SPI mode
3-0	RESERVED	R	0000	RESERVED

7.6.1.1.2 Device Configuration Register (address = 0x002) [reset = 0x00]

Figure 90. Device Configuration Register (DEVICE_CONFIG)

7	6	5	4	3	2	1	0
RESERVED						MODE	
R-0000 00						R/W-00	

Table 46. DEVICE_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0000 00	RESERVED
1-0	MODE	R/W	00	SPI 3.0 specification has 1 as low power functional mode, 2 as low power fast resume and 3 as power-down. This chip does not support these modes. 0: Normal Operation – full power and full performance (default) 1: Normal Operation – full power and full performance 2: Power Down - Everything powered down. Only use for brief periods of time to calibrate on-chip Temperature Diode measurement. Please see note beneath Recommended Operating Conditions for more information. 3: Power Down - Everything powered down. Only use for brief periods of time to calibrate on-chip Temperature Diode measurement. Please see note beneath Recommended Operating Conditions for more information.

7.6.1.1.3 Chip Type Register (address = 0x003) [reset = 0x03]

Figure 91. Chip Type Register (CHIP_TYPE)

7	6	5	4	3	2	1	0
RESERVED				CHIP_TYPE			
R-0000				R-0011			

Table 47. CHIP_TYPE Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	RESERVED
3-0	CHIP_TYPE	R	0011	Always returns 0x3, indicating that the part is a high speed ADC.

7.6.1.1.4 Chip ID Register (address = 0x004 to 0x005) [reset = 0x0020]

Figure 92. Chip ID Register (CHIP_ID)

15	14	13	12	11	10	9	8
CHIP_ID[15:8]							
R-0x00h							
7	6	5	4	3	2	1	0
CHIP_ID[7:0]							
R-0x20h							

Table 48. CHIP_ID Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CHIP_ID	R	0x0020h	Always returns 0x0020 to indicate that this chip is an ADC12DJ3200

7.6.1.1.5 Chip Version Register (address = 0x006) [reset = 0x01]

Figure 93. Chip Version Register (CHIP_VERSION)

7	6	5	4	3	2	1	0
CHIP_VERSION							
R-0000 1010							

Table 49. CHIP_VERSION Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHIP_VERSION	R	0000 1010	Chip version, returns 0x0A

7.6.1.1.6 Vendor Identification Register (address = 0x00C to 0x00D) [reset = 0x0451]

Figure 94. Vendor Identification Register (VENDOR_ID)

15	14	13	12	11	10	9	8
VENDOR_ID[15:8]							
R-0x04h							
7	6	5	4	3	2	1	0
VENDOR_ID[7:0]							
R-0x51h							

Table 50. VENDOR_ID Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VENDOR_ID	R	0x0451h	Always returns 0x0451 (TI Vendor ID)

7.6.1.2 User SPI Configuration (0x010 to 0x01F)

Table 51. User SPI Configuration Registers

Address	Reset	Acronym	Register Name	Section
0x010	0x00	USR0	User SPI Configuration Register	User SPI Configuration Register (address = 0x010) [reset = 0x00]
0x011-0x01F	Undefined	RESERVED	RESERVED	

7.6.1.2.1 User SPI Configuration Register (address = 0x010) [reset = 0x00]

Figure 95. User SPI Configuration Register (USR0)

7	6	5	4	3	2	1	0
RESERVED							ADDR_HOLD
R-0000 000							R/W-0

Table 52. USR0 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	
0	ADDR_HOLD	R/W	0	0: Use ADDR_ASC bit to define what happens to address during streaming (default). 1: Address stays static throughout streaming operation. Useful for reading/writing calibration vector information at CAL_DATA register.

7.6.1.3 Miscellaneous Analog Registers (0x020 to 0x047)

Table 53. Miscellaneous Analog Registers

Address	Reset	Acronym	Register Name	Section
0x020-0x028	Undefined	RESERVED	RESERVED	
0x029	0x00	CLK_CTRL0	Clock Control Register 0	Clock Control Register 0 (address = 0x029) [reset = 0x00]
0x02A	0x20	CLK_CTRL1	Clock Control Register 1	Clock Control Register 1 (address = 0x02A) [reset = 0x00]
0x02B	Undefined	RESERVED	RESERVED	
0x02C-0x02E	Undefined	SYSREF_POS	SYSREF Capture Position Register	SYSREF Capture Position Register (address = 0x02C-0x02E) [reset = Undefined]
0x02F	Undefined	RESERVED	RESERVED	
0x030-0x031	0xA000	FS_RANGE_A	INA Full Scale Range Adjust Register	INA Full Scale Range Adjust Register (address = 0x030-0x031) [reset = 0xA000]
0x032-0x033	0xA000	FS_RANGE_B	INB Full Scale Range Adjust Register	INB Full Scale Range Adjust Register (address = 0x032-0x033) [reset = 0xA000]
0x034-0x037	Undefined	RESERVED	RESERVED	
0x038	0x00	BG_BYPASS	Internal Reference Bypass Register	Internal Reference Bypass Register (address = 0x038) [reset = 0x00]
0x039-0x03A	Undefined	RESERVED	RESERVED	
0x03B	0x00	SYNC_CTRL	TMSTP+/- Control Register	TMSTP+/- Control Register (address = 0x03B) [reset = 0x00]
0x03C-0x047	Undefined	RESERVED	RESERVED	

7.6.1.3.1 Clock Control Register 0 (address = 0x029) [reset = 0x00]

Figure 96. Clock Control Register 0 (CLK_CTRL0)

7	6	5	4	3	2	1	0
RESERVED	SYSREF_PROC_EN	SYSREF_RECV_EN	SYSREF_ZOOM	SYSREF_SEL			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0000			

Table 54. CLK_CTRL0 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	RESERVED
6	SYSREF_PROC_EN	R/W	0	Enable the SYSREF processor. This must be set to allow the part to process SYSREF events. SYSREF_RECV_EN must be set before setting SYSREF_PROC_EN.
5	SYSREF_RECV_EN	R/W	0	Set this bit to enable the SYSREF receiver circuit
4	SYSREF_ZOOM	R/W	0	Set this bit to “zoom” in the SYSREF strobe status (impacts SYSREF_POS)
3-0	SYSREF_SEL	R/W	0000	Set this field to select which SYSREF delay to use. Set this based on the results returned by SYSREF_POS. You must set this to 0 to use SYSREF Calibration.

7.6.1.3.2 Clock Control Register 1 (address = 0x02A) [reset = 0x00]

Figure 97. Clock Control Register 1 (CLK_CTRL1)

7	6	5	4	3	2	1	0
RESERVED					DEVCLK_LVPECL_EN	SYSREF_LVPECL_EN	SYSREF_INVERTED
R/W-0010 0					R/W-0	R/W-0	R/W-0

Table 55. CLK_CTRL1 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0010 0	RESERVED
2	DEVCLK_LVPECL_EN	R/W	0	Activate low voltage PECL mode for DEVCLK
1	SYSREF_LVPECL_EN	R/W	0	Activate low voltage PECL mode for SYSREF
0	SYSREF_INVERTED	R/W	0	Inverts the SYSREF signal used for alignment

7.6.1.3.3 SYSREF Capture Position Register (address = 0x02C-0x02E) [reset = Undefined]

Figure 98. SYSREF Capture Position Register (SYSREF_POS)

23	22	21	20	19	18	17	16
SYSREF_POS[23:16]							
R-Undefined							
15	14	13	12	11	10	9	8
SYSREF_POS[15:8]							
R-Undefined							
7	6	5	4	3	2	1	0
SYSREF_POS[7:0]							
R-Undefined							

Table 56. SYSREF_POS Field Descriptions

Bit	Field	Type	Reset	Description
23-0	SYSREF_POS	R	Undefined	Returns a 24-bit status value that indicates the position of the SYSREF edge with respect to DEVCLK. Use this to program SYSREF_SEL.

7.6.1.3.4 INA Full Scale Range Adjust Register (address = 0x030-0x031) [reset = 0xA000]

Figure 99. INA Full Scale Range Adjust Register (FS_RANGE_A)

15	14	13	12	11	10	9	8
FS_RANGE_A[15:8]							
R/W-0xA0h							
7	6	5	4	3	2	1	0
FS_RANGE_A[7:0]							
R/W-0x00h							

Table 57. FS_RANGE_A Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FS_RANGE_A	R/W	0xA000h	Enables adjustment of the analog full scale range for INA 0x0000: Settings below 0x2000 may result in degraded device performance. 0x2000: 500 mVpp - Recommended minimum setting. 0xA000: 800 mVpp (default) 0xFFFF: 1000 mVpp

7.6.1.3.5 INB Full Scale Range Adjust Register (address = 0x032-0x033) [reset = 0xA000]

Figure 100. INB Full Scale Range Adjust Register (FS_RANGE_B)

15	14	13	12	11	10	9	8
FS_RANGE_B[15:8]							
R/W-0xA0							
7	6	5	4	3	2	1	0
FS_RANGE_B[7:0]							
R/W-0x00							

Table 58. FS_RANGE_B Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FS_RANGE_B	R/W	0xA000h	Enables adjustment of the analog full scale range for INB 0x0000: Settings below 0x2000 may result in degraded device performance. 0x2000: 500 mVpp - Recommended minimum setting. 0xA000: 800 mVpp (default) 0xFFFF: 1000 mVpp

7.6.1.3.6 Internal Reference Bypass Register (address = 0x038) [reset = 0x00]

Figure 101. Internal Reference Bypass Register (BG_BYPASS)

7	6	5	4	3	2	1	0
RESERVED							BG_BYPASS
R/W-0000 000							R/W-0

Table 59. BG_BYPASS Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	BG_BYPASS	R/W	0	When set, VA11 is used as the voltage reference instead of the internal reference

7.6.1.3.7 TMSTP+/- Control Register (address = 0x03B) [reset = 0x00]

Figure 102. TMSTP+/- Control Register (TMSTP_CTRL)

7	6	5	4	3	2	1	0
RESERVED						TMSTP_LVPECL_EN	TMSTP_RECV_EN
R/W-0000 00						R/W-0	R/W-0

Table 60. TMSTP_CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1	TMSTP_LVPECL_EN	R/W	0	When set, activates the low voltage PECL mode for the differential TMSTP+/- input
0	TMSTP_RECV_EN	R/W	0	Enables the differential TMSTP+/- input

7.6.1.4 Serializer Registers (0x048 to 0x05F)

Table 61. Serializer Registers

Address	Reset	Acronym	Register Name	Section
0x048	0x00	SER_PE	Serializer Pre-Emphasis Control Register	
0x049-0x05F	Undefined	RESERVED	RESERVED	

7.6.1.4.1 Serializer Pre-Emphasis Control Register (address = 0x048) [reset = 0x00]

Figure 103. Serializer Pre-Emphasis Control Register (SER_PE)

7	6	5	4	3	2	1	0
RESERVED				SER_PE			
R/W-0000				R/W-0000			

Table 62. SER_PE Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3-0	SER_PE	R/W	0000	Sets the pre-emphasis for the serial lanes to compensate for the low-pass response of the PCB trace. This is a global setting that affects all 16 lanes.

7.6.1.5 Calibration Registers (0x060 to 0x0FF)

Table 63. Calibration Registers

Address	Reset	Acronym	Register Name	Section
0x060	0x01	INPUT_MUX	Input Mux Control Register	Input Mux Control Register (address = 0x060) [reset = 0x01]
0x061	0x01	CAL_EN	Calibration Enable Register	Calibration Enable Register (address = 0x061) [reset = 0x01]
0x062	0x01	CAL_CFG0	Calibration Configuration 0 Register	Calibration Configuration 0 Register (address = 0x062) [reset = 0x01]
0x063-0x069	Undefined	RESERVED	RESERVED	
0x06A	Undefined	CAL_STATUS	Calibration Status Register	Calibration Status Register (address = 0x06A) [reset = Undefined]
0x06B	0x00	CAL_PIN_CFG	Calibration Pin Configuration Register	Calibration Pin Configuration Register (address = 0x06B) [reset = 0x00]
0x06C	0x01	CAL_SOFT_TRIG	Calibration Software Trigger Register	Calibration Software Trigger Register (address = 0x06C) [reset = 0x01]
0x06D	Undefined	RESERVED	RESERVED	
0x06E	0x88	CAL_LP	Low-Power Background Calibration Register	Low-Power Background Calibration Register (address = 0x06E) [reset = 0x88]
0x06F	Undefined	RESERVED	RESERVED	
0x070	0x00	CAL_DATA_EN	Calibration Data Enable Register	Calibration Data Enable Register (address = 0x070) [reset = 0x00]
0x071	Undefined	CAL_DATA	Calibration Data Register	Calibration Data Register (address = 0x071) [reset = Undefined]
0x072-0x079	Undefined	RESERVED	RESERVED	
0x07A	Undefined	GAIN_TRIM_A	Channel A Gain Trim Register	Channel A Gain Trim Register (address = 0x07A) [reset = Undefined]
0x07B	Undefined	GAIN_TRIM_B	Channel B Gain Trim Register	Channel B Gain Trim Register (address = 0x07B) [reset = Undefined]
0x07C	Undefined	BG_TRIM	Band-Gap Reference Trim Register	Band-Gap Reference Trim Register (address = 0x07C) [reset = Undefined]
0x07D	Undefined	RESERVED	RESERVED	
0x07E	Undefined	RTRIM_A	VINA Input Resistor Trim Register	VINA Input Resistor Trim Register (address = 0x07E) [reset = Undefined]
0x07F	Undefined	RTRIM_B	VINB Input Resistor Trim Register	VINB Input Resistor Trim Register (address = 0x07F) [reset = Undefined]
0x080	Undefined	TADJ_A_FG90	Timing Adjustment for A-ADC, Single Channel Mode, Foreground Calibration Register	Timing Adjust for A-ADC, Single Channel Mode, Foreground Calibration Register (address = 0x080) [reset = Undefined]
0x081	Undefined	TADJ_B_FG0	Timing Adjustment for B-ADC, Single Channel Mode, Foreground Calibration Register	Timing Adjust for B-ADC, Single Channel Mode, Foreground Calibration Register (address = 0x081) [reset = Undefined]
0x082	Undefined	TADJ_A_BG90	Timing Adjustment for A-ADC, Single Channel Mode, Background Calibration Register	Timing Adjust for A-ADC, Single Channel Mode, Background Calibration Register (address = 0x082) [reset = Undefined]
0x083	Undefined	TADJ_C_BG0	Timing Adjustment for C-ADC, Single Channel Mode, Background Calibration Register	Timing Adjust for C-ADC, Single Channel Mode, Background Calibration Register (address = 0x084) [reset = Undefined]
0x084	Undefined	TADJ_C_BG90	Timing Adjustment for C-ADC, Single Channel Mode, Background Calibration Register	Timing Adjust for C-ADC, Single Channel Mode, Background Calibration Register (address = 0x084) [reset = Undefined]
0x085	Undefined	TADJ_B_BG0	Timing Adjustment for B-ADC, Single Channel Mode, Background Calibration Register	Timing Adjust for B-ADC, Single Channel Mode, Background Calibration Register (address = 0x085) [reset = Undefined]
0x086	Undefined	TADJ_A	Timing Adjustment for A-ADC, Dual Channel Mode Register	Timing Adjust for A-ADC, Dual Channel Mode Register (address = 0x086) [reset = Undefined]
0x087	Undefined	TADJ_CA	Timing Adjustment for C-ADC acting for A-ADC, Dual Channel Mode Register	Timing Adjust for C-ADC acting for A-ADC, Dual Channel Mode Register (address = 0x087) [reset = Undefined]
0x088	Undefined	TADJ_CB	Timing Adjustment for C-ADC acting for B-ADC, Dual Channel Mode Register	Timing Adjust for C-ADC acting for B-ADC, Dual Channel Mode Register (address = 0x088) [reset = Undefined]

Table 63. Calibration Registers (continued)

Address	Reset	Acronym	Register Name	Section
0x089	Undefined	TADJ_B	Timing Adjustment for B-ADC, Dual Channel Mode Register	Timing Adjust for B-ADC, Dual Channel Mode Register (address = 0x089) [reset = Undefined]
0x08A-0x08B	Undefined	OADJ_A_INA	Offset Adjustment for A-ADC and INA Register	Offset Adjustment for A-ADC and INA Register (address = 0x08A-0x08B) [reset = Undefined]
0x08C-0x08D	Undefined	OADJ_A_INB	Offset Adjustment for A-ADC and INB Register	Offset Adjustment for A-ADC and INB Register (address = 0x08C-0x08D) [reset = Undefined]
0x08E-0x08F	Undefined	OADJ_C_INA	Offset Adjustment for C-ADC and INA Register	Offset Adjustment for C-ADC and INA Register (address = 0x08E-0x08F) [reset = Undefined]
0x090-0x091	Undefined	OADJ_C_INB	Offset Adjustment for C-ADC and INB Register	Offset Adjustment for C-ADC and INB Register (address = 0x090-0x091) [reset = Undefined]
0x092-0x093	Undefined	OADJ_B_INA	Offset Adjustment for B-ADC and INA Register	Offset Adjustment for B-ADC and INA Register (address = 0x092-0x093) [reset = Undefined]
0x094-0x095	Undefined	OADJ_B_INB	Offset Adjustment for B-ADC and INB Register	Offset Adjustment for B-ADC and INB Register (address = 0x094-0x095) [reset = Undefined]
0x096	Undefined	RESERVED	RESERVED	
0x097	0x00	0SFILT0	Offset Filtering Control 0	Offset Filtering Control 0 Register (address = 0x097) [reset = 0x00]
0x098	0x33	OSFILT1	Offset Filtering Control 1	Offset Filtering Control 1 Register (address = 0x098) [reset = 0x33]
0x099-0x0FF	Undefined	RESERVED	RESERVED	

7.6.1.5.1 Input Mux Control Register (address = 0x060) [reset = 0x01]

Figure 104. Input Mux Control Register (INPUT_MUX)

7	6	5	4	3	2	1	0
RESERVED			DUAL_INPUT	RESERVED		SINGLE_INPUT	
R/W-000			R/W-0	R/W-00		R/W-01	

Table 64. INPUT_MUX Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	RESERVED
4	DUAL_INPUT	R/W	0	Select inputs for dual channel modes. If JMODE is selecting a single channel mode, this register has no effect. 0: A channel samples INA, B channel samples INB (no swap) (default) 1: A channel samples INB, B channel samples INA (swap)
3-2	RESERVED	R/W	00	RESERVED
1-0	SINGLE_INPUT	R/W	01	Defines which input is sampled in single channel mode. If JMODE is not selecting a single channel mode, this register has no effect. 0: RESERVED 1: INA is used (default) 2: INB is used 3: RESERVED

7.6.1.5.2 Calibration Enable Register (address = 0x061) [reset = 0x01]

Figure 105. Calibration Enable Register (CAL_EN)

7	6	5	4	3	2	1	0
RESERVED							CAL_EN
R/W-0000 000							R/W-1

Table 65. CAL_EN Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	CAL_EN	R/W	1	Calibration Enable. Set high to run calibration. Set low to hold calibration in reset to program new calibration settings. Clearing CAL_EN also resets the clock dividers that clock the digital block and JESD204B interface. Some calibration registers require clearing CAL_EN before making any changes. All registers with this requirement contain a note in their descriptions. After changing the registers, set CAL_EN to re-run calibration with the new settings. Always set CAL_EN before setting JESD_EN. Always clear JESD_EN before clearing CAL_EN.

7.6.1.5.3 Calibration Configuration 0 Register (address = 0x062) [reset = 0x01]

Only change this register while CAL_EN is 0.

Figure 106. Calibration Configuration 0 Register (CAL_CFG0)

7	6	5	4	3	2	1	0
RESERVED			CAL_OSFILT	CAL_BGOS	CAL_OS	CAL_BG	CAL_FG
R/W-000			R/W-0	R/W-0	R/W-0	R/W-0	R/W-1

Table 66. CAL_CFG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0000	RESERVED
4	CAL_OSFILT	R/W	0	Enable offset filtering by setting this bit high.
3	CAL_BGOS	R/W	0	0 : Disable background offset calibration (default) 1: Enable background offset calibration (requires CAL_BG to be set).
2	CAL_OS	R/W	0	0 : Disable foreground offset calibration (default) 1: Enable foreground offset calibration (requires CAL_FG to be set)
1	CAL_BG	R/W	0	0 : Disable background calibration (default) 1: Enable background calibration
0	CAL_FG	R/W	1	0 : Reset calibration values, skip foreground calibration 1: Reset calibration values, then run foreground calibration (default)

7.6.1.5.4 Calibration Status Register (address = 0x06A) [reset = Undefined]

Figure 107. Calibration Status Register (CAL_STATUS)

7	6	5	4	3	2	1	0
RESERVED						CAL_STOPPED	FG_DONE
R						R	R

Table 67. CAL_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R		RESERVED
1	CAL_STOPPED	R		This bit will return a 1 when background calibration has successfully stopped at the requested phase. This bit will return a 0 once calibration has started operating again. If background calibration is disabled, this bit will be set once foreground calibration is completed or skipped.
0	FG_DONE	R		This bit is set high when foreground calibration has completed

7.6.1.5.5 Calibration Pin Configuration Register (address = 0x06B) [reset = 0x00]

Figure 108. Calibration Pin Configuration Register (CAL_PIN_CFG)

7	6	5	4	3	2	1	0
RESERVED					CAL_STATUS_SEL		CAL_TRIG_EN
R/W-0000 0					R/W-00		R/W-0

Table 68. CAL_PIN_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0000 0	RESERVED
2-1	CAL_STATUS_SEL	R/W	00	0: CALSTAT output pin matches FG_DONE 1: RESERVED 2: CALSTAT output pin matches ALARM 3: CALSTAT output pin is always low.
0	CAL_TRIG_EN	R/W	0	Choose hardware or software trigger source 0: Use the CAL_SOFT_TRIG register for the calibration trigger. The CAL_TRIG input is disabled (ignored). 1: Use the CAL_TRIG input for the calibration trigger. The CAL_SOFT_TRIG register is ignored.

7.6.1.5.6 Calibration Software Trigger Register (address = 0x06C) [reset = 0x01]

Figure 109. Calibration Software Trigger Register (CAL_SOFT_TRIG)

7	6	5	4	3	2	1	0
RESERVED							CAL_SOFT_TRIG
R/W-0000 000							R/W-1

Table 69. CAL_SOFT_TRIG Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	CAL_SOFT_TRIG	R/W	1	CAL_SOFT_TRIG is a software bit to provide the functionality of the CAL_TRIG input. Program CAL_TRIG_EN=0 to use CAL_SOFT_TRIG for the calibration trigger. Note: If no calibration trigger is needed, leave CAL_TRIG_EN=0 and CAL_SOFT_TRIG=1 (trigger set high).

7.6.1.5.7 Low-Power Background Calibration Register (address = 0x06E) [reset = 0x88]

Figure 110. Low-Power Background Calibration Register (CAL_LP)

7	6	5	4	3	2	1	0
LP_SLEEP_DLY			LP_WAKE_DLY		RESERVED	LP_TRIG	LP_EN
R/W-010			R/W-01		R/W-0	R/W-0	R/W-0

Table 70. CAL_LP Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LP_SLEEP_DLY	R/W	010	Adjust how long an ADC sleeps before waking up for calibration (only applys when LP_EN=1 and LP_TRIG=0). Values below 4 are not recommended due to limited overall power reduction benefits. 0: Sleep Delay = $(2^3+1)*256*t_{DEVCLK}$ 1: Sleep Delay = $(2^{15}+1)*256*t_{DEVCLK}$ 2: Sleep Delay = $(2^{18}+1)*256*t_{DEVCLK}$ 3: Sleep Delay = $(2^{21}+1)*256*t_{DEVCLK}$ 4: Sleep Delay = $(2^{24}+1)*256*t_{DEVCLK}$: Default approximately 1338ms with 3.2 GHz clock. 5: Sleep Delay = $(2^{27}+1)*256*t_{DEVCLK}$ 6: Sleep Delay = $(2^{30}+1)*256*t_{DEVCLK}$ 7: Sleep Delay = $(2^{33}+1)*256*t_{DEVCLK}$
4-3	LP_WAKE_DLY	R/W	01	Adjust how much time is given up for settling before calibrating an ADC after it wakes up (only applies when LP_EN=1). Values lower than 1 are not recommended as there will be insufficient time for the core to stabilize before calibration begins. 0:Wake Delay = $(2^3+1)*256*t_{DEVCLK}$ 1: Wake Delay = $(2^{18}+1)*256*t_{DEVCLK}$: Default approximately 21ms with 3.2 GHz clock. 2: Wake Delay = $(2^{21}+1)*256*t_{DEVCLK}$ 3: Wake Delay = $(2^{24}+1)*256*t_{DEVCLK}$
2	RESERVED	R/W	0	RESERVED
1	LP_TRIG	R/W	0	0: ADC sleep duration is set by LP_SLEEP_DLY (autonomous mode). 1: ADCs sleep until woken by a trigger. An ADC is awoken when the calibration trigger (CAL_SOFT_TRIG bit or CAL_TRIG input) is low.
0	LP_EN	R/W	0	0: Disable low-power background calibration (default) 1: Enable low-power background calibration (only applies when CAL_BG=1).

7.6.1.5.8 Calibration Data Enable Register (address = 0x070) [reset = 0x00]

Figure 111. Register (CAL_DATA_EN)

7	6	5	4	3	2	1	0
RESERVED							CAL_DATA_EN
R/W-0000 000							R/W-0

Table 71. CAL_DATA_EN Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	CAL_DATA_EN	R/W	0	Set this bit to enable the CAL_DATA register to enable reading and writing of calibration data. See Calibration Data Read/Write for more information.

7.6.1.5.9 Calibration Data Register (address = 0x071) [reset = Undefined]

Figure 112. Calibration Data Register (CAL_DATA)

7	6	5	4	3	2	1	0
CAL_DATA							
R/W							

Table 72. CAL_DATA Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CAL_DATA	R/W	Undefined	After setting CAL_DATA_EN, repeated reads of this register will return all the calibration values for the ADCs. Repeated writes of this register will input all the calibration values for the ADCs. To read the calibration data, read the register 673 times. To write the vector, write the register 673 times with previously stored calibration data. To speed up the read/write operation, set ADDR_HOLD=1 and use streaming read or write process. IMPORTANT: Accessing the CAL_DATA register while CAL_STOPPED=0 will corrupt the calibration. Also, stopping the process before reading or writing 673 times will leave the calibration data in an invalid state.

7.6.1.5.10 Channel A Gain Trim Register (address = 0x07A) [reset = Undefined]

Figure 113. Channel A Gain Trim Register (GAIN_TRIM_A)

7	6	5	4	3	2	1	0
GAIN_TRIM_A							
R/W							

Table 73. GAIN_TRIM_A Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GAIN_TRIM_A	R/W	Undefined	This register enables gain trim of channel A. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.11 Channel B Gain Trim Register (address = 0x07B) [reset = Undefined]

Figure 114. Channel B Gain Trim Register (GAIN_TRIM_B)

7	6	5	4	3	2	1	0
GAIN_TRIM_B							
R/W							

Table 74. GAIN_TRIM_B Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GAIN_TRIM_B	R/W	Undefined	This register enables gain trim of channel B. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.12 Band-Gap Reference Trim Register (address = 0x07C) [reset = Undefined]

Figure 115. Band-Gap Reference Trim Register (BG_TRIM)

7	6	5	4	3	2	1	0
RESERVED				BG_TRIM			
R/W-0000				R/W			

Table 75. BG_TRIM Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3-0	BG_TRIM	R/W	Undefined	This register enables trim of the internal band-gap reference. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.13 VINA Input Resistor Trim Register (address = 0x07E) [reset = Undefined]

Figure 116. VINA Input Resistor Trim Register (RTRIM_A)

7	6	5	4	3	2	1	0
RTRIM							
R/W							

Table 76. RTRIM_A Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RTRIM_A	R/W	Undefined	This register controls VINA ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.14 VINB Input Resistor Trim Register (address = 0x07F) [reset = Undefined]

Figure 117. VINB Input Resistor Trim Register (RTRIM_B)

7	6	5	4	3	2	1	0
RTRIM							
R/W							

Table 77. RTRIM_B Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RTRIM_B	R/W	Undefined	This register controls VINB ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.15 Timing Adjust for A-ADC, Single Channel Mode, Foreground Calibration Register (address = 0x080) [reset = Undefined]

Figure 118. Register (TADJ_A_FG90)

7	6	5	4	3	2	1	0
TADJ_A_FG90							
R/W							

Table 78. TADJ_A_FG90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_A_FG90	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.16 Timing Adjust for B-ADC, Single Channel Mode, Foreground Calibration Register (address = 0x081) [reset = Undefined]

Figure 119. Register (TADJ_B_FG0)

7	6	5	4	3	2	1	0
TADJ_B_FG0							
R/W							

Table 79. TADJ_B_FG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_B_FG0	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.17 Timing Adjust for A-ADC, Single Channel Mode, Background Calibration Register (address = 0x082) [reset = Undefined]

Figure 120. Register (TADJ_A_BG90)

7	6	5	4	3	2	1	0
TADJ_A_BG90							
R/W							

Table 80. TADJ_B_FG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_A_BG90	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.18 Timing Adjust for C-ADC, Single Channel Mode, Background Calibration Register (address = 0x083) [reset = Undefined]

Figure 121. Register (TADJ_C_BG0)

7	6	5	4	3	2	1	0
TADJ_C_BG0							
R/W							

Table 81. TADJ_B_FG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_C_BG0	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.19 Timing Adjust for C-ADC, Single Channel Mode, Background Calibration Register (address = 0x084) [reset = Undefined]

Figure 122. Register (TADJ_C_BG90)

7	6	5	4	3	2	1	0
TADJ_C_BG90							
R/W							

Table 82. TADJ_B_FG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_C_BG90	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.20 Timing Adjust for B-ADC, Single Channel Mode, Background Calibration Register (address = 0x085) [reset = Undefined]

Figure 123. Register (TADJ_B_BG0)

7	6	5	4	3	2	1	0
TADJ_B_BG0							
R/W							

Table 83. TADJ_B_FG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_B_BG0	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.21 Timing Adjust for A-ADC, Dual Channel Mode Register (address = 0x086) [reset = Undefined]

Figure 124. Register (TADJ_A)

7	6	5	4	3	2	1	0
TADJ_A							
R/W							

Table 84. TADJ_A Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_A	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.22 Timing Adjust for C-ADC acting for A-ADC, Dual Channel Mode Register (address = 0x087) [reset = Undefined]

Figure 125. Register (TADJ_CA)

7	6	5	4	3	2	1	0
TADJ_CA							
R/W							

Table 85. TADJ_CA Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_CA	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.23 Timing Adjust for C-ADC acting for B-ADC, Dual Channel Mode Register (address = 0x088) [reset = Undefined]

Figure 126. Register (TADJ_CB)

7	6	5	4	3	2	1	0
TADJ_CB							
R/W							

Table 86. TADJ_CB Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_CB	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.24 Timing Adjust for B-ADC, Dual Channel Mode Register (address = 0x089) [reset = Undefined]

Figure 127. Register (TADJ_B)

7	6	5	4	3	2	1	0
TADJ_B							
R/W							

Table 87. TADJ_B Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_B	R/W	Undefined	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.5.25 Offset Adjustment for A-ADC and INA Register (address = 0x08A-0x08B) [reset = Undefined]

Figure 128. Register (OADJ_A_INA)

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_INA[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_A_INA[7:0]							
R/W							

Table 88. OADJ_A_INA Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_A_INA	R/W	Undefined	Offset adjustment value for ADC0 (A-ADC) applied when ADC0 samples INA. The format is unsigned. After reset, the factory trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS=1 and CAL_BGOS=0, only read OADJ* registers if FG_DONE=1 • If CAL_BG=1 and CAL_BGOS=1, only read OADJ* register if CAL_STOPPED=1

7.6.1.5.26 Offset Adjustment for A-ADC and INB Register (address = 0x08C-0x08D) [reset = Undefined]

Figure 129. Register (OADJ_A_INB)

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_INB[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_A_INB[7:0]							
R/W							

Table 89. OADJ_A_INB Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_A_INB	R/W	Undefined	Offset adjustment value for ADC0 (A-ADC) applied when ADC0 samples INB. The format is unsigned. After reset, the factory trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS=1 and CAL_BGOS=0, only read OADJ* registers if FG_DONE=1 • If CAL_BG=1 and CAL_BGOS=1, only read OADJ* register if CAL_STOPPED=1

7.6.1.5.27 Offset Adjustment for C-ADC and INA Register (address = 0x08E-0x08F) [reset = Undefined]

Figure 130. Register (OADJ_C_INA)

15	14	13	12	11	10	9	8
RESERVED				OADJ_C_INA[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_C_INA[7:0]							
R/W							

Table 90. OADJ_C_INA Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_C_INA	R/W	Undefined	Offset adjustment value for ADC1 (A-ADC) applied when ADC1 samples INA. The format is unsigned. After reset, the factory trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS=1 and CAL_BGOS=0, only read OADJ* registers if FG_DONE=1 • If CAL_BG=1 and CAL_BGOS=1, only read OADJ* register if CAL_STOPPED=1

7.6.1.5.28 Offset Adjustment for C-ADC and INB Register (address = 0x090-0x091) [reset = Undefined]

Figure 131. Register (OADJ_C_INB)

15	14	13	12	11	10	9	8
RESERVED				OADJ_C_INB[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_C_INB[7:0]							
R/W							

Table 91. OADJ_C_INB Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_C_INB	R/W	Undefined	Offset adjustment value for ADC1 (A-ADC) applied when ADC1 samples INB. The format is unsigned. After reset, the factory trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS=1 and CAL_BGOS=0, only read OADJ* registers if FG_DONE=1 • If CAL_BG=1 and CAL_BGOS=1, only read OADJ* register if CAL_STOPPED=1

7.6.1.5.29 Offset Adjustment for B-ADC and INA Register (address = 0x092-0x093) [reset = Undefined]

Figure 132. Register (OADJ_B_INA)

15	14	13	12	11	10	9	8
RESERVED				OADJ_B_INA[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_B_INA[7:0]							
R/W							

Table 92. OADJ_B_INA Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_B_INA	R/W	Undefined	Offset adjustment value for ADC2 (B-ADC) applied when ADC2 samples INA. The format is unsigned. After reset, the factory trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS=1 and CAL_BGOS=0, only read OADJ* registers if FG_DONE=1 • If CAL_BG=1 and CAL_BGOS=1, only read OADJ* register if CAL_STOPPED=1

7.6.1.5.30 Offset Adjustment for B-ADC and INB Register (address = 0x094-0x095) [reset = Undefined]

Figure 133. Register (OADJ_B_INB)

15	14	13	12	11	10	9	8
RESERVED				OADJ_B_INB[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_B_INB[7:0]							
R/W							

Table 93. OADJ_B_INB Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_B_INB	R/W	Undefined	Offset adjustment value for ADC2 (B-ADC) applied when ADC2 samples INB. The format is unsigned. After reset, the factory trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS=1 and CAL_BGOS=0, only read OADJ* registers if FG_DONE=1 • If CAL_BG=1 and CAL_BGOS=1, only read OADJ* register if CAL_STOPPED=1

7.6.1.5.31 Offset Filtering Control 0 Register (address = 0x097) [reset = 0x00]

Figure 134. Register (OSFILT0)

7	6	5	4	3	2	1	0
RESERVED							DC_RESTORE
R/W-0000 000							R/W

Table 94. OSFILT0 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	DC_RESTORE	R/W	0	When set the offset filtering feature (enabled by CAL_OSFILT) will filter only the offset mismatch across ADC banks and will not remove the frequency content near DC. When cleared, the feature filters all offsets from all banks, thus filtering all DC content in the signal. See Offset Filtering feature description.

7.6.1.5.32 Offset Filtering Control 1 Register (address = 0x098) [reset = 0x33]

Figure 135. Register (OSFILT1)

7	6	5	4	3	2	1	0
OSFILT_BW				OSFILT_SOAK			
R/W-0011				R/W-0011			

Table 95. OSFILT1 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OSFILT_BW	R/W	0011	This adjusts the IIR filter bandwidth for the offset filtering feature (enabled by CAL_OSFILT). More bandwidth will suppress more flicker noise from the ADCs and reduce the offset spurs. Less bandwidth will minimize the impact of the filters on the mission mode signal. OSFILT_BW: IIR Coefficient: -3dB Bandwidth (single sided) 0: RESERVED: RESERVED 1: 2^{-10} : 609e-9*F_{DEVCLK} 2: 2^{-11} : 305e-9*F_{DEVCLK} 3: 2^{-12} : 152e-9*F_{DEVCLK} 4: 2^{-13} : 76e-9*F_{DEVCLK} 5: 2^{-14} : 38e-9*F_{DEVCLK} 6-15: RESERVED
3-0	OSFILT_SOAK	R/W	0011	This adjusts the IIR soak time for the offset filtering feature. This applies when offset filtering and background calibration are both enabled. This field determines how long the IIR filter is allowed to settle when it is first connected to an ADC after the ADC is calibrated. After the soak time completes, the ADC is placed online using the IIR filter. It is recommended to set OSFILT_SOAK = OSFILT_BW.

7.6.1.6 ADC Bank Registers (0x100 to 0x15F)

Table 96. ADC Bank Registers

Address	Reset	Acronym	Register Name	Section
0x100-0x101	Undefined	RESERVED	RESERVED	
0x102	Undefined	B0_TIME_0	Timing Adjustment for Bank 0 (0° Clock) Register	Timing Adjustment for Bank 0 (0° Clock) Register (address = 0x102) [reset = Undefined]
0x103	Undefined	B0_TIME_90	Timing Adjustment for Bank 0 (-90° Clock) Register	Timing Adjustment for Bank 0 (-90° Clock) Register (address = 0x103) [reset = Undefined]
0x104-0x111	Undefined	RESERVED	RESERVED	
0x112	Undefined	B1_TIME_0	Timing Adjustment for Bank 1 (0° Clock) Register	Timing Adjustment for Bank 1 (0° Clock) Register (address = 0x112) [reset = Undefined]
0x113	Undefined	B1_TIME_90	Timing Adjustment for Bank 1 (-90° Clock) Register	Timing Adjustment for Bank 1 (-90° Clock) Register (address = 0x113) [reset = Undefined]
0x114-0x121	Undefined	RESERVED	RESERVED	
0x122	Undefined	B2_TIME_0	Timing Adjustment for Bank 2 (0° Clock) Register	Timing Adjustment for Bank 2 (0° Clock) Register (address = 0x122) [reset = Undefined]
0x123	Undefined	B2_TIME_90	Timing Adjustment for Bank 2 (-90° Clock) Register	Timing Adjustment for Bank 2 (-90° Clock) Register (address = 0x123) [reset = Undefined]
0x124-0x131	Undefined	RESERVED	RESERVED	
0x132	Undefined	B3_TIME_0	Timing Adjustment for Bank 3 (0° Clock) Register	Timing Adjustment for Bank 3 (0° Clock) Register (address = 0x132) [reset = Undefined]
0x133	Undefined	B3_TIME_90	Timing Adjustment for Bank 3 (-90° Clock) Register	Timing Adjustment for Bank 3 (-90° Clock) Register (address = 0x133) [reset = Undefined]
0x134-0x141	Undefined	RESERVED	RESERVED	

Table 96. ADC Bank Registers (continued)

Address	Reset	Acronym	Register Name	Section
0x142	Undefined	B4_TIME_0	Timing Adjustment for Bank 4 (0° Clock) Register	Timing Adjustment for Bank 4 (0° Clock) Register (address = 0x142) [reset = Undefined]
0x143	Undefined	B4_TIME_90	Timing Adjustment for Bank 4 (-90° Clock) Register	Timing Adjustment for Bank 4 (-90° Clock) Register (address = 0x143) [reset = Undefined]
0x144-0x151	Undefined	RESERVED	RESERVED	
0x152	Undefined	B5_TIME_0	Timing Adjustment for Bank 5 (0° Clock) Register	Timing Adjustment for Bank 5 (0° Clock) Register (address = 0x152) [reset = Undefined]
0x153	Undefined	B5_TIME_90	Timing Adjustment for Bank 5 (-90° Clock) Register	Timing Adjustment for Bank 5 (-90° Clock) Register (address = 0x153) [reset = Undefined]
0x154-0x15F	Undefined	RESERVED	RESERVED	

7.6.1.6.1 Timing Adjustment for Bank 0 (0° Clock) Register (address = 0x102) [reset = Undefined]

Figure 136. Timing Adjustment for Bank 0 (0° Clock) Register (B0_TIME_0)

7	6	5	4	3	2	1	0
B0_TIME_0							
R/W							

Table 97. B0_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B0_TIME_0	R/W	Undefined	Time adjustment for bank 0 (applied when ADC is configured for 0° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.2 Timing Adjustment for Bank 0 (-90° Clock) Register (address = 0x103) [reset = Undefined]

Figure 137. Timing Adjustment for Bank 0 (-90° Clock) Register (B0_TIME_90)

7	6	5	4	3	2	1	0
B0_TIME_90							
R/W							

Table 98. B0_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B0_TIME_90	R/W	Undefined	Time adjustment for bank 0 (applied when ADC is configured for -90° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.3 Timing Adjustment for Bank 1 (0° Clock) Register (address = 0x112) [reset = Undefined]

Figure 138. Timing Adjustment for Bank 1 (0° Clock) Register (B1_TIME_0)

7	6	5	4	3	2	1	0
B1_TIME_0							
R/W							

Table 99. B1_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B1_TIME_0	R/W	Undefined	Time adjustment for bank 1 (applied when ADC is configured for 0° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.4 Timing Adjustment for Bank 1 (-90° Clock) Register (address = 0x113) [reset = Undefined]

Figure 139. Timing Adjustment for Bank 1 (-90° Clock) Register (B1_TIME_90)

7	6	5	4	3	2	1	0
B1_TIME_90							
R/W							

Table 100. B1_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B1_TIME_90	R/W	Undefined	Time adjustment for bank 1 (applied when ADC is configured for -90° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.5 Timing Adjustment for Bank 2 (0° Clock) Register (address = 0x122) [reset = Undefined]

Figure 140. Timing Adjustment for Bank 2 (0° Clock) Register (B2_TIME_0)

7	6	5	4	3	2	1	0
B2_TIME_0							
R/W							

Table 101. B2_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B2_TIME_0	R/W	Undefined	Time adjustment for bank 2 (applied when ADC is configured for 0° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.6 Timing Adjustment for Bank 2 (-90° Clock) Register (address = 0x123) [reset = Undefined]

Figure 141. Timing Adjustment for Bank 2 (-90° Clock) Register (B2_TIME_90)

7	6	5	4	3	2	1	0
B2_TIME_90							
R/W							

Table 102. B2_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B2_TIME_90	R/W	Undefined	Time adjustment for bank 2 (applied when ADC is configured for -90° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.7 Timing Adjustment for Bank 3 (0° Clock) Register (address = 0x132) [reset = Undefined]

Figure 142. Timing Adjustment for Bank 3 (0° Clock) Register (B3_TIME_0)

7	6	5	4	3	2	1	0
B3_TIME_0							
R/W							

Table 103. B3_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B3_TIME_0	R/W	Undefined	Time adjustment for bank 3 (applied when ADC is configured for 0° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.8 Timing Adjustment for Bank 3 (-90° Clock) Register (address = 0x133) [reset = Undefined]

Figure 143. Timing Adjustment for Bank 3 (-90° Clock) Register (B3_TIME_90)

7	6	5	4	3	2	1	0
B3_TIME_90							
R/W							

Table 104. B3_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B3_TIME_90	R/W	Undefined	Time adjustment for bank 3 (applied when ADC is configured for -90° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.9 Timing Adjustment for Bank 4 (0° Clock) Register (address = 0x142) [reset = Undefined]

Figure 144. Timing Adjustment for Bank 4 (0° Clock) Register (B4_TIME_0)

7	6	5	4	3	2	1	0
B4_TIME_0							
R/W							

Table 105. B4_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B4_TIME_0	R/W	Undefined	Time adjustment for bank 4 (applied when ADC is configured for 0° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.10 Timing Adjustment for Bank 4 (-90° Clock) Register (address = 0x143) [reset = Undefined]

Figure 145. Timing Adjustment for Bank 4 (-90° Clock) Register (B4_TIME_90)

7	6	5	4	3	2	1	0
B4_TIME_90							
R/W							

Table 106. B4_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B4_TIME_90	R/W	Undefined	Time adjustment for bank 4 (applied when ADC is configured for -90° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.11 Timing Adjustment for Bank 5 (0° Clock) Register (address = 0x152) [reset = Undefined]

Figure 146. Timing Adjustment for Bank 5 (0° Clock) Register (B5_TIME_0)

7	6	5	4	3	2	1	0
B5_TIME_0							
R/W							

Table 107. B5_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B5_TIME_0	R/W	Undefined	Time adjustment for bank 5 (applied when ADC is configured for 0° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.6.12 Timing Adjustment for Bank 5 (-90° Clock) Register (address = 0x153) [reset = Undefined]

Figure 147. Timing Adjustment for Bank 5 (-90° Clock) Register (B5_TIME_90)

7	6	5	4	3	2	1	0
B5_TIME_90							
R/W							

Table 108. B5_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B5_TIME_90	R/W	Undefined	Time adjustment for bank 5 (applied when ADC is configured for -90° clock phase). After reset, the factory trimmed value can be read and adjusted as required.

7.6.1.7 LSB Control Registers (0x160 to 0x1FF)

Table 109. LSB Control Registers

Address	Reset	Acronym	Register Name	Section
0x160	0x00	ENC_LSB	LSB Control Bit Output Register	Figure 148
0x161-0x1FF	Undefined	RESERVED	RESERVED	

7.6.1.7.1 LSB Control Bit Output Register (address = 0x160) [reset = 0x00]

Figure 148. LSB Control Bit Output Register (ENC_LSB)

7	6	5	4	3	2	1	0
RESERVED							TIMESTAMP_EN
R/W-0000 000							R/W-0

Table 110. ENC_LSB Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	TIMESTAMP_EN	R/W	0	When set, the transport layer transmits the timestamp signal on the LSB of the output samples. Only supported in decimate-by-1 (DDC bypass) modes. TIMESTAMP_EN has priority over CAL_STATE_EN. TMSTP_RECV_EN must also be set high when using timestamp. The latency of the timestamp signal (through the entire chip) matches the latency of the analog ADC inputs. Note 1: In 8-bit modes, the control bit is placed on the LSB of the 8-bit samples (leaving 7-bits of sample data). If the part is configured for 12-bit data, the control bit is placed on the LSB of the 12-bit bit data (leaving 11-bits of sample data). Note 2: The control bit that is enabled by this register is never advertised in the ILA (the CS field is 0 in the ILA).

7.6.1.8 JESD204B Registers (0x200 to 0x20F)

Table 111. JESD204B Registers

Address	Reset	Acronym	Register Name	Section
0x200	0x01	JESD_EN	JESD204B Enable Register	JESD204B Enable Register (address = 0x200) [reset = 0x01]
0x201	0x02	JMODE	JESD204B Mode Register	JESD204B Mode Register (address = 0x201) [reset = 0x02]
0x202	0x1F	KM1	JESD204B K Parameter Register	JESD204B K Parameter Register (address = 0x202) [reset = 0x1F]
0x203	0x01	JSYNC_N	JESD204B Manual SYNC Request Register	JESD204B Manual SYNC Request Register (address = 0x203) [reset = 0x01]
0x204	0x02	JCTRL	JESD204B Control Register	JESD204B Control Register (address = 0x204) [reset = 0x02]
0x205	0x00	JTEST	JESD204B Test Pattern Control Register	JESD204B Test Pattern Control Register (address = 0x205) [reset = 0x00]
0x206	0x00	DID	JESD204B DID Parameter Register	JESD204B DID Parameter Register (address = 0x206) [reset = 0x00]
0x207	0x00	FCHAR	JESD204B Frame Character Register	JESD204B Frame Character Register (address = 0x207) [reset = 0x00]
0x208	Undefined	JESD_STATUS	JESD204B / System Status Register	JESD204B / System Status Register (address = 0x208) [reset = Undefined]
0x209	0x00	PD_CH	JESD204B Channel Power Down	JESD204B Channel Power Down Register (address = 0x209) [reset = 0x00]

Table 111. JESD204B Registers (continued)

Address	Reset	Acronym	Register Name	Section
0x20A	0x00	JEXTRA_A	JESD204B Extra Lane Enable (Link A)	JESD204B Extra Lane Enable (Link A) Register (address = 0x20A) [reset = 0x00]
0x20B	0x00	JEXTRA_B	JESD204B Extra Lane Enable (Link B)	JESD204B Extra Lane Enable (Link B) Register (address = 0x20B) [reset = 0x00]
0x20C-0x20F	Undefined	RESERVED	RESERVED	

7.6.1.8.1 JESD204B Enable Register (address = 0x200) [reset = 0x01]

Figure 149. JESD204B Enable Register (JESD_EN)

7	6	5	4	3	2	1	0
RESERVED							JESD_EN
R/W-0000 000							R/W-1

Table 112. JESD_EN Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	JESD_EN	R/W	1	0 : Disable JESD204B interface 1 : Enable JESD204B interface Note 1: Before altering other JESD204B registers, you must clear JESD_EN. When JESD_EN is 0, the block is held in reset and the serializers are powered down. The clocks are gated off to save power. The LMFC counter is also held in reset, so SYSREF will not align the LMFC. Note 2: Always set CAL_EN before setting JESD_EN Note 3: Always clear JESD_EN before clearing CAL_EN

7.6.1.8.2 JESD204B Mode Register (address = 0x201) [reset = 0x02]

Figure 150. JESD204B Mode Register (JMODE)

7	6	5	4	3	2	1	0
RESERVED			JMODE				
R/W-000			R/W-0001 0				

Table 113. JMODE Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	RESERVED
4-0	JMODE	R/W	0001 0	Specify the JESD204B output mode (including DDC decimation factor) Note: This register should only be changed when JESD_EN=0 and CAL_EN=0

7.6.1.8.3 JESD204B K Parameter Register (address = 0x202) [reset = 0x1F]

Figure 151. JESD204B K Parameter Register (KM1)

7	6	5	4	3	2	1	0
RESERVED			KM1				
R/W-000			R/W-1111 1				

Table 114. KM1 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	RESERVED
4-0	KM1	R/W	1111 1	K is the number of frames per multiframe and this register must be programmed as K-1. Depending on the JMODE setting, there are constraints on the legal values of K. (default: KM1=31, K=32) Note: This register should only be changed when JESD_EN is 0.

7.6.1.8.4 JESD204B Manual SYNC Request Register (address = 0x203) [reset = 0x01]

Figure 152. JESD204B Manual SYNC Request Register (JSYNC_N)

7	6	5	4	3	2	1	0
RESERVED							JSYNC_N
R/W-0000 000							R/W-1

Table 115. JSYNC_N Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	JSYNC_N	R/W	1	Set this bit to 0 to request JESD204B synchronization (equivalent to the SYNCSE pin being asserted). For normal operation, leave this bit set to 1. Note: The JSYNC_N register can always generate a synchronization request, regardless of the SYNC_SEL register. However, if the selected sync pin is stuck low, you cannot de-assert the synchronization request unless you program SYNC_SEL=2.

7.6.1.8.5 JESD204B Control Register (address = 0x204) [reset = 0x02]

Figure 153. JESD204B Control Register (JCTRL)

7	6	5	4	3	2	1	0
RESERVED				SYNC_SEL		SFORMAT	SCR
R/W-0000				R/W-00		R/W-1	R/W-0

Table 116. JCTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3-2	SYNC_SEL	R/W	00	0: Use the SYNCSE input for SYNC~ function (default) 1: Use the TMSTP+/- differential input for SYNC~ function. TMSTP_RECV_EN must also be set. 2: Do not use any sync input signal (use software SYNC~ through JSYNC_N)
1	SFORMAT	R/W	1	Output sample format for JESD204B samples 0: Offset binary 1: Signed 2's complement (default)
0	SCR	R/W	0	0: Scrambler disabled (default) 1: Scrambler enabled Note: This register should only be changed when JESD_EN is 0.

7.6.1.8.6 JESD204B Test Pattern Control Register (address = 0x205) [reset = 0x00]

Figure 154. JESD204B Test Pattern Control Register (JTEST)

7	6	5	4	3	2	1	0
RESERVED				JTEST			
R/W-0000				R/W-0000			

Table 117. JTEST Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3-0	JTEST	R/W	0000	0: Test mode disabled. Normal operation (default) 1: PRBS7 test mode 2: PRBS15 test mode 3: PRBS23 test mode 4: Ramp test mode 5: Transport Layer test mode 6: D21.5 test mode 7: K28.5 test mode 8: Repeated ILA test mode 9: Modified RPAT test mode 10: Serial outputs held low 11: Serial outputs held high 12 thru 15: RESERVED Note: This register should only be changed when JESD_EN is 0.

7.6.1.8.7 JESD204B DID Parameter Register (address = 0x206) [reset = 0x00]

Figure 155. JESD204B DID Parameter Register (DID)

7	6	5	4	3	2	1	0
DID							
R/W-0000 0000							

Table 118. DID Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DID	R/W	0000 0000	Specifies the DID (Device ID) value that is transmitted during the second multiframe of the JESD204B ILA. Link A will transmit DID, and link B will transmit DID+1. Bit 0 is ignored and always returns 0 (if you program an odd number, it will be decremented to an even number). Note: This register should only be changed when JESD_EN is 0.

7.6.1.8.8 JESD204B Frame Character Register (address = 0x207) [reset = 0x00]

Figure 156. JESD204B Frame Character Register (FCHAR)

7	6	5	4	3	2	1	0
RESERVED						FCHAR	
R/W-0000 00						R/W-00	

Table 119. FCHAR Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1-0	FCHAR	R/W	00	Specify which comma character is used to denote end-of-frame. This character is transmitted opportunistically (see section 12.8.5) 0: Use K28.7 (default) (JESD204B compliant) 1: Use K28.1 (not JESD204B compliant) 2: Use K28.5 (not JESD204B compliant) 3: RESERVED When using a JESD204B receiver, always use FCHAR=0. When using a general purpose 8b/10b receiver, the K28.7 character may cause issues. When K28.7 is combined with certain data characters, a false, misaligned comma character can result, and some receivers will re-align to the false comma. To avoid this, program FCHAR to 1 or 2. Note: This register should only be changed when JESD_EN is 0.

7.6.1.8.9 JESD204B / System Status Register (address = 0x208) [reset = Undefined]

Figure 157. JESD204B / System Status Register (JESD_STATUS)

7	6	5	4	3	2	1	0
RESERVED	LINK_UP	SYNC_STATUS	REALIGNED	ALIGNED	PLL_LOCKED	RESERVED	
R	R	R	R/W	R/W	R	R	

Table 120. JESD_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	Undefined	RESERVED
6	LINK_UP	R	Undefined	When set, indicates that the JESD204B link is up
5	SYNC_STATUS	R	Undefined	Returns the state of the JESD204B SYNC~ signal. 0: SYNC~ asserted 1: SYNC~ de-asserted
4	REALIGNED	R/W	Undefined	When high, indicates that an internal digital clock, frame clock, or multiframe (LMFC) clock phase was realigned by SYSREF. Writing a 1 to this bit will clear it.
3	ALIGNED	R/W	Undefined	When high, indicates that the multiframe (LMFC) clock phase has been established by SYSREF. The first SYSREF event after enabling the JESD204B encoder will set this bit. Writing a 1 to this bit will clear it.
2	PLL_LOCKED	R	Undefined	When high, indicates that the PLL is locked
1-0	RESERVED	R	Undefined	RESERVED

7.6.1.8.10 JESD204B Channel Power Down Register (address = 0x209) [reset = 0x00]

Figure 158. JESD204B Channel Power Down Register (PD_CH)

7	6	5	4	3	2	1	0
RESERVED						PD_BCH	PD_ACH
R/W-0000 00						R/W-0	R/W-0

Table 121. PD_CH Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1	PD_BCH	R/W	0	When set, the “B” ADC channel is powered down. The digital channels that are bound to the “B” ADC channel are also powered down (see DIG_BIND). Important notes: 1. You must set JESD_EN=0 before changing PD_CH 2. To power down both ADC channels, use MODE 3. If both channels are powered down, then the entire JESD204B subsystem (including the PLL and LMFC) are powered down 4. If the selected JESD204B mode transmits A and B data on link A, and the B digital channel is disabled, link A remains operational, but the B-channel samples are undefined.
0	PD_ACH	R/W	0	When set, the “A” ADC channel is powered down. The digital channels that are bound to the “A” ADC channel are also powered down (see DIG_BIND). Important notes: 1. You must set JESD_EN=0 before changing PD_CH 2. To power down both ADC channels, use MODE 3. If both channels are powered down, then the entire JESD204B subsystem (including the PLL and LMFC) are powered down 4. If the selected JESD204B mode transmits A and B data on link A, and the B digital channel is disabled, link A remains operational, but the B-channel samples are undefined.

7.6.1.8.11 JESD204B Extra Lane Enable (Link A) Register (address = 0x20A) [reset = 0x00]

Figure 159. JESD204B Extra Lane Enable (Link A) Register (JEXTRA_A)

7	6	5	4	3	2	1	0
EXTRA_LANE_A							EXTRA_SER_A
R/W-0000 000							R/W-0

Table 122. JESD204B Extra Lane Enable (Link A) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	EXTRA_LANE_A	R/W	0000 000	Program these register bits to enable extra lanes (even if the selected JMODE does not require the lanes to be enabled). EXTRA_LANE_A(n) enables An (n=1 to 7). This register enables the link layer clocks for the affected lanes. To also enable the extra serializes set EXTRA_SER_A=1.
0	EXTRA_SER_A	R/W	0	0: Only the link layer clocks for extra lanes are enabled. 1: Serializers for extra lanes are also enabled. Use this mode to transmit data from the extra lanes. Important notes: This register should only be changed when JESD_EN=0. The bit-rate and mode of the extra lanes are set by the JMODE and JTEST parameters. This register does not override the PD_CH register, so ensure that the link is enabled to use this feature. To enable serializer 'n', the lower number lanes 0 to n-1 must also be enabled, otherwise serializer 'n' will not receive a clock.

7.6.1.8.12 JESD204B Extra Lane Enable (Link B) Register (address = 0x20B) [reset = 0x00]

Figure 160. JESD204B Extra Lane Enable (Link B) Register (JEXTRA_B)

7	6	5	4	3	2	1	0
EXTRA_LANE_B							EXTRA_SER_B
R/W-0000 000							R/W-0

Table 123. JESD204B Extra Lane Enable (Link B) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	EXTRA_LANE_B	R/W	0000 000	Program these register bits to enable extra lanes (even if the selected JMODE does not require the lanes to be enabled). EXTRA_LANE_B(n) enables Bn (n=1 to 7). This register enables the link layer clocks for the affected lanes. To also enable the extra serializes set EXTRA_SER_B=1.
0	EXTRA_SER_B	R/W	0	0: Only the link layer clocks for extra lanes are enabled. 1: Serializers for extra lanes are also enabled. Use this mode to transmit data from the extra lanes. Important notes: This register should only be changed when JESD_EN=0. The bit-rate and mode of the extra lanes are set by the JMODE and JTEST parameters. This register does not override the PD_CH register, so ensure that the link is enabled to use this feature. To enable serializer 'n', the lower number lanes 0 to n-1 must also be enabled, otherwise serializer 'n' will not receive a clock.

7.6.1.9 Digital Down Converter Registers (0x210-0x2AF)

Table 124. Digital Down Converter and Over-range Registers

Address	Reset	Acronym	Register Name	Section
0x210	0x00	DDC_CFG	DDC Configuration Register	DDC Configuration Register (address = 0x210) [reset = 0x00]
0x211	0xF2	OVR_T0	Over-range Threshold 0 Register	Over-range Threshold 0 Register (address = 0x211) [reset = 0xF2]
0x212	0xAB	OVR_T1	Over-range Threshold 1 Register	Over-range Threshold 1 Register (address = 0x212) [reset = 0xAB]
0x213	0x07	OVR_CFG	Over-range Configuration Register	Over-range Configuration Register (address = 0x213) [reset = 0x07]
0x214	0x00	CMODE	DDC Configuration Preset Mode Register	DDC Configuration Preset Mode Register (address = 0x214) [reset = 0x00]
0x215	0x00	CSEL	DDC Configuration Preset Select Register	DDC Configuration Preset Select Register (address = 0x215) [reset = 0x00]
0x216	0x02	DIG_BIND	Digital Channel Binding Register	Digital Channel Binding Register (address = 0x216) [reset = 0x02]
0x217-0x218	0x0000	NCO_RDIV	Rational NCO Reference Divisor Register	Rational NCO Reference Divisor Register (address = 0x217 to 0x218) [reset = 0x0000]
0x219	0x02	NCO_SYNC	NCO Synchronization Register	NCO Synchronization Register (address = 0x219) [reset = 0x02]
0x21A-0x21F	Undefined	RESERVED	RESERVED	
0x220-0x223	0xC0000000	FREQA0	NCO Frequency (DDC A Preset 0)	NCO Frequency (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x224-0x225	0x0000	PHASEA0	NCO Phase (DDC A Preset 0)	NCO Phase (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x226-0x227	Undefined	RESERVED	RESERVED	
0x228-0x22B	0xC0000000	FREQA1	NCO Frequency (DDC A Preset 1)	NCO Frequency (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x22C-0x22D	0x0000	PHASEA1	NCO Phase (DDC A Preset 1)	NCO Phase (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x22E-0x22F	Undefined	RESERVED	RESERVED	
0x230-0x233	0xC0000000	FREQA2	NCO Frequency (DDC A Preset 2)	NCO Frequency (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x234-0x235	0x0000	PHASEA2	NCO Phase (DDC A Preset 2)	NCO Phase (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x236-0x237	Undefined	RESERVED	RESERVED	
0x238-0x23B	0xC0000000	FREQA3	NCO Frequency (DDC A Preset 3)	NCO Frequency (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x23C-0x23D	0x0000	PHASEA3	NCO Phase (DDC A Preset 3)	NCO Phase (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x23E-0x23F	Undefined	RESERVED	RESERVED	
0x240-0x243	0xC0000000	FREQB0	NCO Frequency (DDC B Preset 0)	NCO Frequency (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x244-0x245	0x0000	PHASEB0	NCO Phase (DDC B Preset 0)	NCO Phase (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x246-0x247	Undefined	RESERVED	RESERVED	
0x248-0x24B	0xC0000000	FREQB1	NCO Frequency (DDC B Preset 1)	NCO Frequency (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]

Table 124. Digital Down Converter and Over-range Registers (continued)

Address	Reset	Acronym	Register Name	Section
0x24C-0x24D	0x0000	PHASEB1	NCO Phase (DDC B Preset 1)	NCO Phase (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x24E-0x24F	Undefined	RESERVED	RESERVED	
0x250-0x253	0xC0000000	FREQB2	NCO Frequency (DDC B Preset 2)	NCO Frequency (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x254-0x255	0x0000	PHASEB2	NCO Phase (DDC B Preset 2)	NCO Phase (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x256-0x257	Undefined	RESERVED	RESERVED	
0x258-0x25B	0xC0000000	FREQB3	NCO Frequency (DDC B Preset 3)	NCO Frequency (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x25C-0x25D	0x0000	PHASEB3	NCO Phase (DDC B Preset 3)	NCO Phase (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]
0x25E-0x296	Undefined	RESERVED	RESERVED	
0x297	Undefined	SPIN_ID	Spin Identification Value	Spin Identification Register (address = 0x297) [reset = Undefined]
0x298-0x2AF	Undefined	RESERVED	RESERVED	

7.6.1.9.1 DDC Configuration Register (address = 0x210) [reset = 0x00]

Figure 161. DDC Configuration Register (DDC_CFG)

7	6	5	4	3	2	1	0
RESERVED				D4_AP87	D2_HIGH_PASS	INVERT_SPECTRUM	BOOST
R/W-0000				R/W-0	R/W-0	R/W-0	R/W-0

Table 125. DDC_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3	D4_AP87	R/W	0	0: Decimate-by-4 mode uses 80% alias protection, >80dB suppression 1: Decimate-by-4 mode uses 87.5% alias protection, >60dB suppression
2	D2_HIGH_PASS	R/W	0	0: Decimate-by-2 mode uses a low-pass filter 1: Decimate-by-2 mode uses a high-pass filter. Decimating the high-pass signal will cause spectral inversion. This can be undone by setting INVERT_SPECTRUM.
1	INVERT_SPECTRUM	R/W	0	0: No inversion applied to output spectrum 1: Output spectrum is inverted This register only applies when the DDC is enabled and is producing a real output (not complex). The spectrum is inverted by mixing the signal with FSOUT/2 (i.e. invert all odd samples).
0	BOOST	R/W	0	DDC gain control. Only applies to DDC modes with complex decimation. 0: Final filter has 0dB gain (default) 1: Final filter has 6.02dB gain. Only use this when you are certain the negative image of your input signal is filtered out by the DDC, otherwise digital clipping may occur.

7.6.1.9.2 Over-range Threshold 0 Register (address = 0x211) [reset = 0xF2]

Figure 162. Over-range Threshold 0 Register (OVR_T0)

7	6	5	4	3	2	1	0
OVR_T0							
R/W-1111 0010							

Table 126. OVR_T0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OVR_T0	R/W	1111 0010	Over-range threshold 0. This parameter defines the absolute sample level that causes control bit 0 to be set. The detection level in dBFS (peak) is 20_{log10}(OVR_T0 / 256) Default: 0xF2 = 242 → –0.5 dBFS

7.6.1.9.3 Over-range Threshold 1 Register (address = 0x212) [reset = 0xAB]

Figure 163. Over-range Threshold 1 Register (OVR_T1)

7	6	5	4	3	2	1	0
OVR_T1							
R/W-1010 1011							

Table 127. OVR_T1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OVR_T1	R/W	1010 1011	Over-range threshold 1. This parameter defines the absolute sample level that causes control bit 1 to be set. The detection level in dBFS (peak) is 20_{log10}(OVR_T1 / 256) Default: 0xAB = 171 → –3.5 dBFS

7.6.1.9.4 Over-range Configuration Register (address = 0x213) [reset = 0x07]

Figure 164. Over-range Configuration Register (OVR_CFG)

7	6	5	4	3	2	1	0
RESERVED				OVR_EN	OVR_N		
R/W-0000				R/W-0	R/W-111		

Table 128. OVR_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000 0	RESERVED
3	OVR_EN	R/W	0	Enables over-range status output pins when set high. The ORA0, ORA1, ORB0 and ORB1 outputs are held low when OVR_EN is set low. This register only effects the over-range output pins (ORxx) and not the over-range status embedded in the data samples.
2-0	OVR_N (1)	R/W	111	Program this register to adjust the pulse extension for the ORA0/1 and ORB0/1 outputs. The minimum pulse duration of the over-range outputs is 8 * 2^{OVR_N} DEVCLK cycles. Incrementing this field doubles the monitoring period.

(1) Changing the OVR_N setting while JESD_EN=1 may cause the phase of the monitoring period to change.

7.6.1.9.5 DDC Configuration Preset Mode Register (address = 0x214) [reset = 0x00]

Figure 165. DDC Configuration Preset Mode Register (CMODE)

7	6	5	4	3	2	1	0
RESERVED						CMODE	
R/W-0000 00						R/W-00	

Table 129. CMODE Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1-0	CMODE	R/W	00	The NCO frequency and phase for DDC A are set by the FREQAx and PHASEAx registers and the NCO frequency and phase for DDC B are set by the FREQBx and PHASEBx registers, where *x* is the configuration preset (0 through 3). 0: Use CSEL register to select the active NCO configuration preset for DDC A and DDC B 1: Use NCOA[1:0] pins to select the active NCO configuration preset for DDC A and use NCOB[1:0] pins to select the active NCO configuration preset for DDC B 2: Use NCOA[1:0] pins to select the active NCO configuration preset for both DDC A and DDC B 3: RESERVED

7.6.1.9.6 DDC Configuration Preset Select Register (address = 0x215) [reset = 0x00]

Figure 166. DDC Configuration Preset Select Register (CSEL)

7	6	5	4	3	2	1	0
RESERVED				CSELB		CSELA	
R/W-0000				R/W-00		R/W-00	

Table 130. CSEL Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3-2	CSELB	R/W	00	When CMODE=0, this register is used to select the active NCO configuration preset for DDC B
1-0	CSELA	R/W	00	When CMODE=0, this register is used to select the active NCO configuration preset for DDC A Example: If CSELA=0, then FREQA0 and PHASEA0 are the active settings. If CSELA=1, then FREQA1 and PHASEA1 are the active settings.

7.6.1.9.7 Digital Channel Binding Register (address = 0x216) [reset = 0x02]

Figure 167. Digital Channel Binding Register (DIG_BIND)

7	6	5	4	3	2	1	0
RESERVED						DIG_BIND_B	DIG_BIND_A
R/W-0000 00						R/W-1	R/W-0

Table 131. DIG_BIND Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1	DIG_BIND_B	R/W	0	Digital channel B input select: 0: Digital channel B receives data from ADC channel A 1: Digital channel B receives data from ADC channel B (default)
0	DIG_BIND_A	R/W	0	Digital channel A input select: 0: Digital channel A receives data from ADC channel A (default) 1: Digital channel A receives data from ADC channel B Note 1: When using single channel mode, you must always use the default setting for DIG_BIND or the part will not work. Note 2: You must set JESD_EN=0 and CAL_EN=0 before changing DIG_BIND. Note 3: The DIG_BIND setting is combined with PD_ACH/PD_BCH to determine if a digital channel is powered down. Each digital channel (and link) is powered down when the ADC channel it is bound to is powered down (by PD_ACH/PD_BCH).

7.6.1.9.8 Rational NCO Reference Divisor Register (address = 0x217 to 0x218) [reset = 0x0000]

Figure 168. Rational NCO Reference Divisor Register (NCO_RDIV)

15	14	13	12	11	10	9	8
NCO_RDIV[15:8]							
R/W-0000 0000							
7	6	5	4	3	2	1	0
NCO_RDIV[7:0]							
R/W-0000 0000							

Table 132. NCO_RDIV Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NCO_RDIV	R/W	0x0000h	Sometimes the 32-bit NCO frequency word does not provide the desired frequency step size and can only approximate the desired frequency. This results in a frequency error. Use this register to eliminate the frequency error. This register is used for all configuration presets. See .

7.6.1.9.9 NCO Synchronization Register (address = 0x219) [reset = 0x02]

Figure 169. NCO Synchronization Register (NCO_SYNC)

7	6	5	4	3	2	1	0
RESERVED						NCO_SYNC_ILA	NCO_SYNC_NEXT
R/W-0000 00						R/W-1	R/W-0

Table 133. NCO_SYNC Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1	NCO_SYNC_ILA	R/W	0	When this bit is set, the NCO phase is initialized by the LMFC edge that starts the ILA sequence (default)
0	NCO_SYNC_NEXT	R/W	0	After writing ‘0’ and then ‘1’ to this bit, the next SYSREF rising edge will initialize the NCO phase. Once the NCO phase has been initialized by SYSREF, the NCO will not re-initialize on future SYSREF edges unless ‘0’ and ‘1’ is written to this bit again. Use this to align the NCO in multiple parts: • Ensure the part is powered up, JESD_EN is set, and the device clock is running. • Ensure that SYSREF is disabled (not toggling). • Program NCO_SYNC_ILA=0 on all parts. • Write NCO_SYNC_NEXT=0 on all parts. • Write NCO_SYNC_NEXT=1 on all parts. NCO sync is armed. • Instruct the SYSREF source to generate 1 or more SYSREF pulses. • All parts will initialize their NCO using the first SYSREF rising edge.

7.6.1.9.10 NCO Frequency (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]

Figure 170. NCO Frequency (DDC A or DDC B and Preset x) Register (FREQAx or FREQBx)

31	30	29	28	27	26	25	24
FREQAx[31:24] or FREQBx[31:24]							
R/W-0xC0							
23	22	21	20	19	18	17	16
FREQAx[23:16] or FREQBx[23:16]							
R/W-0x00							
15	14	13	12	11	10	9	8
FREQAx[15:8] or FREQBx[15:8]							
R/W-0x00							
7	6	5	4	3	2	1	0
FREQAx[7:0] or FREQBx[7:0]							
R/W-0x00							

Table 134. FREQAx or FREQBx Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FREQAx or FREQBx	R/W	See Table 124	Changing this register after the JESD204B interface is running results in non-deterministic NCO phase. If deterministic phase is required, the JESD204B interface must be re-initialized after changing this register. This register can be interpreted as signed or unsigned. See .

7.6.1.9.11 NCO Phase (DDC A or DDC B and Preset x) Register (address = see Table 124) [reset = see Table 124]

Figure 171. NCO Phase (DDC A or DDC B and Preset x) Register (PHASEAx or PHASEBx)

15	14	13	12	11	10	9	8
PHASEAx[15:8] or PHASEBx[15:8]							
R/W-0x00							
7	6	5	4	3	2	1	0
PHASEAx[7:0] or PHASEBx[7:0]							
R/W-0x00							

Table 135. PHASEAx or PHASEBx Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHASEAx or PHASEBx	R/W	See Table 124	This value is MSB-justified into a 32−bit field and then added to the phase accumulator. This register can be interpreted as signed or unsigned. See NCO Phase Offset Setting.

7.6.1.10 Spin Identification Register (address = 0x297) [reset = Undefined]

Figure 172. Spin Identification Register (SPIN_ID)

7	6	5	4	3	2	1	0
RESERVED			SPIN_ID				
R-000			R				

Table 136. SPIN_ID Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	000	RESERVED
4-0	SPIN_ID	R	See description	Spin identification value: 0 : ADC12DJ3200

7.6.2 SYSREF Calibration Registers (0x2B0 to 0x2BF)

Table 137. SYSREF Calibration Registers

Address	Reset	Acronym	Register Name	Section
0x2B0	0x00	SRC_EN	SYSREF Calibration Enable Register	SYSREF Calibration Enable Register (address = 0x2B0) [reset = 0x00]
0x2B1	0x05	SRC_CFG	SYSREF Calibration Configuration Register	SYSREF Calibration Configuration Register (address = 0x2B1) [reset = 0x05]
0x2B2-0x2B4	Undefined	SRC_STATUS	SYSREF Calibration Status	SYSREF Calibration Status Register (address = 0x2B2 to 0x2B4) [reset = Undefined]
0x2B5-0x2B7	0x00	TAD	DEVCLK Aperture Delay Adjustment Register	DEVCLK Aperture Delay Adjustment Register (address = 0x2B5 to 0x2B7) [reset = 0x000000]
0x2B8	0x00	TAD_RAMP	DEVCLK Timing Adjust Ramp Control Register	DEVCLK Timing Adjust Ramp Control Register (address = 0x2B8) [reset = 0x00]
0x2B9-0x2BF	Undefined	RESERVED	RESERVED	

7.6.2.1 SYSREF Calibration Enable Register (address = 0x2B0) [reset = 0x00]

Figure 173. SYSREF Calibration Enable Register (SRC_EN)

7	6	5	4	3	2	1	0
RESERVED							SRC_EN
R/W-0000 000							R/W-0

Table 138. SRC_EN Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	SRC_EN	R/W	0	0: SYSREF Calibration Disabled. Use the TAD register to manually control the tad[16:0] output and adjust the DEVCLK delay. (default) 1: SYSREF Calibration Enabled. The DEVCLK delay is automatically calibrated. The TAD register is ignored. A 0-to-1 transition on SRC_EN starts the SYSREF calibration sequence. Program SRC_CFG before setting SRC_EN. Ensure that ADC calibration is not currently running before setting SRC_EN.

7.6.2.2 SYSREF Calibration Configuration Register (address = 0x2B1) [reset = 0x05]

Figure 174. SYSREF Calibration Configuration Register (SRC_CFG)

7	6	5	4	3	2	1	0
RESERVED				SRC_AVG		SRC_HDUR	
R/W-0000				R/W-01		R/W-01	

Table 139. SRC_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000 00	RESERVED
3-2	SRC_AVG	R/W	01	Specifies the amount of averaging used for SYSREF Calibration. Larger values will increase calibration time and reduce the variance of the calibrated value. 0: 4 averages 1: 16 averages 2: 64 averages 3: 256 averages
1-0	SRC_HDUR	R/W	01	Specifies the duration of each high-speed accumulation for SYSREF Calibration. If the SYSREF period exceeds the supported value, calibration will fail. Larger values will increase calibration time and support longer SYSREF periods. For a given SYSREF period, larger values will also reduce the variance of the calibrated value. 0: 4 cycles per accumulation, max SYSREF period of 85 DEVCLK cycles 1: 16 cycles per accumulation, max SYSREF period of 1100 DEVCLK cycles 2: 64 cycles per accumulation, max SYSREF period of 5200 DEVCLK cycles 3: 256 cycles per accumulation, max SYSREF period of 21580 DEVCLK cycles Max duration of SYSREF calibration is bounded by: $T_{SYSREFCAL}$ (in DEVCLK cycles) = $256 * 19 * 4^{(SRC\_AVG + SRC\_HDUR + 2)}$

7.6.2.3 SYSREF Calibration Status Register (address = 0x2B2 to 0x2B4) [reset = Undefined]

Figure 175. SYSREF Calibration Status Register (SRC_STATUS)

23	22	21	20	19	18	17	16
RESERVED						SRC_DONE	SRC_TAD[16]
R						R	R
15	14	13	12	11	10	9	8
SRC_TAD[15:8]							
R							
7	6	5	4	3	2	1	0
SRC_TAD[7:0]							
R							

Table 140. SRC_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
23-18	RESERVED	R	Undefined	RESERVED
17	SRC_DONE	R	Undefined	This bit returns '1' when SRC_EN=1 and SYSREF Calibration has been completed
16-0	SRC_TAD	R	Undefined	This field returns the value for tad[16:0] computed by SYSREF Calibration. It is only valid if SRC_DONE=1.

7.6.2.4 DEVCLK Aperture Delay Adjustment Register (address = 0x2B5 to 0x2B7) [reset = 0x000000]

Figure 176. DEVCLK Aperture Delay Adjustment Register (TAD)

23	22	21	20	19	18	17	16
RESERVED							TAD_INV
R/W-0000 000							R/W-0
15	14	13	12	11	10	9	8
TAD_COARSE							
R/W-0000 0000							
7	6	5	4	3	2	1	0
TAD_FINE							
R/W-0000 0000							

Table 141. TAD Field Descriptions

Bit	Field	Type	Reset	Description
23-17	RESERVED	R/W	0000 000	RESERVED
16	TAD_INV	R/W	0	Invert DEVCLK by setting this bit equal to 1
15-8	TAD_COARSE	R/W	0000 0000	This register controls the DEVCLK aperture delay adjustment when SRC_EN=0. Use this register to manually control the DEVCLK aperture delay when SYSREF Calibration is disabled. If ADC calibration or JESD204B is running, it is recommended that you gradually increase or decrease this value (1 code at a time) to avoid clock glitches. Refer to Switching Characteristics for TAD_COARSE resolution.
7-0	TAD_FINE	R/W	0000 0000	Refer to Switching Characteristics for TAD_FINE resolution.

7.6.2.5 DEVCLK Timing Adjust Ramp Control Register (address = 0x2B8) [reset = 0x00]

Figure 177. DEVCLK Timing Adjust Ramp Control Register (TAD_RAMP)

7	6	5	4	3	2	1	0
RESERVED						TAD_RAMP_RATE	TAD_RAMP_EN
R/W-0000 00						R/W-0	R/W-0

Table 142. TAD_RAMP Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1	TAD_RAMP_RATE	R/W	0	Specifies the ramp rate for the tad[15:8] output when the TAD[15:8] register is written while TAD_RAMP_EN=1. 0: tad[15:8] ramps up or down one code per 256 DEVCLK cycles. 1: tad[15:8] ramps up or down 4 codes per 256 DEVCLK cycles.
0	TAD_RAMP_EN	R/W	0	TAD Ramp enable. Set this bit if you want the coarse TAD adjustments to ramp up or down instead of changing abruptly. 0: After writing the TAD[15:8] register the tad[15:7] output port is updated within 1024 DEVCLK cycles. 1: After writing the TAD[15:8] register the tad[15:7] output port ramps up or down until it matches the TAD[15:8] register.

7.6.3 Alarm Registers (0x2C0 to 0x2C2)

Table 143. Alarm Registers

Address	Reset	Acronym	Register Name	Section
0x2C0	Undefined	ALARM	Alarm Interrupt Status Register	Alarm Interrupt Register (address = 0x2C0) [reset = Undefined]
0x2C1	0x1F	ALM_STATUS	Alarm Status Register	Alarm Status Register (address = 0x2C1) [reset = 0x1F]
0x2C2	0x1F	ALM_MASK	Alarm Mask Register	Alarm Mask Register (address = 0x2C2) [reset = 0x1F]

7.6.3.1 Alarm Interrupt Register (address = 0x2C0) [reset = Undefined]

Figure 178. Alarm Interrupt Register (ALARM)

7	6	5	4	3	2	1	0
RESERVED							ALARM
R							R

Table 144. ALARM Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	Undefined	RESERVED
0	ALARM	R	Undefined	This bit returns a ‘1’ whenever any alarm occurs that is unmasked in the ALM_STATUS register. Use ALM_MASK to mask (disable) individual alarms. CAL_STATUS_SEL can be used to drive the ALARM bit onto the CALSTAT output pin to provide a hardware alarm interrupt signal.

7.6.3.2 Alarm Status Register (address = 0x2C1) [reset = 0x1F]

Figure 179. Alarm Status Register (ALM_STATUS)

7	6	5	4	3	2	1	0
RESERVED			PLL_ALM	LINK_ALM	REALIGNED_ALM	NCO_ALM	CLK_ALM
R/W-000			R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Table 145. ALM_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	RESERVED
4	PLL_ALM	R/W	1	PLL Lock Lost Alarm: This bit is set whenever the PLL is not locked. Write a ‘1’ to clear this bit.
3	LINK_ALM	R/W	1	Link Alarm: This bit is set whenever the JESD204B link is enabled, but is not in the DATA_ENC state. Write a ‘1’ to clear this bit.
2	REALIGNED_ALM	R/W	1	Realigned Alarm: This bit is set whenever SYSREF causes the internal clocks (including the LMFC) to be realigned. Write a ‘1’ to clear this bit.
1	NCO_ALM	R/W	1	NCO Alarm: This bit can be used to detect an upset to the NCO phase. This bit is set when any of the following occur: • The NCOs are disabled (JESD_EN=0) • The NCOs are synchronized (intentionally or unintentionally) • Any phase accumulators in channel A do not match channel B Write a ‘1’ to clear this bit.
0	CLK_ALM	R/W	1	Clock Alarm: This bit can be used to detect an upset to the digital block and JESD204B clocks. This bit is set whenever the internal clock dividers for the A and B channels do not match. Write a ‘1’ to clear this bit.

7.6.3.3 Alarm Mask Register (address = 0x2C2) [reset = 0x1F]

Figure 180. Alarm Mask Register (ALM_MASK)

7	6	5	4	3	2	1	0
RESERVED			MASK_PLL_ALM	MASK_LINK_ALM	MASK_REALIGNED_ALM	MASK_NCO_ALM	MASK_CLK_ALM
R/W-000			R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Table 146. ALM_MASK Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	RESERVED
4	MASK_PLL_ALM	R/W	1	When set, PLL_ALM is masked and will not impact the ALARM register bit
3	MASK_LINK_ALM	R/W	1	When set, LINK_ALM is masked and will not impact the ALARM register bit
2	MASK_REALIGNED_ALM	R/W	1	When set, REALIGNED_ALM is masked and will not impact the ALARM register bit
1	MASK_NCO_ALM	R/W	1	When set, NCO_ALM is masked and will not impact the ALARM register bit
0	MASK_CLK_ALM	R/W	1	When set, CLK_ALM is masked and will not impact the ALARM register bit

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application

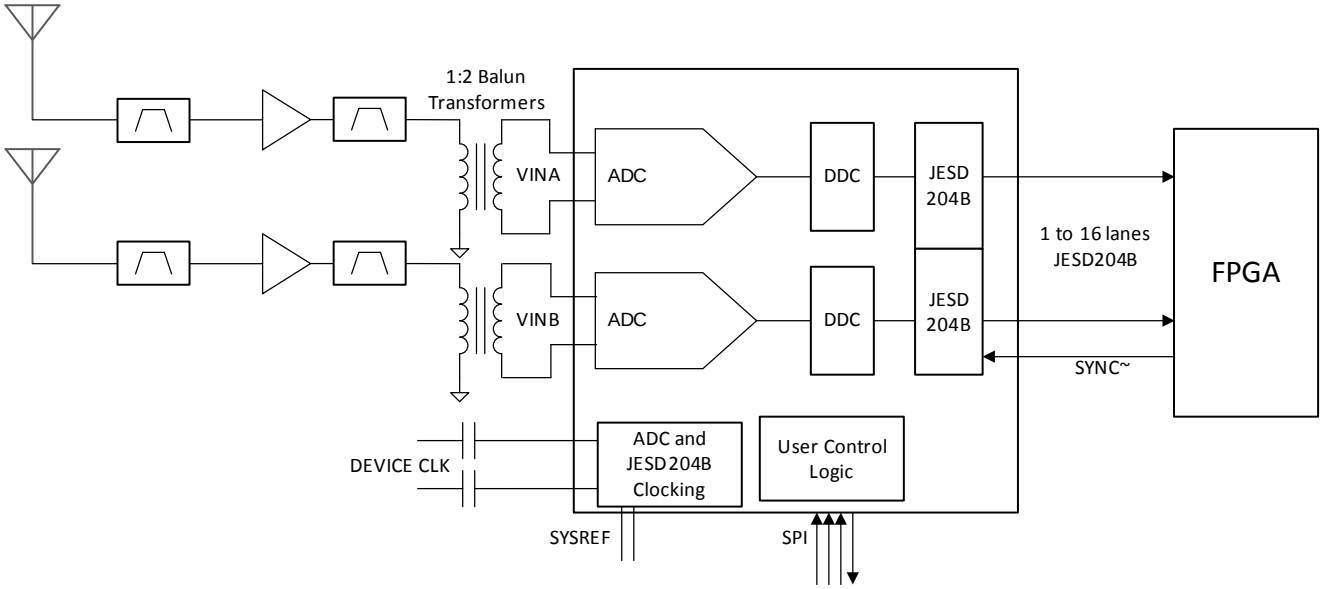


Figure 181. Typical Configuration for Wideband RF Sampling

8.2.1 Design Requirements

8.2.1.1 Input Signal Path

Appropriate band limiting filters should be utilized to reject unwanted frequencies in the input signal path.

A 1:2 balun transformer is needed to convert the 50-Ω single-ended signal to 100-Ω differential for input to the ADC. The balun outputs can be either AC-coupled, or directly connected to the ADC differential inputs, which are terminated internally to GND.

Drivers should be selected to provide any needed signal gain, and which have the necessary bandwidth capabilities.

Baluns should be selected to cover the needed frequency range, have a 1:2 impedance ratio, and have acceptable Gain and Phase balance over the frequency range of interest. The table below lists a number of recommended baluns for different frequency ranges.

Table 147. Recommended Baluns

Part Number	Manufacturer(1)	Minimum Frequency (MHz)	Maximum Frequency (MHz)
BAL-0009SMG	Marki Microwave	0.5	9000
BAL-0208SMG	Marki Microwave	2000	8000
TCM2-43X+	Mini-Circuits	10	4000
TCM2-33WX+	Mini-Circuits	10	3000

(1) See Third-party Products Disclaimer

Typical Application (continued)

Table 147. Recommended Baluns (continued)

Part Number	Manufacturer(1)	Minimum Frequency (MHz)	Maximum Frequency (MHz)
B0430J50100AHF	Anaren	400	3000

8.2.1.2 Clocking

The ADC12DJ3200clock inputs must be AC-coupled to the device to ensure rated performance. The clock source must have extremely low jitter (integrated phase-noise) to enable rated performance. Recommended clock synthesizers include the following:

- LMX2594
- LMX2592
- LMX2582

The JESD204B data converter system (ADC plus FPGA) will require additional SYSREF and device clocks. The following devices are suitable to generate these clocks. Depending on the ADC clock frequency and jitter requirements, this device may also be usable as the system clock synthesizer:

- LMK04828
- LMK04826
- LMK04821

8.2.2 Detailed Design Procedure

Certain component values used in conjunction with the ADC12DJ3200 must be calculated based on system parameters. Those items are covered in this detailed design procedure section.

8.2.2.1 Calculating Values of AC-Coupling Capacitors

AC-coupling capacitors are used in the input CLK+/- and JESD204B output data pairs. The capacitor values must be large enough to address the lowest frequency signals of interest, but not so large as to cause excessively long startup biasing times, or unwanted parasitic inductance.

The minimum capacitor value can be calculated based on the lowest frequency signal that will be transferred through the capacitor. Given a 50-Ω single-ended clock or data path impedance, it is good practice to set the capacitor impedance to be <1 Ω at the lowest frequency of interest. This ensures minimal impact on signal level at that frequency. For the CLK+/- path, the minimum rated clock frequency is 800 MHz. Therefore the minimum capacitor value can be calculated from:

$$Z_C = 1/\left(2 \times \pi \times f_{CLK} \times C\right) \tag{12}$$

Setting Z_c = 1 Ω and rearranging gives:

$$C = 1/\left(2 \times \pi \times 800\ \text{MHz} \times 1\ \Omega\right) = 199\ \text{pF} \tag{13}$$

Therefore a capacitance value of at least 199 pF is needed to provide the low frequency response for the CLK+/- path. If the minimum clock frequency will be higher than 800 MHz this calculation can be revisited for that frequency. Similar calculations can be done for the JESD204B output data capacitors based on the minimum frequency in that interface. Capacitors should also be selected for good response at high frequencies, and with dimensions that match the high frequency signal traces they are connected to. '0201' size capacitors are frequently well suited to these applications.

8.2.3 Application Curves

The ADC12DJ3200can be used in a number of different operating modes to suit multiple applications. The 3 plots that follow illustrate operation with a 497.77 MHz input signal in the following configurations:

- 6.4 GSPS, Single Input Mode, 12-bit Output, JMODE0
- 3.2 GSPS, Dual Input Mode, 12-bit Output, JMODE2
- 3.2 GSPS with 16x Decimation, Dual Input Mode, 15+15-bit Complex Output, JMODE11

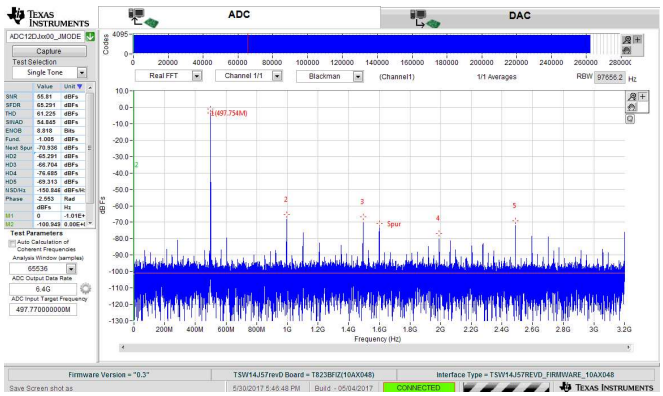


Figure 182. FFT for 497.77 MHz Input Signal, 6.4 GSPS, JMODE0

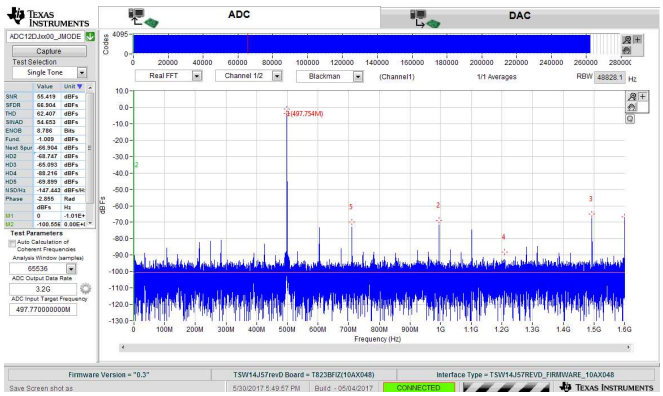


Figure 183. FFT for 497.77 MHz Input Signal, 3.2 GSPS, JMODE2

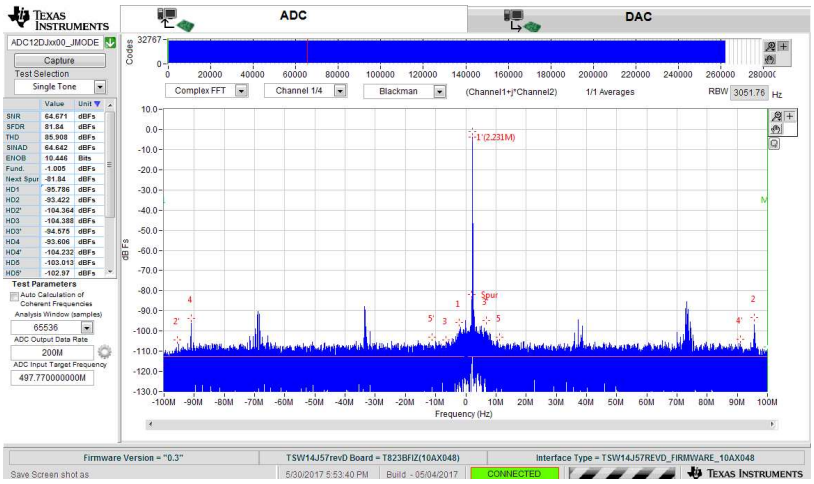


Figure 184. FFT for 497.77 MHz Input Signal, 3.2 GSPS, Decimation-by-16, f_{NCO} = 500 MHz, JMODE11

8.3 Initialization Set Up

The device and JESD204 interface requires a specific startup and alignment sequence. The general order of that sequence is listed in the following steps.

1. Power up or reset the device.
2. Apply stable device CLK signal at desired frequency.
3. Program JESD_EN=0 to stop the JESD204B state machine and allow setting changes.
4. Program CAL_EN=0 to stop the calibration state machine and allow setting changes.
5. Program desired JMODE.
6. Program desired KM1 value. KM1 = K-1.
7. Program SYNC_SEL as needed. Choose SYNCSE or Timestamp differential inputs.
8. Configure device calibration settings as desired. Select Foreground or Background calibration modes and Offset calibration as needed.
9. Program CAL_EN=1 to enable the calibration state machine.
10. Enable over-range via OVR_EN and adjust settings if desired.
11. Program JESD_EN=1 to re-start the JESD204B state machine and allow the link to re-start.
12. JESD204B interface will operate in response to applied SYNC signal from receiver.
13. Program CAL_SOFT_TRIG=0.
14. Program CAL_SOFT_TRIG=1 to initiate a calibration.

9 Power Supply Recommendations

The device requires 2 different power supply voltages. 1.9 V DC is required for the VA19 power bus and 1.1 V DC is required for the VA11 and VD11 power buses.

The power supply voltages must be low noise and provide the needed current to achieve rated device performance.

There are two recommended power supply architectures:

1. Stepdown using high efficiency switching converters, followed by a second stage of regulation to provide switching noise reduction and improved voltage accuracy.
2. Direct stepdown the final ADC supply voltage using high efficiency switching converters. This approach provides the best efficiency, but care must be taken to ensure switching noise is minimized to prevent degraded ADC performance.

TI WEBENCH® Power Designer can be used to select and design the individual power supply elements needed: http://www.ti.com/lsds/ti/analog/webench/power.page

Recommended switching regulators for the first stage include the TPS62085, TPS82130, TPS62130A and similar devices.

Recommended Low Drop-Out (LDO) linear regulators include the TPS7A7200, TPS74401 and similar devices.

For the switcher only approach, it is critical to design the ripple filter with a notch frequency that aligns with the switching ripple frequency of the DC-DC converter. Note the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed. Figure 185 and Figure 186 below illustrate the two approaches:

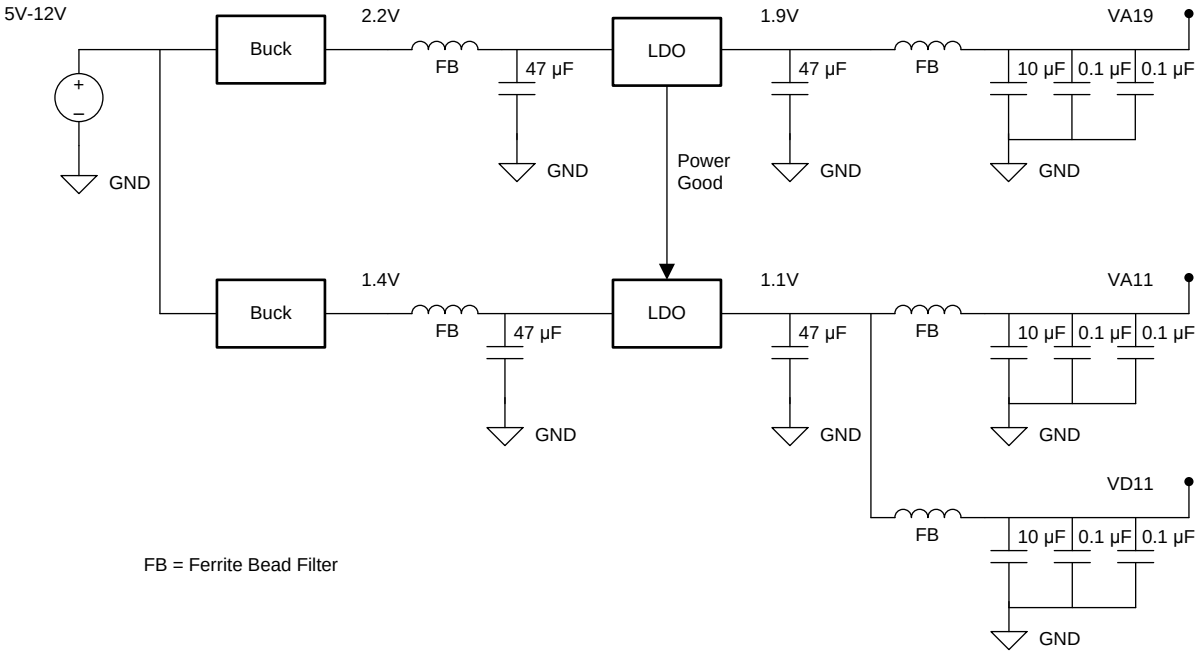


Figure 185. Example LDO Linear Regulator Approach

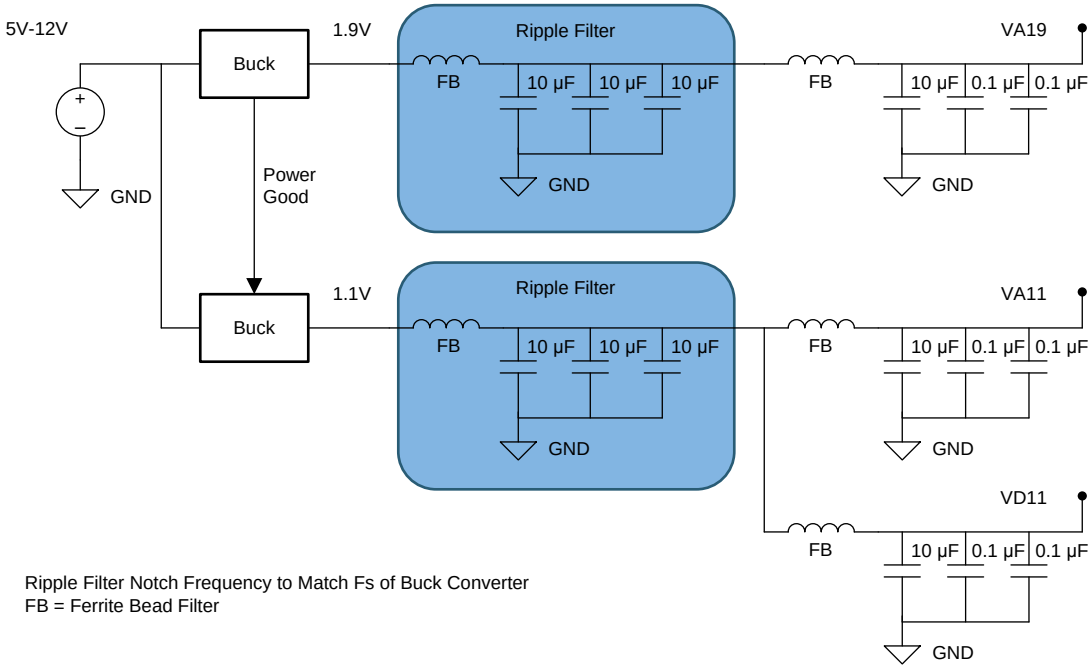


Figure 186. Example Switcher-Only Approach

Power Sequencing

The voltage regulators should be sequenced using the Power Good outputs and Enable inputs to ensure that the Vx11 regulator is enabled after the VA19 supply is good. Similarly, as soon as the VA19 supply drops out of regulation on power-down, the Vx11 regulator will be disabled.

The general requirement for the ADC is that VA19 ≥ Vx11 during power-up, operation, and power-down.

TI also recommends that VA11 and VD11 are derived from a common 1.1-V regulator. This ensures that all of the 1.1-V blocks are at the same voltage, and no sequencing problems exist between these supplies. Ferrite bead filters should be used to isolate any noise on the VA11 and VD11 buses from affecting each-other.

10 Layout

10.1 Layout Guidelines

There are many critical signals which require specific care during board design:

1. Analog Input Signals
2. CLK and SYSREF
3. JESD204B Data Outputs
   (a) a. Lower 8 pairs operating at up to 12.8 Gbit/sec
   (b) b. Upper 8 pairs operating at up to 6.4 Gbit/sec
4. Power Connections
5. Ground Connections

Items 1, 2 and 3 must be routed for excellent signal quality at high frequencies. The following general practices should be used:

1. Route using loosely coupled 100-Ω differential traces. This will minimize impact of corners and length matching serpentines on pair impedance.
2. Provide adequate pair to pair spacing to minimize crosstalk.
3. Provide adequate ground plane pour spacing to minimize coupling with the high speed traces.
4. Use smoothly radiused corners. Avoid 45 or 90 degree bends.
5. Incorporate ground plane cutouts at component landing pads to avoid impedance discontinuities at these locations. Cut-out below the landing pads on one or multiple ground planes to achieve a pad size/stackup height that achieves the needed 50 ohm single ended impedance.
6. Avoid routing traces near irregularities in the reference ground planes. This includes ground plane clearances associated with power and signal vias and through-hole component leads.
7. Provide symmetrically located ground tie vias adjacent to any high speed signal vias.
8. When high speed signals must transition to another layer using vias, transition as far through the board as possible (top to bottom is best case) to minimize via stubs on top and/or bottom of the vias. If layer selection is not flexible, use back-drilled or buried/blind vias to eliminate stubs.

In addition, TI recommends performing signal quality simulations of the critical signal traces before committing to fabrication. Insertion Loss, Return Loss and TDR (Time Domain Reflectometry) evaluations should be done.

The Power and Ground connections for the device are also very important. The following rules should be followed:

1. Provide low resistance connection paths to all power and ground pins.
2. Use multiple power layers if necessary to access all pins.
3. Avoid narrow isolated paths which increase the connection resistance.
4. Use a Signal/Ground/Power circuit board stackup to maximum coupling between the Ground and Power planes.

10.2 Layout Example

The following 3 figures provide examples of the critical traces routed on the device EVM (EValuation Module):

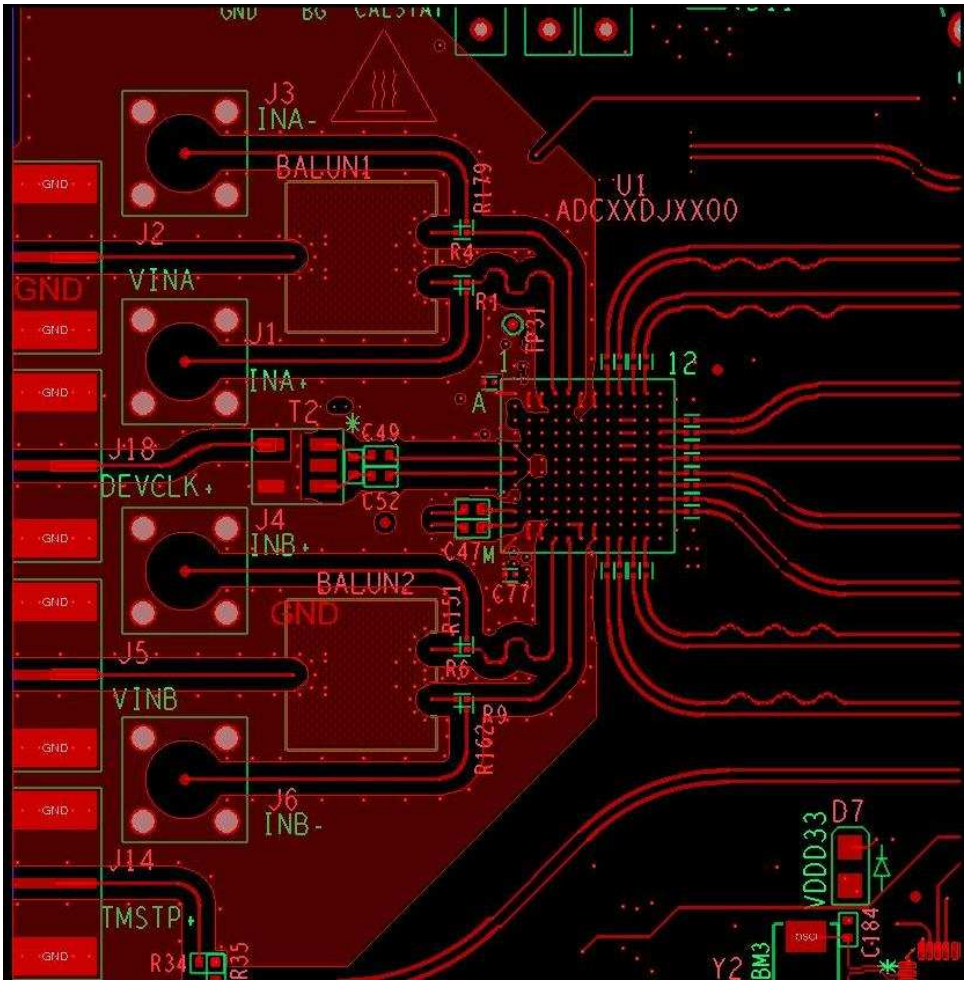


Figure 187. Top Layer Routing - Analog Inputs, CLK and SYSREF, DA0-3, DB0-3

Layout Example (continued)

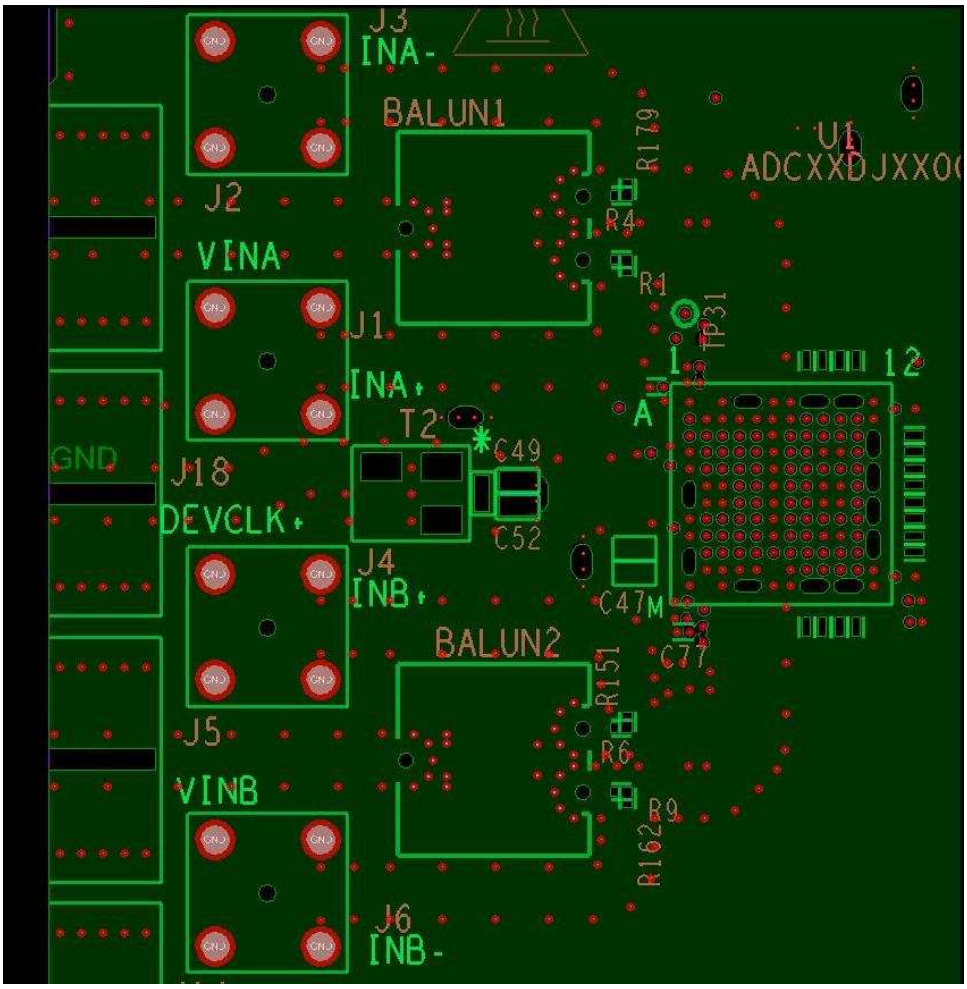


Figure 188. GND1 Cutouts to Optimize Impedance of Component Pads

Layout Example (continued)

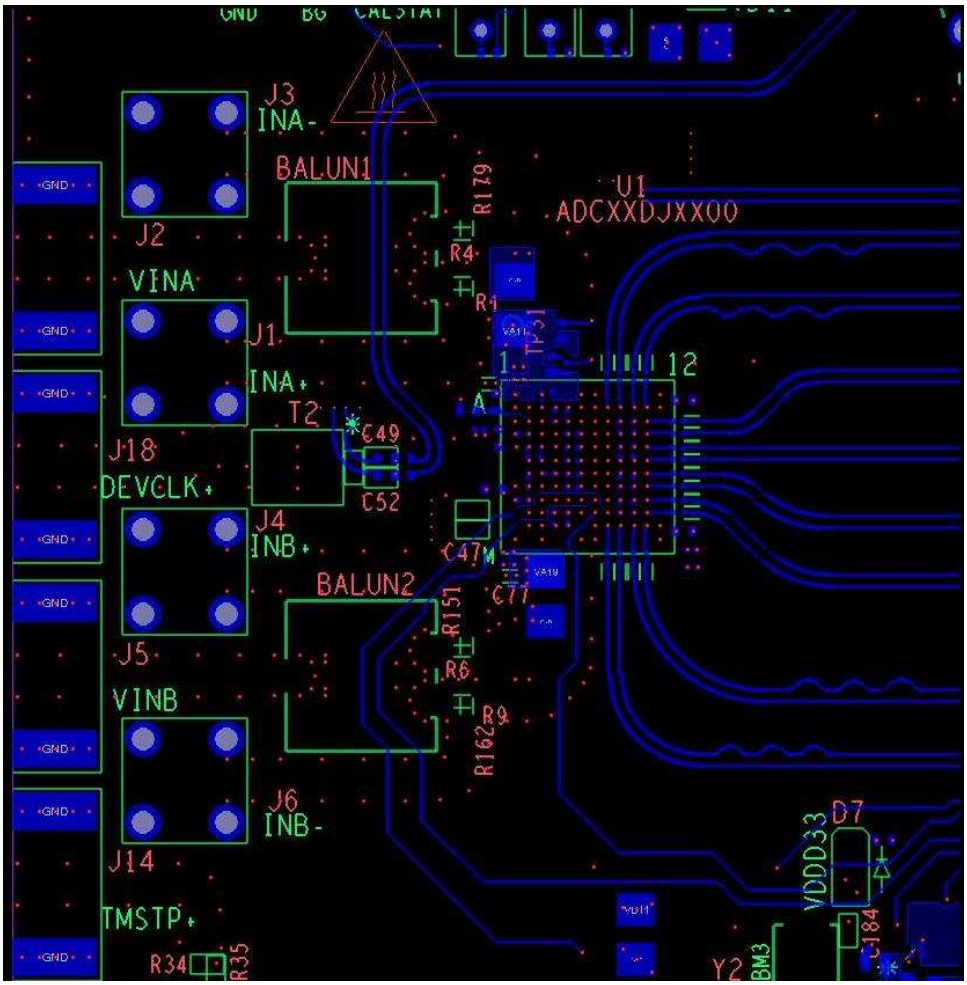


Figure 189. Bottom Layer Routing - Additional CLK Routing, DA4-7, DB4-7

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 148. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADC12DJ3200	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC12DJ3200AAV	ACTIVE	FCBGA	AAV	144	1	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADC12DJ32	Samples
ADC12DJ3200AAVT	ACTIVE	FCBGA	AAV	144	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADC12DJ32	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

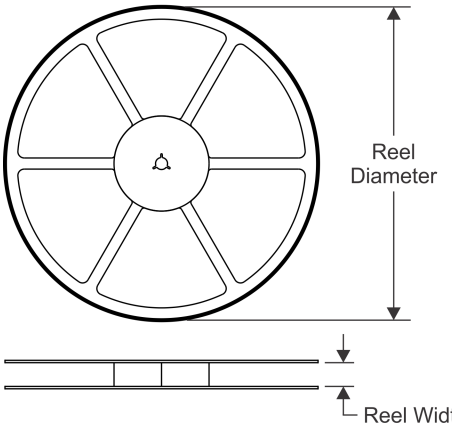
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

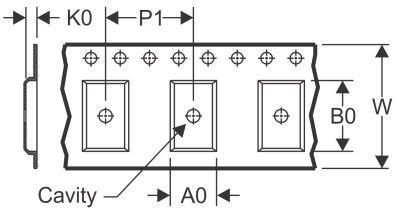
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

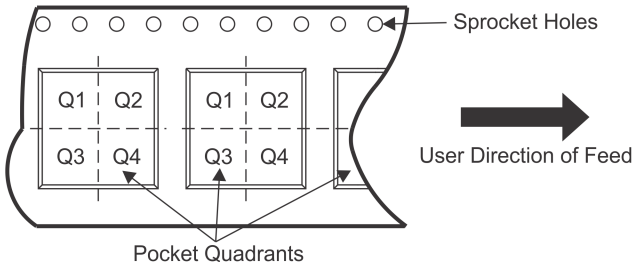


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

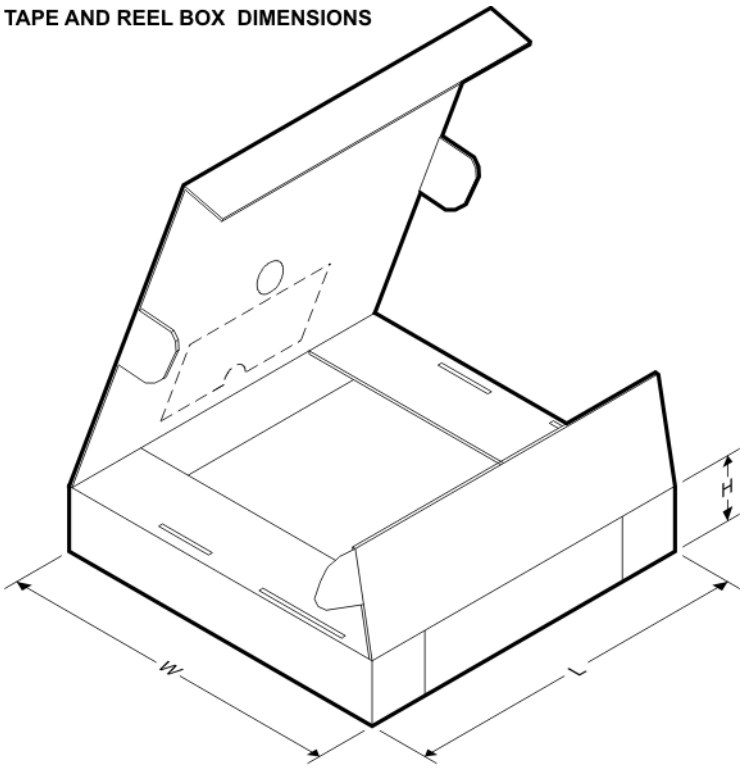
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC12DJ3200AAVT	FCBGA	AAV	144	250	180.0	24.4	10.3	10.3	2.5	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

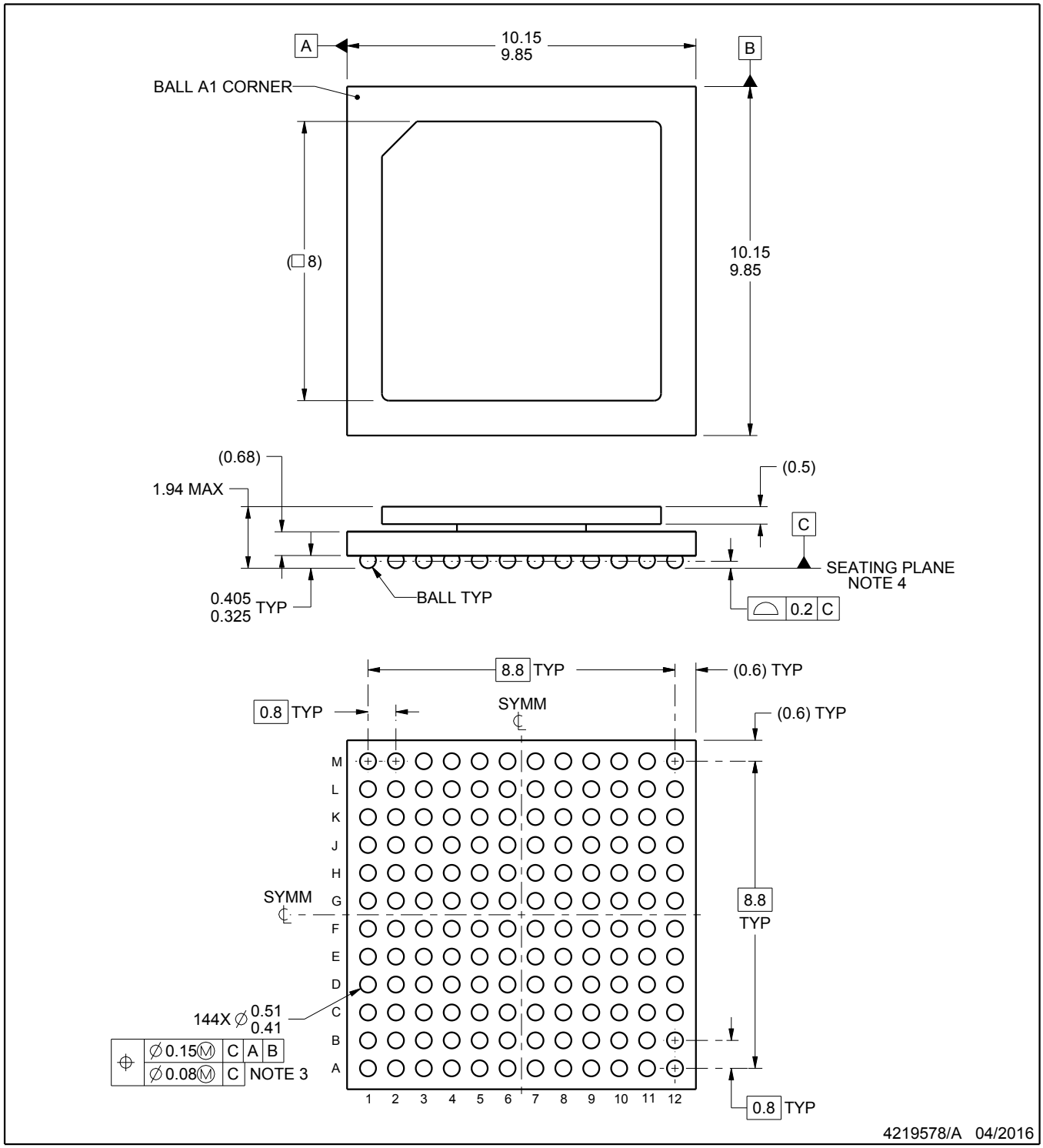
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC12DJ3200AAVT	FCBGA	AAV	144	250	213.0	191.0	55.0

PACKAGE OUTLINE

AAV0144A

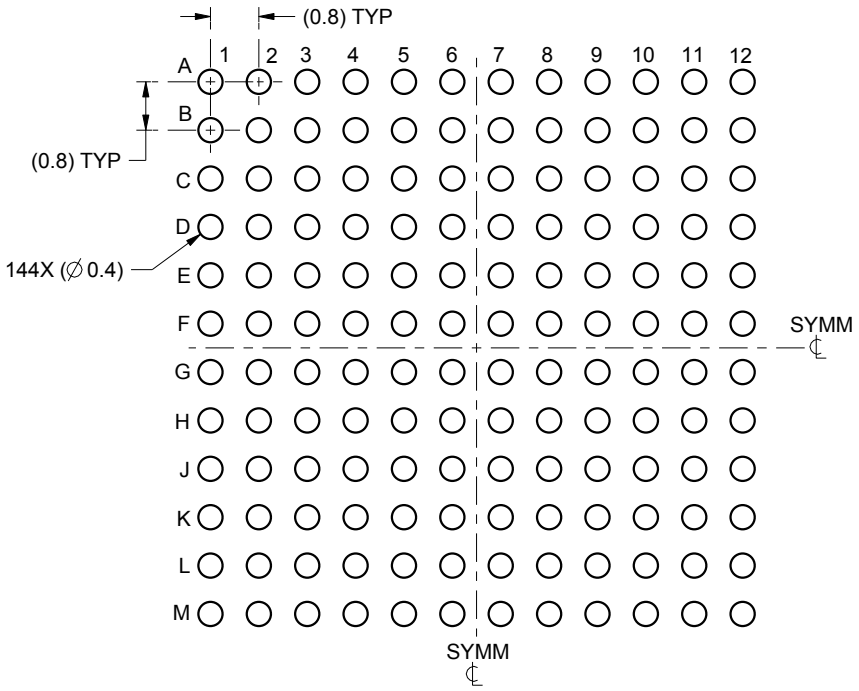
FCBGA - 1.94 mm max height

BALL GRID ARRAY

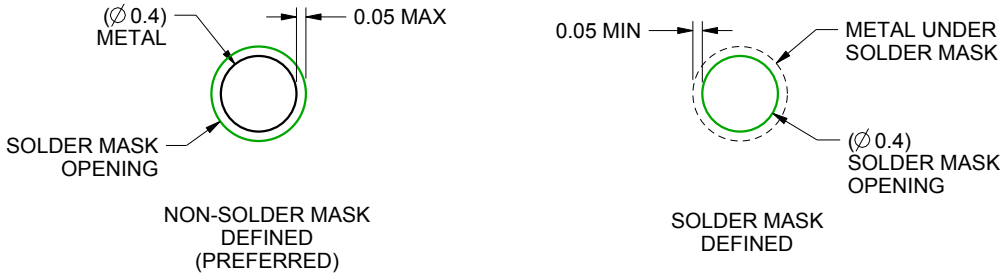


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.



LAND PATTERN EXAMPLE
SCALE:8X

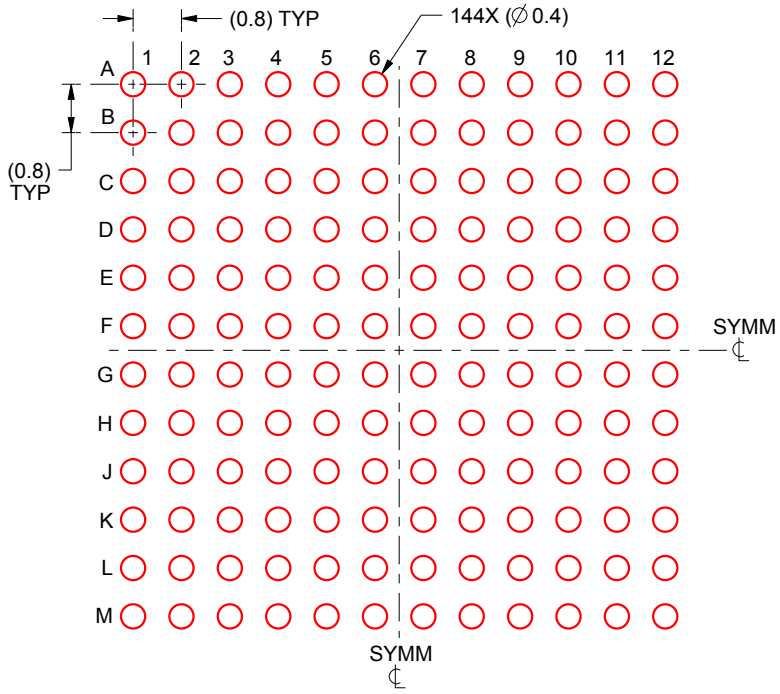


SOLDER MASK DETAILS
NOT TO SCALE

4219578/A 04/2016

NOTES: (continued)

5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4219578/A 04/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265