ADC128S102QML 8-Channel, 50 kSPS to 1 MSPS, 12-Bit A/D Converter

Check for Samples: ADC128S102QML

FEATURES

- **Total Ionizing Dose 100 krad(Si)**
- **Single Event Latch-up 120 MeV-cm^2/mg**
- **Eight input channels**
- **Variable power management**
- **Independent analog and digital supplies**
- **SPI™/ QSPI™/ MICROWIRE™/DSP compatible**
- **Packaged in 16-lead Ceramic SOIC**

APPLICATIONS

- **Automotive Navigation**
- **Portable Systems**
- **Medical Instruments**
- **Mobile Communications**
- **Instrumentation and Control Systems**

DESCRIPTION

The ADC128S102 is a low-power, eight-channel CMOS 12-bit analog-to-digital converter specified for conversion throughput rates of 50 kSPS to 1 MSPS. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. It can be configured to accept up to eight input signals at inputs IN0 through IN7.

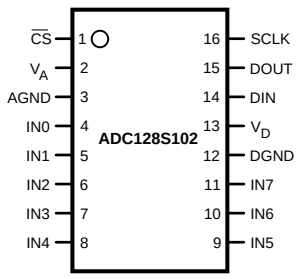
The output serial data is straight binary and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE™, and many common DSP serial interfaces.

The ADC128S102 may be operated with independent analog and digital supplies. The analog supply (V_A) can range from +2.7V to +5.25V, and the digital supply (V_D) can range from +2.7V to V_A. Normal power consumption using a +3V or +5V supply is 2.3 mW and 10.7 mW, respectively. The power-down feature reduces the power consumption to 0.06 µW using a +3V supply and 0.25 µW using a +5V supply.

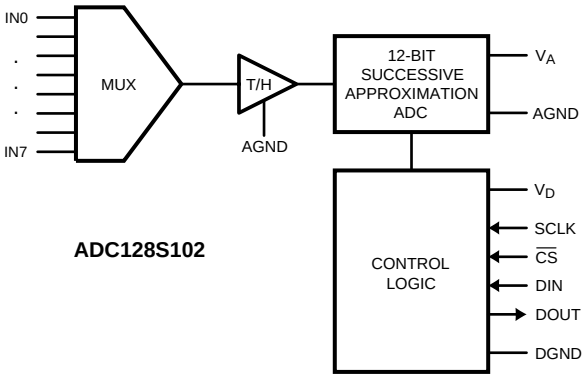
Table 1. Key Specifications

		VALUE	UNIT
Conversion Rate		50 kSPS to 1	MSPS
DNL (V_A = V_D = 5.0 V)		+1.5 / −0.9	LSB (max)
INL (V_A = V_D = 5.0 V)		+1.4 / −1.25	LSB (max)
Power Consumption			
	3V Supply	2.3	mW (typ)
	5V Supply	10.7	mW (typ)

Connection Diagram



Block Diagram



ADC128S102

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
4 - 11	IN0 to IN7		Analog inputs. These signals can range from 0V to V_{REF}.
DIGITAL I/O			
16	SCLK		Digital clock input. The guaranteed performance range of frequencies for this input is 0.8 MHz to 16 MHz. This clock directly controls the conversion and readout processes.
15	DOUT		Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
14	DIN		Digital data input. The ADC128S102QML's Control Register is loaded through this pin on rising edges of the SCLK pin.
1	$\overline{CS}$		Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
POWER SUPPLY			
2	V_A		Positive analog supply pin. This voltage is also used as the reference voltage. This pin should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with 1 µF and 0.1 µF monolithic ceramic capacitors located within 1 cm of the power pin.
13	V_D		Positive digital supply pin. This pin should be connected to a +2.7V to V_A supply, and bypassed to GND with a 0.1 µF monolithic ceramic capacitor located within 1 cm of the power pin.
3	AGND		The ground return for the analog supply and signals.
12	DGND		The ground return for the digital supply and signals.

Absolute Maximum Ratings (1)

Analog Supply Voltage V_A	−0.3V to 6.5V
Digital Supply Voltage V_D	−0.3V to V_A + 0.3V, max 6.5V
Voltage on Any Pin to GND	−0.3V to V_A +0.3V
Input Current at Any Pin (2)	±10 mA
Power Dissipation (3)	T_A = 25°C
Package Input Current (2)	±20 mA
ESD Susceptibility (4) Human Body Model	(Class 3A) 8000V
Soldering Temperature 10 seconds	260°C
Junction Temperature	+175°C
Storage Temperature	−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND or V_{IN} > V_A or V_D), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(3) The absolute maximum junction temperature ($T_J$max) for this device is 175°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the ADC128S102QML is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(4) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO ohms

Operating Ratings (1) (2)

Operating Temperature	
T_{MIN}	−55°C
T^{MAX}	+125°C
V_A Supply Voltage	+2.7V to +5.25V
V_D Supply Voltage	+2.7V to V_A
Digital Input Voltage	0V to V_A
Analog Input Voltage	0V to V_A
Clock Frequency	0.8 MHz to 16 MHz

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

Package Thermal Resistance

Package	θ_{JA}	θ_{JC}
16-lead Cerpack Gullwing	127°C/W	11.2°C/ W

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25

Subgroup	Description	Temp (°C)
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Setting time at	+25
13	Setting time at	+125
14	Setting time at	-55

ADC128S102QML Converter Electrical Characteristics

The following specifications apply for AGND = DGND = 0V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, C_L = 50pF, unless otherwise noted.

Symbol	Parameter	Conditions	Notes	Typical (1)	Min	Max	Units	Sub-groups
STATIC CONVERTER CHARACTERISTICS								
	Resolution with No Missing Codes					**12**	Bits	
INL	Integral Non-Linearity (End Point Method)	$V_A = V_D$ = +3.0V		±0.6	**−1.0**	**+1.1**	LSB	1, 2, 3
		$V_A = V_D$ = +5.0V		±0.9	**−1.25**	**+1.4**	LSB	1, 2, 3
DNL	Differential Non-Linearity	$V_A = V_D$ = +3.0V		+0.5		**+0.9**	LSB	1, 2, 3
				−0.3	**−0.7**		LSB	1, 2, 3
		$V_A = V_D$ = +5.0V		+0.9		**+1.5**	LSB	1, 2, 3
				−0.5	**−0.9**		LSB	1, 2, 3
V_{OFF}	Offset Error	$V_A = V_D$ = +3.0V		+0.8	**−2.3**	**+2.3**	LSB	1, 2, 3
		$V_A = V_D$ = +5.0V		+1.1	**−2.3**	**+2.3**	LSB	1, 2, 3
OEM	Offset Error Match	$V_A = V_D$ = +3.0V		±0.1	**−1.5**	**+1.5**	LSB	1, 2, 3
		$V_A = V_D$ = +5.0V		±0.3	**−1.5**	**+1.5**	LSB	1, 2, 3
FSE	Full Scale Error	$V_A = V_D$ = +3.0V		+0.8	**−2.0**	**+2.0**	LSB	1, 2, 3
		$V_A = V_D$ = +5.0V		+0.3	**−2.0**	**+2.0**	LSB	1, 2, 3
FSEM	Full Scale Error Match	$V_A = V_D$ = +3.0V		±0.1	**−1.5**	**+1.5**	LSB	1, 2, 3
		$V_A = V_D$ = +5.0V		±0.3	**−1.5**	**+1.5**	LSB	1, 2, 3
DYNAMIC CONVERTER CHARACTERISTICS								
FPBW	Full Power Bandwidth (−3dB)	$V_A = V_D$ = +3.0V		6.8			MHz	
		$V_A = V_D$ = +5.0V		10			MHz	
SINAD	Signal-to-Noise Plus Distortion Ratio	$V_A = V_D$ = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS		72	**68**		dB	4, 5, 6
		$V_A = V_D$ = +5.0V, f_{IN} = 40.2 kHz, −0.02 dBFS		72	**68**		dB	4, 5, 6
SNR	Signal-to-Noise Ratio	$V_A = V_D$ = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS		72	**69**		dB	4, 5, 6
		$V_A = V_D$ = +5.0V, f_{IN} = 40.2 kHz, −0.02 dBFS		72	**68.5**		dB	4, 5, 6
THD	Total Harmonic Distortion	$V_A = V_D$ = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS		−86		**−74**	dB	4, 5, 6
		$V_A = V_D$ = +5.0V, f_{IN} = 40.2 kHz, −0.02 dBFS		−87		**−74**	dB	4, 5, 6
SFDR	Spurious-Free Dynamic Range	$V_A = V_D$ = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS		91	**75**		dB	4, 5, 6
		$V_A = V_D$ = +5.0V, f_{IN} = 40.2 kHz, −0.02 dBFS		90	**75**		dB	4, 5, 6
ENOB	Effective Number of Bits	$V_A = V_D$ = +3.0V, f_{IN} = 40.2 kHz		11.6	**11.1**		Bits	4, 5, 6
		$V_A = V_D$ = +5.0V, f_{IN} = 40.2 kHz, −0.02 dBFS		11.6	**11.1**		Bits	4, 5, 6
ISO	Channel-to-Channel Isolation	$V_A = V_D$ = +3.0V, f_{IN} = 20 kHz		84			dB	
		$V_A = V_D$ = +5.0V, f_{IN} = 20 kHz, −0.02 dBFS		85			dB	

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms.

ADC128S102QML Converter Electrical Characteristics (continued)

The following specifications apply for AGND = DGND = 0V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, C_L = 50pF, unless otherwise noted.

Symbol	Parameter	Conditions	Notes	Typical (1)	Min	Max	Units	Sub-groups
IMD	Intermodulation Distortion, Second Order Terms	$V_A = V_D$ = +3.0V, f_a = 19.5 kHz, f_b = 20.5 kHz		−93		**−78**	dB	4, 5, 6
		$V_A = V_D$ = +5.0V, f_a = 19.5 kHz, f_b = 20.5 kHz		−93		**−78**	dB	4, 5, 6
	Intermodulation Distortion, Third Order Terms	$V_A = V_D$ = +3.0V, f_a = 19.5 kHz, f_b = 20.5 kHz		−91		**−70**	dB	4, 5, 6
		$V_A = V_D$ = +5.0V, f_a = 19.5 kHz, f_b = 20.5 kHz		−91		**−70**	dB	4, 5, 6
ANALOG INPUT CHARACTERISTICS								
V_{IN}	Input Range			0 to V_A			V	
I_{DCL}	DC Leakage Current			±0.01		**±1.0**	µA	1, 2, 3
C_{INA}	Input Capacitance	Track Mode	(2)	38			pF	
		Hold Mode	(2)	4.5			pF	
DIGITAL INPUT CHARACTERISTICS								
V_{IH}	Input High Voltage	$V_A = V_D$ = +2.7V to +3.6V			**2.1**		V	1, 2, 3
		$V_A = V_D$ = +4.75V to +5.25V			**2.4**		V	1, 2, 3
V_{IL}	Input Low Voltage	$V_A = V_D$ = +2.7V to +5.25V				**0.8**	V	1, 2, 3
I_{IN}	Input Current	V_{IN} = 0V or V_D		±1.0		**±1.0**	µA	1, 2, 3
C_{IND}	Digital Input Capacitance		(3)	3.5			pF (max)	
DIGITAL OUTPUT CHARACTERISTICS								
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA, $V_A = V_D$ = +2.7V to +5.25V			**V_D −0.5**		V	1, 2, 3
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA to 1.0 mA, $V_A = V_D$ = +2.7V to +5.25V				**0.4**	V	1, 2, 3
I_{OZH}, I_{OZL}	Hi-Impedance Output Leakage Current	$V_A = V_D$ = +2.7V to +5.25V		±0.01		**±1.0**	µA	1, 2, 3
C_{OUT}	Hi-Impedance Output Capacitance		(3)	3.5			pF (max)	
	Output Coding			Straight (Natural) Binary				
POWER SUPPLY CHARACTERISTICS (C_L = 10 pF)								
V_A, V_D	Analog and Digital Supply Voltages	$V_A \geq V_D$			**2.7**		V	1, 2, 3
						5.25	V	1, 2, 3
$I_A + I_D$	Total Supply Current Normal Mode ($\overline{CS}$ low)	$V_A = V_D$ = +2.7V to +3.6V, f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz		0.9		**1.5**	mA	1, 2, 3
		$V_A = V_D$ = +4.75V to +5.25V, f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz		2.2		**3.1**	mA	1, 2, 3
	Total Supply Current Shutdown Mode ($\overline{CS}$ high)	$V_A = V_D$ = +2.7V to +3.6V, f_{SCLK} = 0 kSPS		0.11		**1.0**	µA	1, 2, 3
		$V_A = V_D$ = +4.75V to +5.25V, f_{SCLK} = 0 kSPS		0.12		**1.4**	µA	1, 2, 3
P_C	Power Consumption Normal Mode ($\overline{CS}$ low)	$V_A = V_D$ = +3.0V f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz		2.7		**4.5**	mW	1, 2, 3
		$V_A = V_D$ = +5.0V f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz		11.0		**15.5**	mW	1, 2, 3
	Power Consumption Shutdown Mode ($\overline{CS}$ high)	$V_A = V_D$ = +3.0V f_{SCLK} = 0 kSPS		0.33		**3.0**	µW	1, 2, 3
		$V_A = V_D$ = +5.0V f_{SCLK} = 0 kSPS		0.6		**7.0**	µW	1, 2, 3

(2) This parameter is guaranteed by design and/or characterization and is not tested in production.
(3) This parameter is guaranteed by design and/or characterization and is not tested in production.

ADC128S102QML Converter Electrical Characteristics (continued)

The following specifications apply for AGND = DGND = 0V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, C_L = 50pF, unless otherwise noted.

Symbol	Parameter	Conditions	Notes	Typical (1)	Min	Max	Units	Sub-groups
AC ELECTRICAL CHARACTERISTICS								
f_{SCLK}MIN	Minimum Clock Frequency	$V_A = V_D$ = +2.7V to +5.25V			**0.8**		MHz	9, 10, 11
f_{SCLK}	Maximum Clock Frequency	$V_A = V_D$ = +2.7V to +5.25V				**16**	MHz	9, 10, 11
f_S	Sample Rate Continuous Mode	$V_A = V_D$ = +2.7V to +5.25V			**50**		kSPS	9, 10, 11
						1	MSPS	9, 10, 11
$t_{CONVERT}$	Conversion (Hold) Time	$V_A = V_D$ = +2.7V to +5.25V				**13**	SCLK cycles	9, 10, 11
DC	SCLK Duty Cycle	$V_A = V_D$ = +2.7V to +5.25V		40			%	
				60			%	
t_{ACQ}	Acquisition (Track) Time	$V_A = V_D$ = +2.7V to +5.25V				**3**	SCLK cycles	9, 10, 11
	Throughput Time	Acquisition Time + Conversion Time $V_A = V_D$ = +2.7V to +5.25V				**16**	SCLK cycles	9, 10, 11
t_{AD}	Aperture Delay	$V_A = V_D$ = +2.7V to +5.25V		4			ns	

Timing Specifications

The following specifications apply for $V_A = V_D$ = +2.7V to +5.25V, AGND = DGND = 0V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50pF.

Symbol	Parameter	Conditions	Notes	Typical (1)	Min	Max	Units	Sub-groups
t_{CSH}	$\overline{CS}$ Hold Time after SCLK Rising Edge		(2)	0	**10**		ns	9, 10, 11
t_{CSS}	$\overline{CS}$ Setup Time prior to SCLK Rising Edge		(2)	4.5	**10**		ns	9, 10, 11
t_{EN}	$\overline{CS}$ Falling Edge to DOUT enabled			5		**30**	ns	9, 10, 11
t_{DACC}	DOUT Access Time after SCLK Falling Edge			17		**27**	ns	9, 10, 11
t_{DHLD}	DOUT Hold Time after SCLK Falling Edge			4	**11**		ns	9, 10, 11
t_{DS}	DIN Setup Time prior to SCLK Rising Edge			3	**10**		ns	9, 10, 11
t_{DH}	DIN Hold Time after SCLK Rising Edge			3	**10**		ns	9, 10, 11
t_{CH}	SCLK High Time			0.4 X t_{SCLK}			ns (min)	
t_{CL}	SCLK Low Time			0.4 X t_{SCLK}			ns (min)	
t_{DIS}	$\overline{CS}$ Rising Edge to DOUT High-Impedance	DOUT falling		2.4		**20**	ns	9, 10, 11
		DOUT rising		0.9		**20**	ns	9, 10, 11

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms.
(2) Clock may be in any state (high or low) when $\overline{CS}$ goes high. Setup and hold time restrictions apply only to $\overline{CS}$ going low.

Radiation Electrical Characteristics (1)

The following specifications apply for $V_A = V_D$ = +2.7V to +5.25V, AGND = DGND = 0V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50pF.

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
$I_A + I_D$	Total Supply Current Shutdown Mode ($\overline{CS}$ high)	$V_A = V_D$ = +2.7V to +3.6V, f_{SCLK} = 0 kSPS				30	µA	1
		$V_A = V_D$ = +4.75V to +5.25V, f_{SCLK} = 0 kSPS				100	µA	1
I_{OZH}, I_{OZL}	Hi-Impedance Output Leakage Current	$V_A = V_D$ = +2.7V to +5.25V				±10	µA	1

(1) Pre and post irradiation limits are identical to those listed in the “DC Parameters” and “AC and Timing Characteristics” tables, except as listed in the “Radiation Electrical Characteristics” table. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

Burn In Delta Parameters T_A @ 25°C (1)

The following specifications apply for $V_A = V_D$ = +2.7V to +5.25V, AGND = DGND = 0V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50pF.

Symbol	Parameter	Conditions	Notes	Typical	Mim	Max	Units	Sub-groups
INL	Integral Non-LInearity	$V_A = V_D$ = 3.0V		.106	−0.5	+0.5	LSB	
		$V_A = V_D$ = +5.0V		.016	−0.35	+0.35	LSB	
IMD	Intermodulation Distortion, Second Order Terms	$V_A = V_D$ = 3.0V		1.35	−14	+14	dB	
		$V_A = V_D$ = 5.0V		1.67	−17	+17	dB	
IMD	Intermodulation Distortion, Third Order Terms	$V_A = V_D$ = 3.0V		.47	−10	+10	dB	
		$V_A = V_D$ = 5.0V		.90	−10	+10	dB	

(1) This is worse case drift, Deltas are performed at room temperature post operational life. All other parameters, no deltas are required.

Timing Diagrams

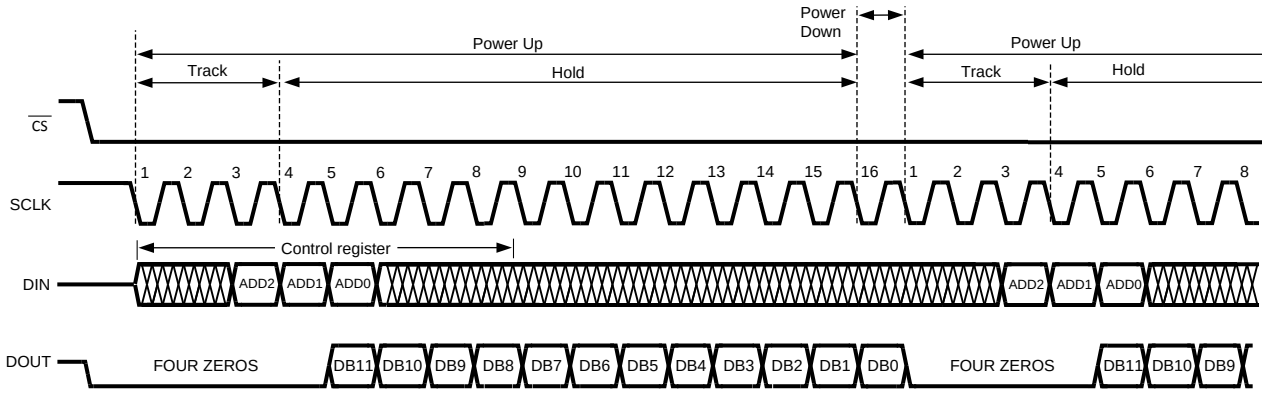


Figure 1. ADC128S102 Operational Timing Diagram

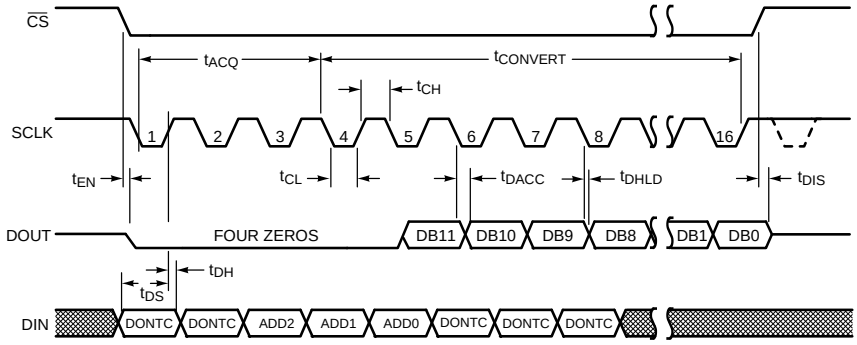


Figure 2. ADC128S102 Serial Timing Diagram

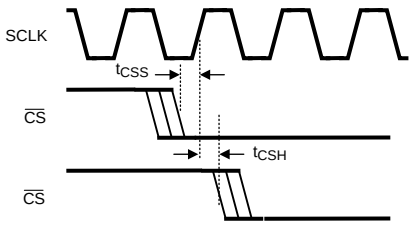


Figure 3. SCLK and $\overline{CS}$ Timing Parameters

Specification Definitions

ACQUISITION TIME is the time required for the ADC to acquire the input voltage. During this time, the hold capacitor is charged by the input voltage.

APERTURE DELAY is the time between the fourth falling edge of SCLK and the time when the input signal is internally acquired or held for conversion.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

CHANNEL-TO-CHANNEL ISOLATION is resistance to coupling of energy from one channel into another channel.

CROSSTALK is the coupling of energy from one channel into another channel. This is similar to Channel-to-Channel Isolation, except for the sign of the data.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} - 1.5 LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to an individual ADC input at the same time. It is defined as the ratio of the power in either the second or the third order intermodulation products to the sum of the power in both of the original frequencies. Second order products are $f_a \pm f_b$, where f_a and f_b are the two sine wave input frequencies. Third order products are ($2f_a \pm f_b$) and ($f_a \pm 2f_b$). IMD is usually expressed in dB.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC128S102 is guaranteed not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f10}^2}{A_{f1}^2}} \quad (1)$$

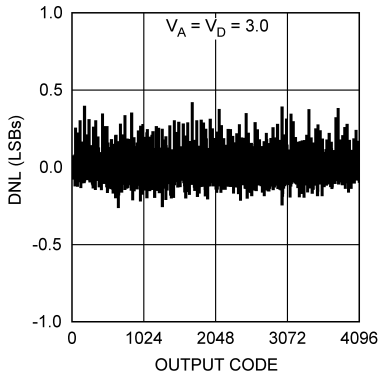
where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f10} are the RMS power in the first 9 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversions. It is the acquisition time plus the conversion time.

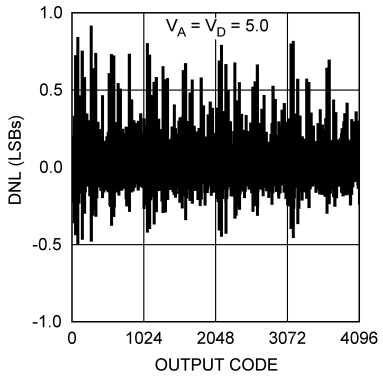
Typical Performance Characteristics

T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

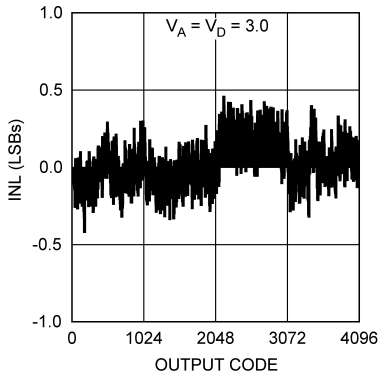
DNL



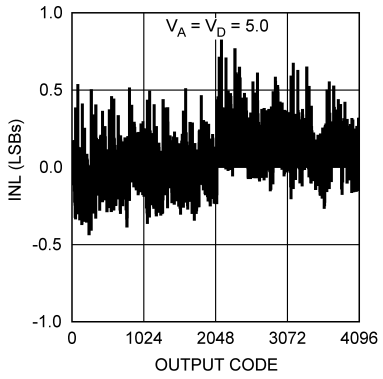
DNL



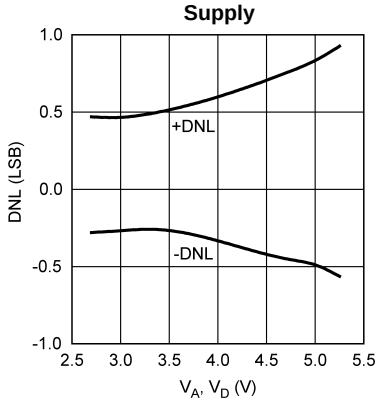
INL



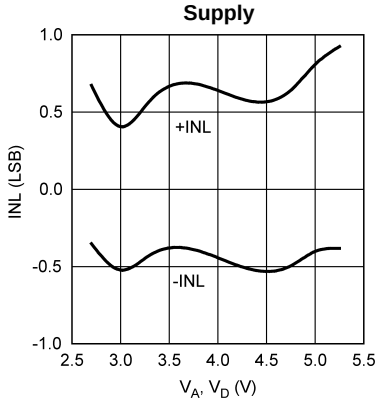
INL



DNL vs. Supply



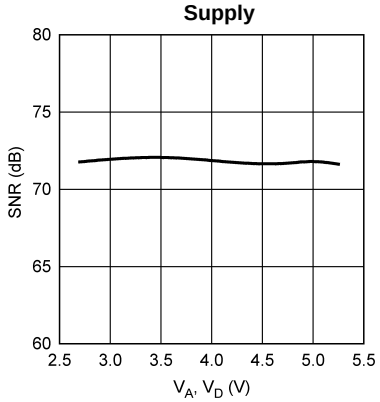
INL vs. Supply



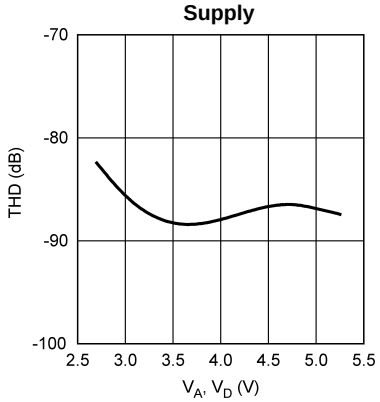
Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

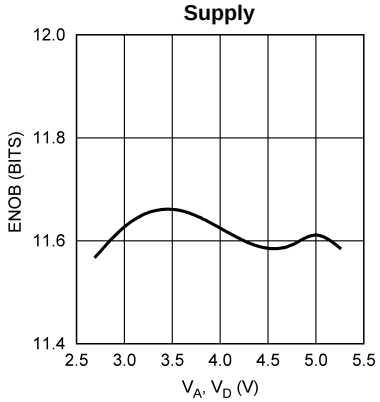
SNR vs. Supply



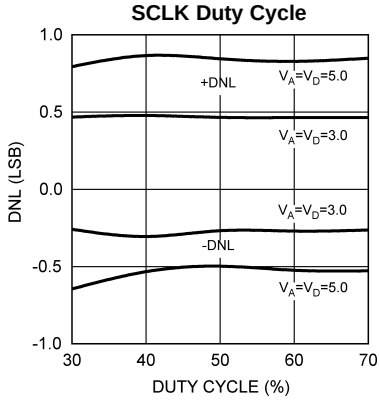
THD vs. Supply



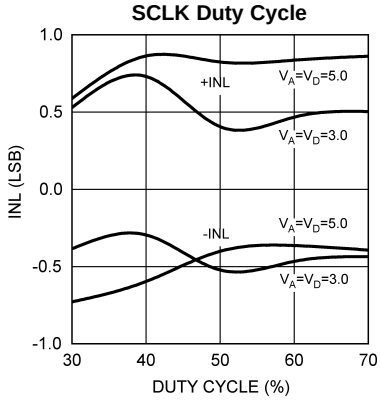
ENOB vs. Supply



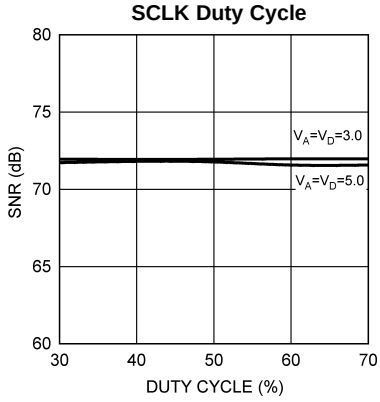
DNL vs. SCLK Duty Cycle



INL vs. SCLK Duty Cycle



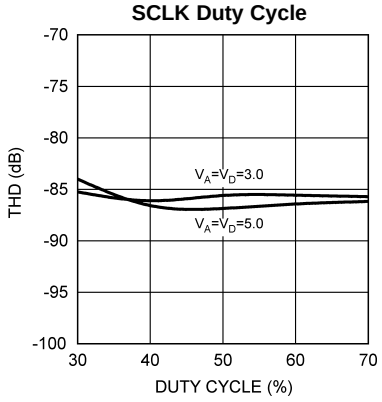
SNR vs. SCLK Duty Cycle



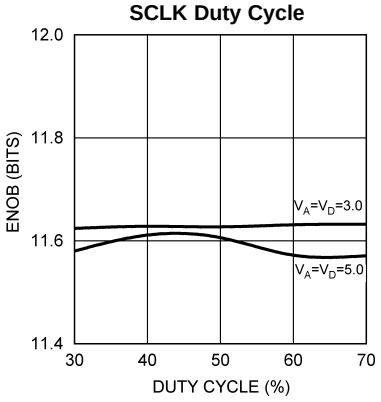
Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

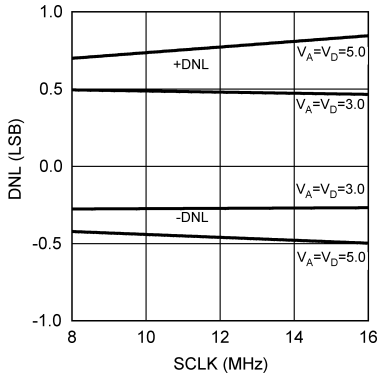
THD vs. SCLK Duty Cycle



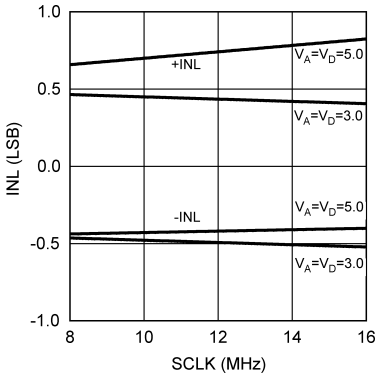
ENOB vs. SCLK Duty Cycle



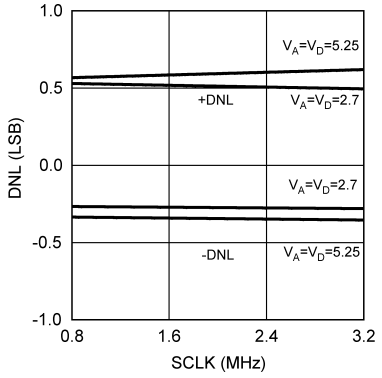
DNL vs. SCLK



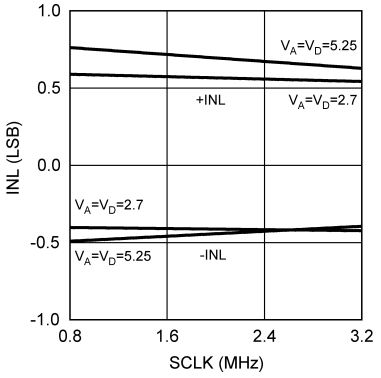
INL vs. SCLK



DNL vs. SCLK



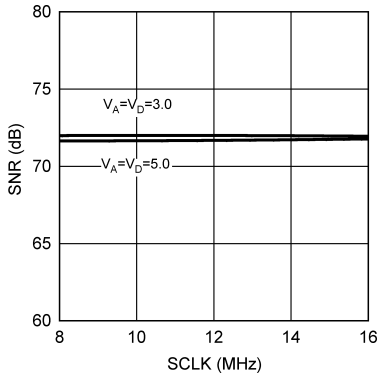
INL vs. SCLK



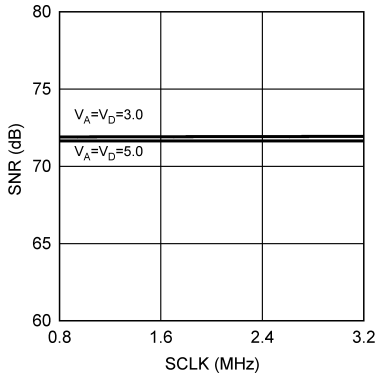
Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

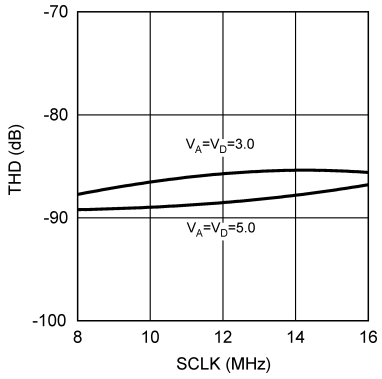
SNR vs. SCLK



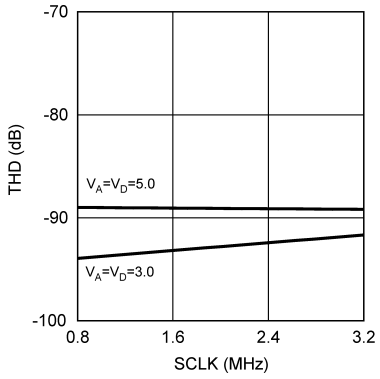
SNR vs. SCLK



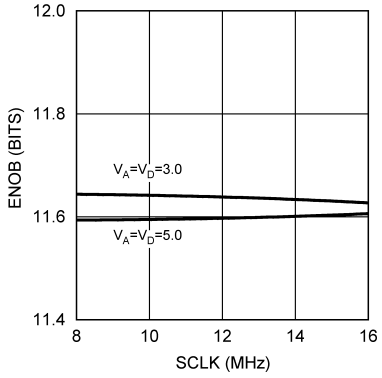
THD vs. SCLK



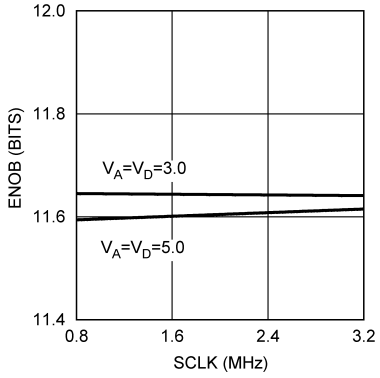
THD vs SCLK



ENOB vs. SCLK



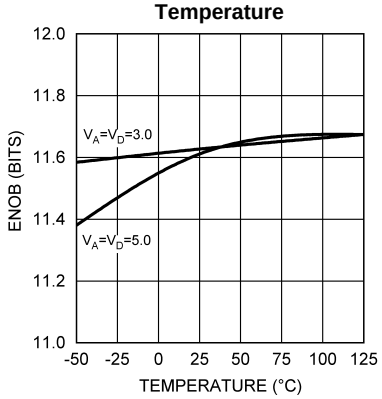
ENOB vs. SCLK



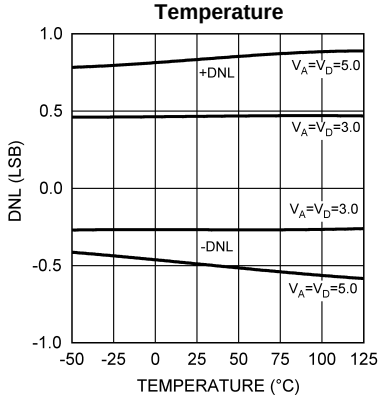
Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

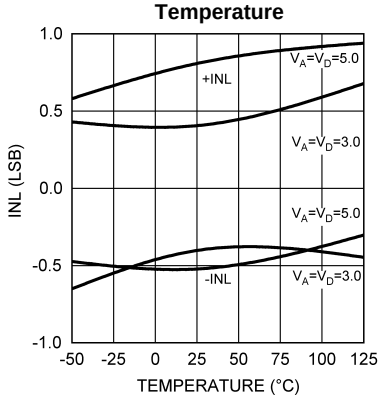
ENOB vs. Temperature



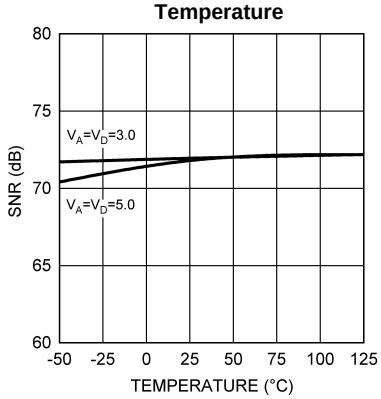
DNL vs. Temperature



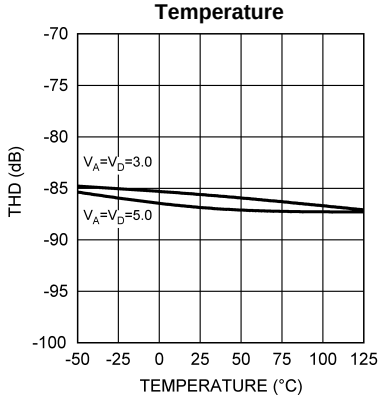
INL vs. Temperature



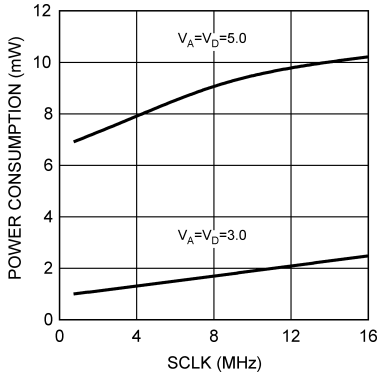
SNR vs. Temperature



THD vs. Temperature



Power Consumption vs. SCLK



Functional Description

The ADC128S102 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter.

ADC128S102 OPERATION

Simplified schematics of the ADC128S102 in both track and hold operation are shown in Figure 4 and Figure 5 respectively. In Figure 4, the ADC128S102 is in track mode: switch SW1 connects the sampling capacitor to one of eight analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC128S102 is in this state for the first three SCLK cycles after $\overline{CS}$ is brought low.

Figure 5 shows the ADC128S102 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge to or from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC128S102 is in this state for the last thirteen SCLK cycles after $\overline{CS}$ is brought low.

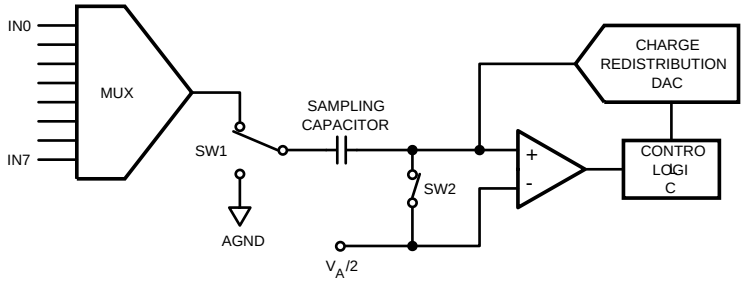


Figure 4. ADC128S102 in Track Mode

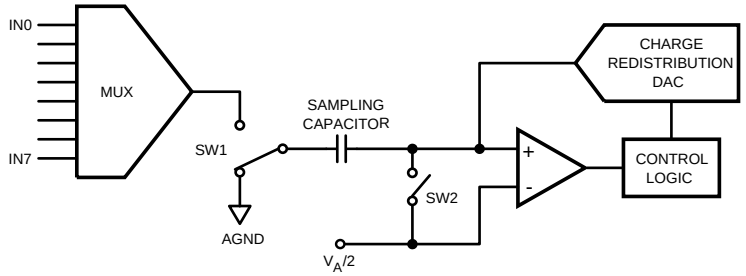


Figure 5. ADC128S102 in Hold Mode

SERIAL INTERFACE

An operational timing diagram and a serial interface timing diagram for the ADC128S102 are shown in The Timing Diagrams section. $\overline{CS}$, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the ADC128S102's Control Register is placed on DIN, the serial data input pin. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC's DOUT pin is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low. Thus, $\overline{CS}$ acts as an output enable. Similarly, SCLK is internally gated off when $\overline{CS}$ is brought high.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out. SCLK falling edges 1 through 4 clock out leading zeros while falling edges 5 through 16 clock out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC will re-enter the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK and re-enter the hold/convert mode on the N*16+4th falling edge of SCLK. "N" is an integer value.

The ADC128S102 enters track mode under three different conditions. In Figure 1, $\overline{CS}$ goes low with SCLK high and the ADC enters track mode on the first falling edge of SCLK. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC automatically enters track mode and the falling edge of $\overline{CS}$ is seen as the first falling edge of SCLK. In the third condition, $\overline{CS}$ and SCLK go low simultaneously and the ADC enters track mode. While there is no timing restriction with respect to the falling edges of $\overline{CS}$ and SCLK, see Figure 3 for setup and hold time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK.

During each conversion, data is clocked into a control register through the DIN pin on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. The control register is loaded with data indicating the input channel to be converted on the subsequent conversion (see Table 2 Table 3 Table 4).

Although the ADC128S102 is able to acquire the input signal to full resolution in the first conversion immediately following power-up, the first conversion result after power-up will be that of a randomly selected channel. Therefore, the user needs to incorporate a dummy conversion to set the required channel that will be used on the subsequent conversion.

Table 2. Control Register Bits

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DONTC	**DONTC**	**ADD2**	**ADD1**	**ADD0**	**DONTC**	**DONTC**	**DONTC**

Table 3. Control Register Bit Descriptions

Bit #:	Symbol:	Description
7, 6, 2, 1, 0	DONTC	Don't care. The values of these bits do not affect the device.
5	ADD2	These three bits determine which input channel will be sampled and converted at the next conversion cycle. The mapping between codes and channels is shown in Table 4.
4	ADD1	
3	ADD0	

Table 4. Input Channel Selection

ADD2	ADD1	ADD0	Input Channel
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

ADC128S102 TRANSFER FUNCTION

The output format of the ADC128S102 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC128S102 is V_A / 4096. The ideal transfer characteristic is shown in Figure 6. The transition from an output code of 0000 0000 0000 to a code of 0000 0000 0001 is at 1/2 LSB, or a voltage of V_A / 8192. Other code transitions occur at steps of one LSB.

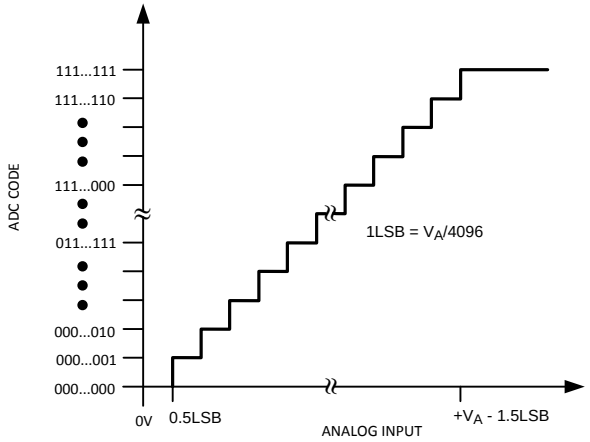


Figure 6. Ideal Transfer Characteristic

ANALOG INPUTS

An equivalent circuit for one of the ADC128S102's input channels is shown in Figure 7. Diodes D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0 V to V_A. Going beyond this range will cause the ESD diodes to conduct and result in erratic operation.

The capacitor C1 in Figure 7 has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch and is typically 500 ohms. Capacitor C2 is the ADC128S102 sampling capacitor, and is typically 30 pF. The ADC128S102 will deliver best performance when driven by a low-impedance source (less than 100 ohms). This is especially important when using the ADC128S102 to sample dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter which reduces harmonics and noise in the input. These filters are often referred to as anti-aliasing filters.

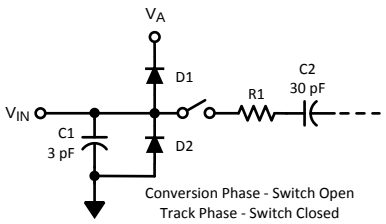


Figure 7. Equivalent Input Circuit

DIGITAL INPUTS AND OUTPUTS

The ADC128S102's digital inputs (SCLK, $\overline{CS}$, and DIN) have an operating range of 0 V to V_A. They are not prone to latch-up and may be asserted before the digital supply (V_D) without any risk. The digital output (DOUT) operating range is controlled by V_D. The output high voltage is V_D - 0.5V (min) while the output low voltage is 0.4V (max).

Applications Information

TYPICAL APPLICATION CIRCUIT

A typical application is shown in Figure 8. The split analog and digital supply pins are both powered in this example by the National LP2950 low-dropout voltage regulator. The analog supply is bypassed with a capacitor network located close to the ADC128S102. The digital supply is separated from the analog supply by an isolation resistor and bypassed with additional capacitors. The ADC128S102 uses the analog supply (V_A) as its reference voltage, so it is very important that V_A be kept as clean as possible. Due to the low power requirements of the ADC128S102, it is also possible to use a precision reference as a power supply.

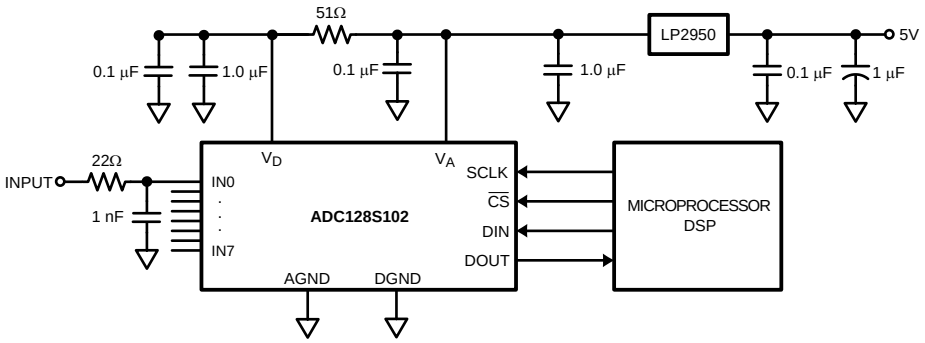


Figure 8. Typical Application Circuit

POWER SUPPLY CONSIDERATIONS

There are three major power supply concerns with this product: power supply sequencing, power management, and the effect of digital supply noise on the analog supply.

Power Supply Sequence

The ADC128S102 is a dual-supply device. The two supply pins share ESD resources, so care must be exercised to ensure that the power is applied in the correct sequence. To avoid turning on the ESD diodes, the digital supply (V_D) cannot exceed the analog supply (V_A) by more than 300 mV, during a conversion cycle. Therefore, V_A must ramp up before or concurrently with V_D.

Power Management

The ADC128S102 is fully powered-up whenever $\overline{CS}$ is low and fully powered-down whenever $\overline{CS}$ is high, with one exception. If operating in continuous conversion mode, the ADC128S102 automatically enters power-down mode between SCLK's 16th falling edge of a conversion and SCLK's 1st falling edge of the subsequent conversion (see Figure 1).

In continuous conversion mode, the ADC128S102 can perform multiple conversions back to back. Each conversion requires 16 SCLK cycles and the ADC128S102 will perform conversions continuously as long as $\overline{CS}$ is held low. Continuous mode offers maximum throughput.

In burst mode, the user may trade off throughput for power consumption by performing fewer conversions per unit time. This means spending more time in power-down mode and less time in normal mode. By utilizing this technique, the user can achieve very low sample rates while still utilizing an SCLK frequency within the electrical specifications. The Power Consumption vs. SCLK curve in the Typical Performance Curves section shows the typical power consumption of the ADC128S102. To calculate the power consumption (P_C), simply multiply the fraction of time spent in the normal mode (t_N) by the normal mode power consumption (P_N), and add the fraction of time spent in shutdown mode (t_S) multiplied by the shutdown mode power consumption (P_S) as shown in Figure 9.

$$P_C = \frac{t_N}{t_N + t_S} \times P_N + \frac{t_S}{t_N + t_S} \times P_S$$

Figure 9. Power Consumption Equation

Power Supply Noise Considerations

The charging of any output load capacitance requires current from the digital supply, V_D. The current pulses required from the supply to charge the output capacitance will cause voltage variations on the digital supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, if the analog and digital supplies are tied directly together, the noise on the digital supply will be coupled directly into the analog supply, causing greater performance degradation than would noise on the digital supply alone.

Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater the noise coupled into the analog channel.

The first solution to keeping digital noise out of the analog supply is to decouple the analog and digital supplies from each other or use separate supplies for them. To keep noise out of the digital supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100 Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve noise performance. Since the series resistor and the load capacitance form a low frequency pole, verify signal integrity once the series resistor has been added.

LAYOUT AND GROUNDING

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC128S102 due to supply noise, do not use the same supply for the ADC128S102 that is used for digital logic.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

We recommend the use of a single, uniform ground plane and the use of split power planes. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry and I/O lines should be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the analog ground plane at a single, quiet point.

Radiation Environments

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

TOTAL IONIZING DOSE

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the Ordering Information table on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883G, Test Method 1019.7. Testing is done according to Condition A and the “Extended room temperature anneal test” described in section 3.11 for application environment dose rates less than 0.16 rad(Si)/s. Wafer level TID data is available with lot shipments.

SINGLE EVENT LATCH-UP

One time single event latchup testing (SEL) was performed according to EIA/JEDEC Standard, EIA/JEDEC57. Testing was done at maximum operating temperature and supply voltage. The linear energy transfer threshold (LETth) shown in the Key Specifications table on the front page is the maximum LET tested. A test report is available upon request.

SINGLE EVENT UPSET

A report on single event upset (SEU) is available upon request.

Revision History

Date Released	Revision	Section	Changes
08/21/08	A	New Data Sheet, Initial Release	New product data sheet, Initial Release
11/03/08	B	Timing Diagrams	Typo, Changed Figure 2, tDIS lower left hand side changed to tDS and tDIH lower left hand side change to tDH. Revision A will be Archived.
01/09/09	C	Features, Ordering Information	Corrected package reference from 16-lead TSSOP to 16-lead Ceramic SOIC, Removed QV NSID reference and Added SMD Number to RQV NSID. Revision B will be Archived.
06/02/09	D	Features, Ordering Information, Electrical Section	Moved Rad information from Key Specifications to Features. Deleted ADC128S102WGMLS reference. Added Burn In Delta Table. Revision C will be Archived.
10/27/09	E	Operating Ratings, Electricals, Note and Typical Performance Characteristics	Spec Typo for Clock Frequency range, Electrical headings, currently shows 8 Mhz to 16 Mhz, Should be 0.8 Mhz and 16 Mhz. Reword Note 10. Reformatted Burn In Delta table. Added new ENOB vs SCLK Plot. Revision D will be Archived.
03/11/2010	F	AC Electrical Characteristics - SCLK Duty Cycle	AC Electrical Characteristics - SCLK Duty Cycle, typ limits. Revision E will be Archived.
01/13/2011	G	Electrical Characteristics	Removed reference to Ta Min & Ta Max under titled sections.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962R0722701VZA	ACTIVE	CLGA	NAC	16	42	TBD	Call TI	Level-1-NA-UNLIM	
ADC128S102WGRQV	ACTIVE	CLGA	NAC	16	42	TBD	Call TI	Level-1-NA-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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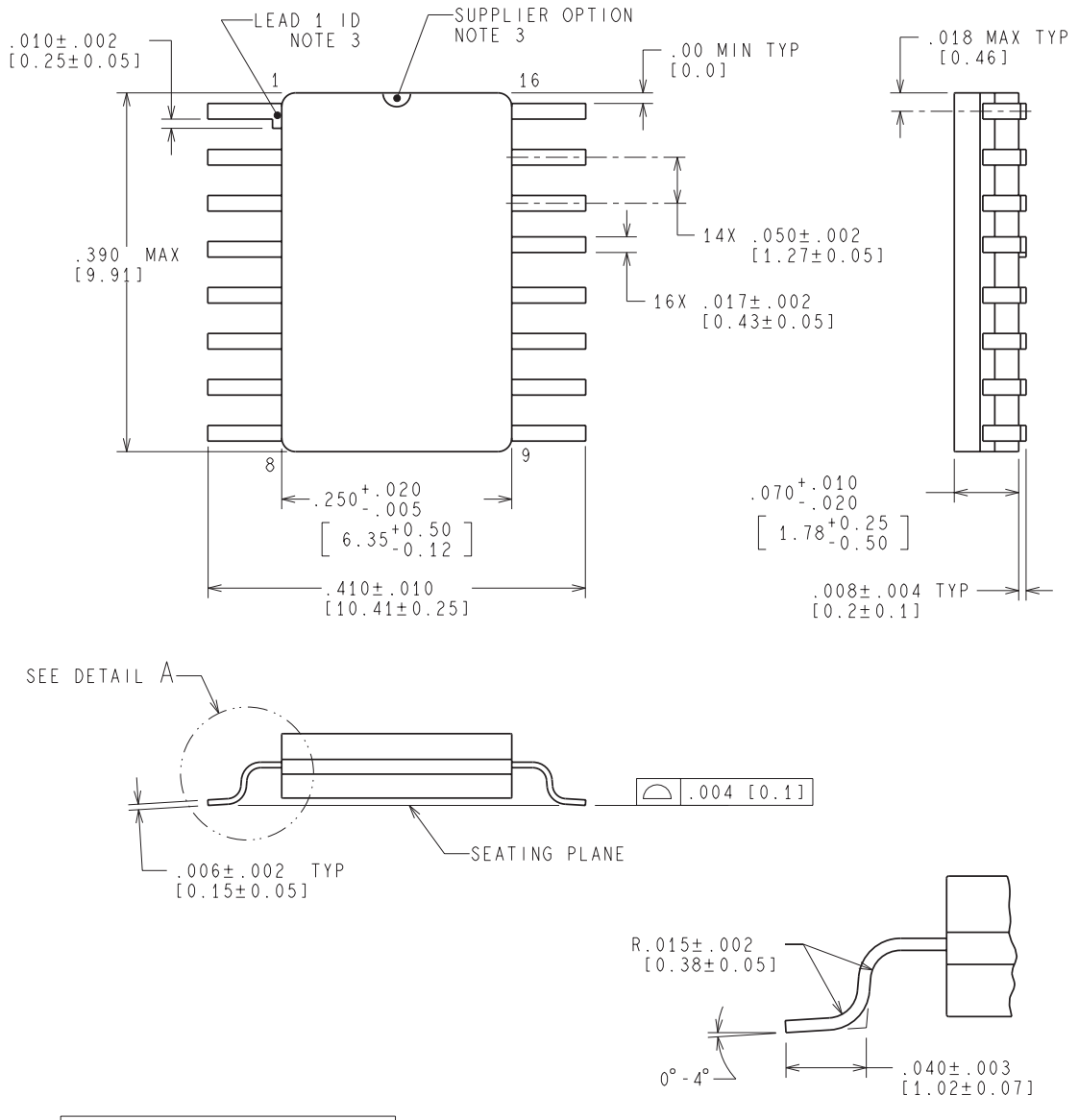
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.070 +.010 -.020
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.008±.004 TYP
[0.2±0.1]
SEE DETAIL A
.004 [0.1]
SEATING PLANE
.006±.002 TYP
[0.15±0.05]
R.015±.002
[0.38±0.05]
0°-4°
.040±.003
[1.02±0.07]
MIL-PRF-38535
CONFIGURATION CONTROL
DETAIL A
TYPICAL
WG16A (RevG)

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