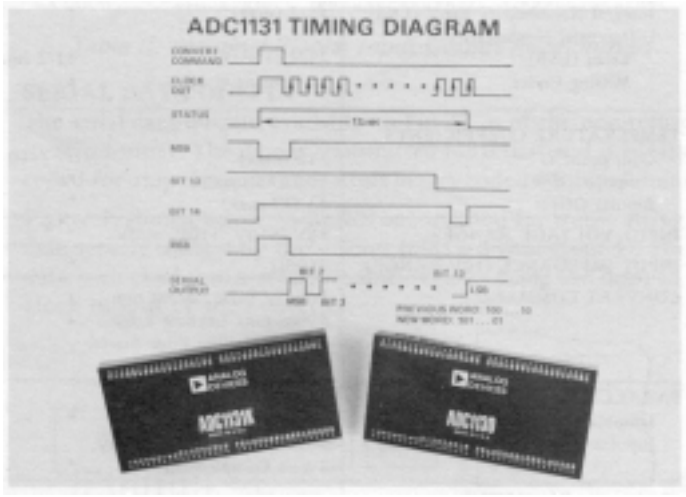
14-Bit High Speed Analog to Digital Converter

Models ADC1130, ADC1131

FEATURES
14-BIT Resolution and Accuracy
Fast 12μs Conversion Time (ADC1131J/K)
Low 10ppm/°C Maximum Gain TC
User Choice of Input Range
No Missing Codes

APPLICATIONS
Wide Band Data Digitizing Multi-Channel Computer Interface High Accuracy Data Acquisition X-Ray Tomography Nuclear Accelerator Instrumentation



GENERAL DESCRIPTION

The ADC11130 and ADCI 131 are high speed analog-to-digital converters packaged in a small 2" x 4" x 0.4" (51 x 102 x 10mm) module, which perform complete 14-bit conversions in 25μs and 12μs respectively. Using the successive approximations technique, they convert analog input voltages into natural binary, offset binary, or two's complement coded outputs. Data outputs are provided in both parallel and non-return-to-zero serial form.

Four analog input ranges are available: 0V to +20V, 0V to +10V, ±10V, and ±5V. The user selects the desired range by making appropriate connections to the module terminals. The ADC1130 and ADC1131 can also be connected so as to perform conversions of less than 14 bit resolution with a proportionate decrease in conversion time.

TIMING

As shown in Figure 1, the leading edge of the convert command set the MSB output to Logic "0" and the CLOCK OUT, STATUS, MSB, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the convert command returns to Logic "0", at which time the clock starts to run and the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic 0" and another comparison is made. This process continues through ach successive bit until the BIT 14 (LSB) comparison is completed.

At this point the STATUS and CLOCK OUT return to Logic "0" and the conversion cycle ends.

The serial data output is of the non-return-to-zero (NRZ) format. The data is available, MSB first, 20ns after each of the fourteen "0" to "1" clock transitions.

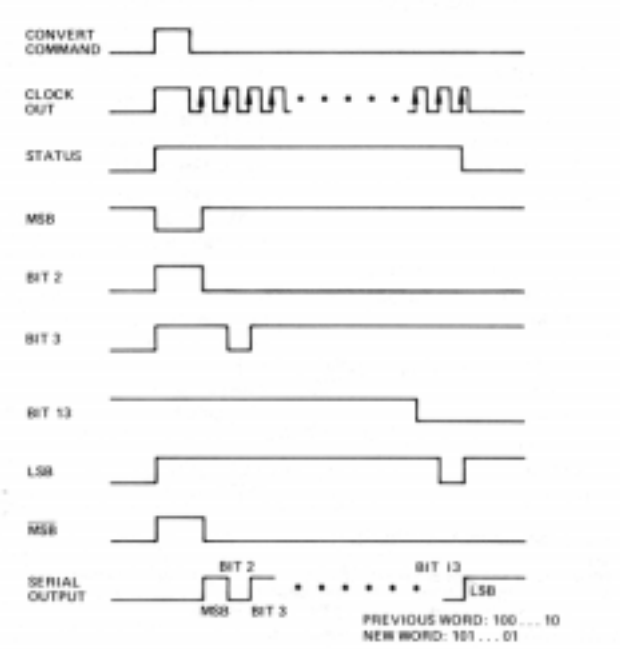


Figure 1. Timing Diagram

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