ADC1001

ADC1001 10-Bit µP Compatible A/D Converter

Literature Number: SNAS536

National Semiconductor

June 1999

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10-Bit µP Compatible A/D Converter

General Description

The ADC1001 is a CMOS, 10-bit successive approximation A/D converter. The 20-pin ADC1001 is pin compatible with the ADC0801 8-bit A/D family. The 10-bit data word is read in two 8-bit bytes, formatted left justified and high byte first. The six least significant bits of the second byte are set to zero, as is proper for a 16-bit word.

Differential inputs provide low frequency input common mode rejection and allow offsetting the analog range of the converter. In addition, the reference input can be adjusted enabling the conversion of reduced analog ranges with 10-bit resolution.

Key Specifications

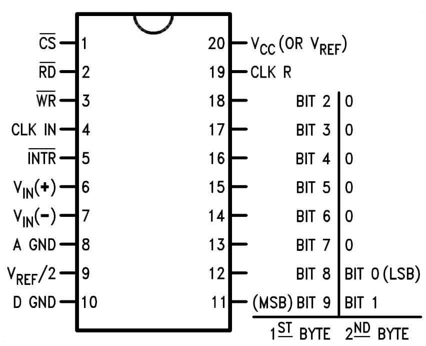
- Resolution: 10 bits
- Linearity error: ±1 LSB
- Conversion time: 200µS

Features

- ADC1001 is pin compatible with ADC0801 series 8-bit A/D converters
- Compatible with NSC800 and 8080 µP derivatives — no interfacing logic needed
- Easily interfaced to 6800 µP derivatives
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference
- 0.3" standard width 20-pin DIP package

Connection Diagram

ADC1001
Dual-In-Line Package



Top View

Ordering Information

Temperature Range	0˚C to +70˚C	−40˚C to +85˚C
Order Number	ADC1001CCJ-1	ADC1001CCJ
Package Outline	J20A	J20A

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Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Logic Control Inputs	−0.3V to +18V
Voltage at Other Inputs and Outputs	−0.3V to (V_{CC}+0.3V)
Storage Temperature Range	−65˚C to +150˚C
Package Dissipation at T_A=25˚C	875 mW
Lead Temp. (Soldering, 10 seconds)	300˚C
ESD Susceptibility (Note 10)	800V

Operating Conditions (Notes 1, 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC1001CCJ	−40˚C≤T_A≤+85˚C
ADC1001CCJ-1	0˚C≤T_A≤+70˚C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Converter Characteristics

Converter Specifications: V_{CC}=5 V_{DC}, V_{REF}/2=2.500 V_{DC}, $T_{MIN} \leq T_A \leq T_{MAX}$ and f_{CLK}=410 kHz unless otherwise specified.

Parameter	Conditions	MIn	Typ	Max	Units
Linearity Error				±1	LSB
Zero Error				±2	LSB
Full-Scale Error				±2	LSB
Total Ladder Resistance (Note 9)	Input Resistance at Pin 9	2.2	4.8		KΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±⅛		LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC}±5% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±⅛		LSB

AC Electrical Characteristics

Timing Specifications: V_{CC}=5 $V_{DC}$and T_A=25˚C unless otherwise specified.

Symbol	Parameter	Conditions	MIn	Typ	Max	Units
T_c	Conversion Time	(Note 5)	80		90	1/f_{CLK}
		f_{CLK}=410 kHz	195		220	µs
f_{CLK}	Clock Frequency	(Note 8)	100		1260	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ =0 V_{DC}, f_{CLK}=410 kHz			4600	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ =0 V_{DC} (Note 6)	150			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		170	300	ns
t_{1H}, t_{0H}	TRI-STATE® Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
t_{1rs}	$\overline{INTR}$ to 1st Read Set-Up Time		550	400		ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

DC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and T_{MIN}≤T_A≤ T_{MAX}, unless otherwise specified.

Symbol	Parameter	Conditions	MIn	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical “1” Input Voltage (Except CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical “0” Input Voltage (Except CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical “1” Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical “0” input Current (All Inputs)	V_{IN}=0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN						
V_T+	CLK IN Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T−	CLK IN Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN Hysteresis (V_T+)−(V_T−)		0.6	1.3	2.0	V_{DC}
OUTPUTS AND $\overline{INTR}$						
V_{OUT}(0)	Logical “0” Output Voltage	I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT}(1)	Logical “1” Output Voltage	I_O=−360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
		I_O=−10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0.4 V_{DC}		0.1	−100	μA_{DC}
		V_{OUT}=5 V_{DC}		0.1	3	μA_{DC}
I_{SOURCE}		V_{OUT} Short to GND, T_A=25˚C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25˚C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	f_{CLK}=410 kHz, V_{REF}/2=NC, T_A=25˚C and $\overline{CS}$ =1		2.5	5.0	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified. The separate A GND point should always be wired to the D GND.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For V_{IN}(−)≥ V_{IN}(+) the digital output code will be all zeros. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near fullscale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 3* .

Note 6: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see Timing Diagrams).

Note 7: All typical values are for T_A=25˚C.

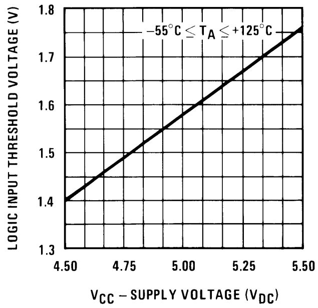
Note 8: Accuracy is guaranteed at f_{CLK}=410 kHz. At higher clock frequencies accuracy can degrade.

Note 9: The $V_{REF/2}$ pin is the center point of a two resistor divider (each resistor is 2.4kΩ) connected from V_{CC} to ground. Total ladder input resistance is the sum of these two equal resistors.

Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

Logic Input Threshold Voltage vs Supply Voltage



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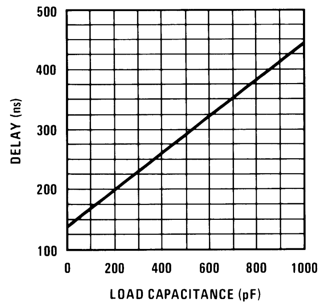
Delay From Falling Edge of RD to Output Data Valid vs Load Capacitance



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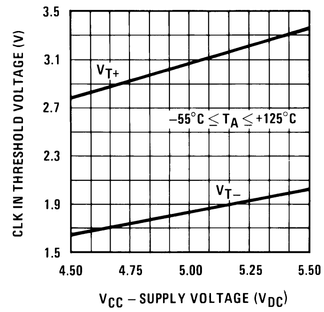
CLK IN Schmitt Trip Levels vs Supply Voltage



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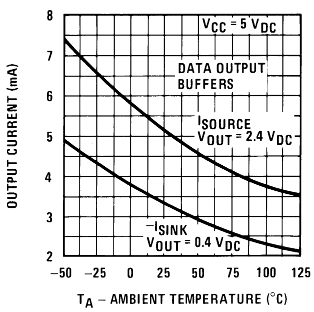
Output Current vs Temperature



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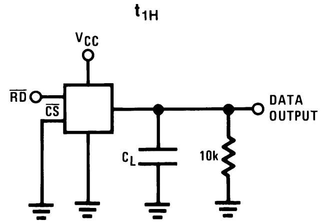
TRI-STATE Test Circuits and Waveforms

t_{1H}



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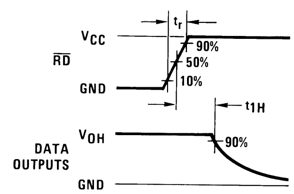
t_{1H}, C_L=10 pF



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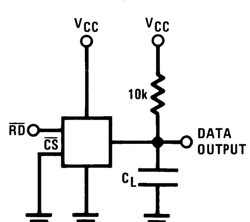
t_r=20 ns

t_{0H}



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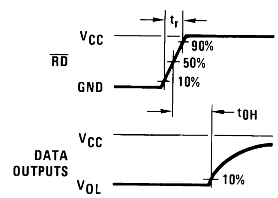
t_{0H}, C_L=10 pF



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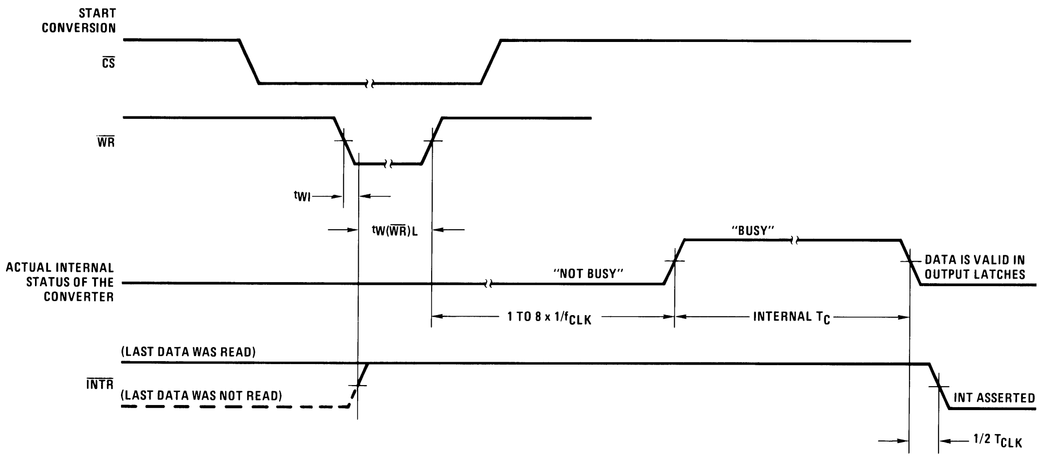
t_r=20 ns

TRI-STATE Test Circuits and Waveforms (Continued)

Timing Diagrams



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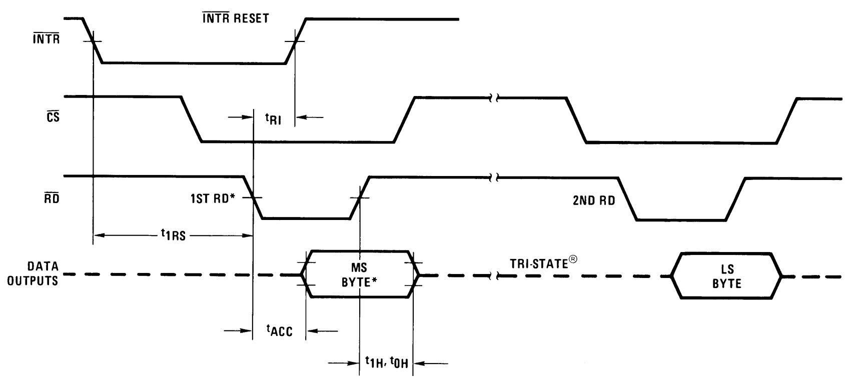
Output Enable and Reset $\overline{INTR}$



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*All timing is measured from the 50% voltage points.

Timing Diagrams (Continued)

Byte Sequencing For The 20-Pin ADC1001

Byte Order	8-Bit Data Bus Connection							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1st	MSB Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
2nd	Bit 1	LSB Bit 0	0	0	0	0	0	0

Functional Description

The ADC1001 uses an advanced potentiometric resistive ladder network. The analog inputs, as well as the taps of this ladder network, are switched into a weighted capacitor array. The output of this capacitor array is the input to a sampled data comparator. This comparator allows the successive approximation logic to match the analog difference input voltage [$V_{IN}(+)-V_{IN}(-)$] to taps on the R network. The most significant bit is tested first and after 10 comparisons (80 clock cycles) a digital 10-bit binary code (all "1"s=full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ =0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion in process can be interrupted by issuing a second start command.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 3*. All of the inputs and outputs are shown and the major logic control paths are drawn in heavier weight lines.

The conversion is initialized by taking $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 10-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 10-bit shift register then can have the "1" clocked in, which allows the conversion process to continue. If the set signal were to still be present, this reset pulse would have no effect and the 10-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

After the "1" is clocked through the 10-bit shift register (which completes the SAR search) it causes the new digital word to transfer to the TRI-STATE output latches. When this XFER signal makes a high-to-low transition the one shot fires, setting the INTR F/F. An inverting buffer then supplies the $\overline{INTR}$ output signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for aproximately 400 ns. If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of the conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal.

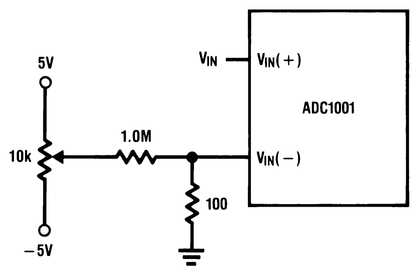
When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled.

Zero and Full-Scale Adjustment

Zero error can be adjusted as shown in *Figure 1*. $V_{IN}(+)$ is forced to +2.5 mV (+½ LSB) and the potentiometer is adjusted until the digital output code changes from 00 0000 0000 to 00 0000 0001.

Full-scale is adjusted as shown in *Figure 2*, with the $V_{REF}/2$ input. With V_{IN} (+) forced to the desired full-scale voltage less 1½ LSBs (V_{FS}−1½ LSBs), $V_{REF}/2$ is adjusted until the digital output code changes from 11 1111 1110 to 11 1111 1111.

Functional Description (Continued)



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Note 11: $V_{IN}(-)$ should be biased so that $V_{IN}(-) \geq -0.05V$ when potentiometer wiper is set at most negative voltage position.

FIGURE 1. Zero Adjust Circuit

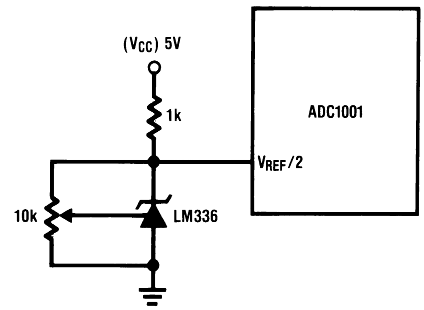

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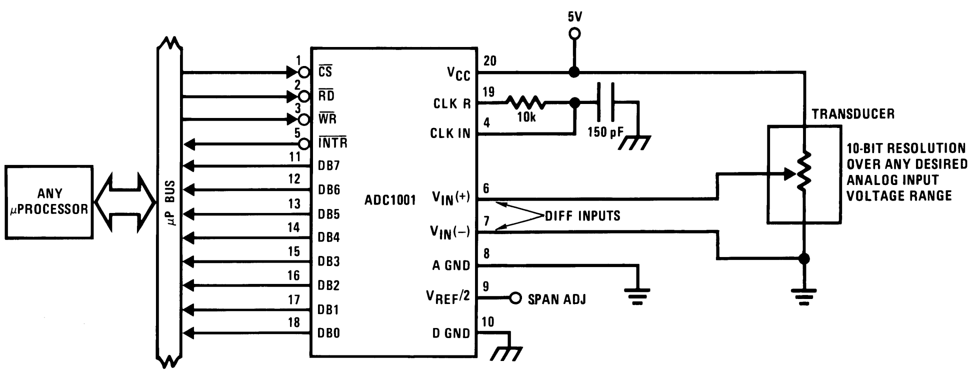
FIGURE 2. Full-Scale Adjust

Typical Application



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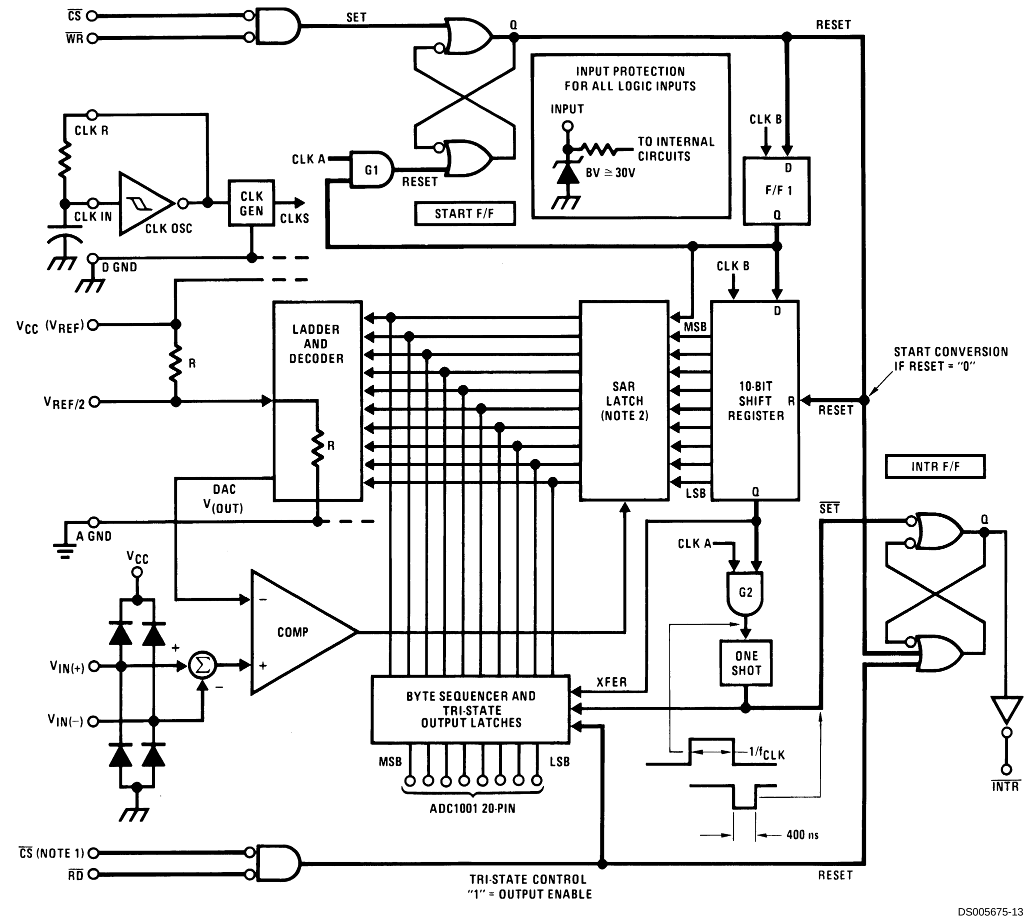
Block Diagram

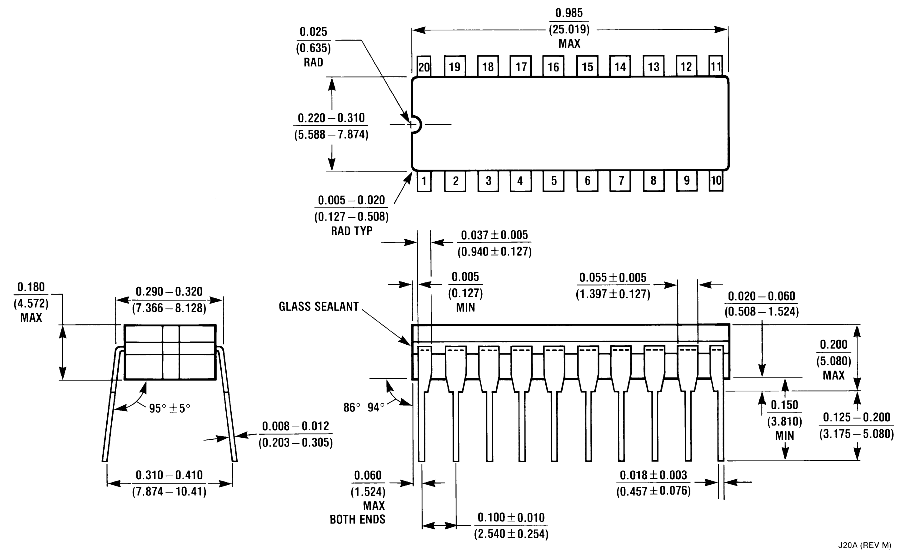


Note 12: $\overline{CS}$ shown twice for clarity.

Note 13: SAR= Successive Approximation Register.

FIGURE 3.

Physical Dimensions inches (millimeters) unless otherwise noted



Cavity Dual-In-Line Package (J) (Side Brazed)
Order Number ADC1001CCJ or ADC1001CCJ-1
NS Package Number J20A

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