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# Broadband Modem Mixed Signal Front End

## Preliminary Technical Data AD9875 / AD9876

**FEATURES**

**Low Cost 3.3V-CMOS Mixed Signal Front End Converter for Broadband Modems**
**10/12-Bit Direct IF D/A Converter (TxDAC+™)**
- **64 / 32 MSPS Input Word Rate**
- **2 x / 4 x Interpolation LP- or BP- Transmit Filter**
- **128 MSPS DAC Output Update Rate**
- **26 MHz Transmit Bandwidth**
- **Power Down Modes**

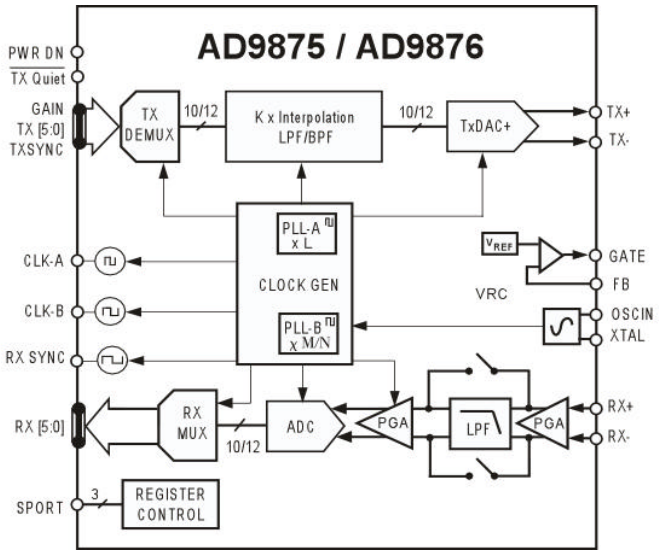
**10/12-Bit, 50 MSPS Direct IF A/D Converter**
- **4th Order Low Pass Filter 12 or 29 MHz with Bypass**
- **-6dB to 36dB Programmable Gain Amplifier**

**Internal 4 x Clock Multiplier (PLL)**
**Clock Outputs**
**Voltage Regulator Controller**
**48-Lead LQFP Package**

**APPLICATIONS**

**Powerline Networking**
**Home Phone Networking**
**xDSL**
**Broadband Wireless**
**Home RF**

**FUNCTIONAL BLOCK DIAGRAM**




**PRODUCT DESCRIPTION**

The AD9875/76 are single supply broadband modem mixed signal front end ICs. They contain the transmit path Interpolation Filter and DAC, and the receive path PGA, LPF and ADC required for a variety of broadband modem applications. Also on-chip is a PLL clock multiplier which provides all required clocks from a single crystal or clock input. The AD9875/76 provide 10 bit and 12 bit converter performance respectively

The TxDAC+™ uses a digital 2- or 4-times interpolation low pass or band pass filter to further oversample transmit data and ease the complexity of analog reconstruction filtering. Full-scale waveforms with bandwidths as high as 15 MHz can be reconstructed while operating at an input data rate of 32 MSPS. The 10/12-bit DAC provides differential current outputs. The DAC full-scale current can be adjusted from 2 mA to 20 mA by a single resistor, providing 20 dB of additional gain range.

The receive path consists of a PGA, LPF and ADC. The two-stage PGA has a gain range of -6dB to +36dB, and is programmable in 2 dB steps. This adds 42 dB of dynamic range to the receive path. The receive path LPF cut off frequency can be programmed to either 12 MHz or 29 MHz. The filter cutoff frequency can also be tuned or bypassed where filter requirements differ. The 10/12-bit ADC uses a multistage differential pipeline architecture to achieve excellent dynamic performance with low power consumption.

The AD9875/6 provides a voltage regulator controller (VRC) that can be used with an external power MOSFET transistor to form a cost effective 1.3V linear regulator.

The digital transmit and receive ports are each multiplexed to a bus width of 5/6 bits and are clocked at a frequency of twice the 10/12-bit word rate.

AD9875/6's ADC and/or DAC can also be used at higher sampling rates in a 5/6-bit resolution non-multiplexed mode.

The AD9875 and AD9876 are pin compatible devices, which are available in a space-saving 48-lead LQFP package. They are specified over the commercial (-40ºC to +85ºC) temperature range.



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# AD9875 / AD9876 – SPECIFICATIONS

($V_S$ = +3.3V ± 10, $f_{OSCIN}$=32 MHz, $f_{SYSCLK}$ = 128 MHz, $R_{SET}$ = 10 kΩ, 100 Ω DAC Load)

| PARAMETER | Temp | Test Level | AD9875/6 Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| OSC IN CHARACTERISTICS | | | | | | |
| Frequency Range | FULL | I | 10 | | 50 | MHz |
| Duty Cycle | +25°C | II | 45 | 50 | 55 | % |
| Input Capacitance | +25°C | III | | 3 | | pF |
| Input Impedance | +25°C | III | | 100 | | MΩ |
| CLOCK OUTPUT CHARACTERISTICS | | | | | | |
| CLKA Jitter ($f_{CLKA}$ Derived from PLL) | +25°C | II | | 14 | | ps rms |
| CLKA Duty cycle | +25°C | III | | ±5 | | % |
| CLKB Jitter ($f_{CLKB}$ Derived from PLL) | +25°C | II | | 33 | | ps rms |
| CLKB Duty cycle | +25°C | III | | ±5 | | % |
| TX-CHARACTERISTICS | | | | | | |
| TX-Path Latency | n.a. | n.a. | | 82 | | $f_{SYSLK}$ Cycles |
| Interpolation Filter Bandwidth (-0.1dB) | | | | | | |
| 4 x Interpolation, LPF | FULL | III | | 13 | | MHz |
| 2 x Interpolation, LPF | FULL | III | | 26 | | MHz |
| TX-DAC | | | | | | |
| Resolution, AD9875 | n.a. | n.a. | | 10 | | Bits |
| Resolution, AD9876 | n.a. | n.a. | | 12 | | Bits |
| Conversion Rate | FULL | II | 10 | | 128 | MHz |
| Full-Scale Output Current | FULL | II | 2 | 4 | 20 | mA |
| Gain Error | +25°C | II | -10 | ±2 | +10 | %FS |
| Output Offset | +25°C | II | 0 | 2 | 10 | µA |
| Differential Nonlinearity | +25°C | III | | 0.5 | | LSB |
| Integral Nonlinearity | +25°C | II | | | 1 | LSB |
| Output Capacitance | +25°C | III | | 5 | | pF |
| Phase Noise @ 1kHz Offset, 10 MHz Signal | | | | | | |
| OSC IN Multiplier Enabled at 4× | +25°C | III | | -85 | | dBc/Hz |
| Multiplier Disabled | +25°C | III | | -110 | | dBc/Hz |
| Voltage Compliance Range | FULL | II | -0.5 | | 1.5 | V |
| Signal-to-Noise and Distortion Ratio (SINAD) | | | | | | |
| 10 MHz Analog Out AD9875 (20MHz BW) | +25°C | II | | tbd | | dB |
| Signal-to-Noise Ratio and Distortion (SINAD) | | | | | | |
| 10 MHz Analog Out AD9876 (20MHz BW) | +25°C | II | | tbd | | dB |
| Wideband SFDR (to Nyquist, 64MHz max.) | +25°C | III | | | | |
| 5 MHZ Analog Out | +25°C | III | | 70 | | dBc |
| 10 MHz Analog Out | +25°C | III | | tbd | | dBc |
| Narrowband SFDR (3MHz Window): | | | | | | |
| 10 MHz Analog Out | +25°C | III | | 75 | | dBc |
| IP3 | +25°C | III | | 30 | | dBm |
| Common Mode Rejection | +25°C | III | | 40 | | dB |
| 10-BIT ADC CHARACTERISTICS (AD9875) | | | | | | |
| Resolution | n.a. | n.a. | | 10 | | Bits |
| Conversion Rate | FULL | II | 7.5 | | 55 | MHz |
| Pipeline Delay, ADC Clock Cycles | n.a. | n.a. | | 5.5 | | Cycles |
| DC Accuracy | | | | | | |
| Differential Nonlinearity | +25°C | III | | ±0.25 | | LSB |
| Integral Nonlinearity | +25°C | III | | ±0.5 | | LSB |
| Offset Error | +25°C | III | | ±0.5 | | % FSR |
| Gain Error | +25°C | III | | ±3 | | % FSR |
| Dynamic Performance (Ain=-0.5dB FS, f=10MHz) @ $f_{oscin}$=32 MHz | | | | | | |
| Signal-to-Noise and Distortion Ratio (SINAD) | FULL | I | tbd | 58 | | dB |
| Effective Number of Bits (ENOB) | FULL | I | tbd | 9.3 | | Bits |
| Signal-to-Noise Ratio (SNR) | FULL | I | tbd | 59 | | dB |
| Total Harmonic Distortion (THD) | FULL | I | | -72.0 | -tbd | dB |

($V_S$ = +3.3V ± 10, $f_{OSCIN}$=32 MHz, $f_{SYSCLK}$ = 128 MHz, $R_{SET}$ = 10 k**W**, 100 **W** DAC Load)



| PARAMETER | Temp | Test Level | AD9875/6 Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Spurious Free Dynamic Range (SFDR) | FULL | I | tbd | 74 | | dB |
| Differential Phase | +25°C | III | | < 0.1 | | Degree |
| Differential Gain | +25°C | III | | < 1 | | LSB |
| Dynamic Performance (Ain=-0.5dB FS, f=10MHz) | | | | | | |
| @ $f_{oscin}$=50 MHz | | | | | | |
| Signal-to-Noise and Distortion Ratio (SINAD) | FULL | III | | 58 | | dB |
| Effective Number of Bits (ENOB) | FULL | III | | 9.3 | | Bits |
| Signal-to-Noise Ratio (SNR) | FULL | III | | 59 | | dB |
| Total Harmonic Distortion (THD) | FULL | III | | -67 | | dB |
| Spurious Free Dynamic Range (SFDR) | FULL | III | | 68 | | dB |
| Differential Phase | +25°C | III | | < 0.1 | | Degree |
| Differential Gain | +25°C | III | | < 1 | | LSB |
| 12-BIT ADC CHARACTERISTICS (AD9876) | | | | | | |
| Resolution | n.a. | n.a. | | 12 | | Bits |
| Conversion Rate, 12 bit Mode | FULL | II | 7.5 | | 55 | MHz |
| Conversion Rate, 6 bit Mode | FULL | II | 7.5 | | 64 | MHz |
| Pipeline Delay, ADC Clock Cycles | n.a. | n.a. | | 5.5 | | Cycles |
| DC Accuracy | | | | | | |
| Differential Nonlinearity | +25°C | III | | ±0.75 | | LSB |
| Integral Nonlinearity | +25°C | III | | ±1.5 | | LSB |
| Offset Error | +25°C | III | | ±1 | | % FSR |
| Gain Error | +25°C | III | | ±2 | | % FSR |
| Dynamic Performance (Ain=-0.5dB FS, f= 10 MHz) | | | | | | |
| @ $f_{oscin}$=32 MHz | | | | | | |
| Signal-to-Noise and Distortion Ratio (SINAD) | FULL | I | tbd | 59 | | dB |
| Effective Number of Bits (ENOB) | FULL | I | tbd | 10.1 | | Bits |
| Signal-to-Noise Ratio (SNR) | FULL | I | tbd | 62 | | dB |
| Total Harmonic Distortion (THD) | FULL | I | | -62 | tbd | dB |
| Spurious Free Dynamic Range (SFDR) | FULL | I | tbd | 63 | | dB |
| Differential Phase | +25°C | III | | < 0.1 | | Degree |
| Differential Gain | +25°C | III | | < 1 | | LSB |
| Dynamic Performance (Ain=-0.5dB FS, f=10MHz) | | | | | | |
| @ $f_{oscin}$=50 MHz | | | | | | |
| Signal-to-Noise and Distortion Ratio (SINAD) | FULL | III | | 59 | | dB |
| Effective Number of Bits (ENOB) | FULL | III | | 10.1 | | Bits |
| Signal-to-Noise Ratio (SNR) | FULL | III | | 62 | | dB |
| Total Harmonic Distortion (THD) | FULL | III | | -62 | | dB |
| Spurious Free Dynamic Range (SFDR) | FULL | III | | 63 | | dB |
| Differential Phase | +25°C | III | | < 0.1 | | Degree |
| Differential Gain | +25°C | III | | < 1 | | LSB |
| PROGRAMMABLE GAIN AMPLIFIER | | | | | | |
| Programmable Gain Range (12 MHz Filter) | +25°C | I | -6 | | 36 | dB |
| Programmable Gain Range (26 MHz Filter) | +25°C | I | -6 | | 30 | dB |
| Gain Step Size | +25°C | I | | 2 | | dB |
| Gain Step Accuracy | +25°C | II | | 0.25 | | dB |
| Passband | FULL | II | 0 | | 30 | MHz |
| Output Settling to 1% FS (Gain Change Ripple) at Min. to Max. Gain Change | | | | 0.5 | | µs |
| Gain Error | FULL | II | | tbd | | % |
| Offset Error | FULL | II | | tbd | | % |
| ANALOG INPUT | | | | | | |
| Input Voltage Range | FULL | III | | 4 | | Vppd |
| Input Capacitance | +25°C | III | | 4 | | pF |
| Differential Input Resistance | +25°C | III | | 270 | | Ohm |

# AD9875 / AD9876 – SPECIFICATIONS

($V_S$ = +3.3V ± 10, $f_{OSCIN}$=32 MHz, $f_{SYSCLK}$ = 128 MHz, $R_{SET}$ = 10 kΩ, 100 Ω DAC Load)

| PARAMETER | Temp | Test Level | AD9875/6 Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Bandwidth (-3dB) | +25°C | III | | 50 | | MHz |
| Input referred Noise (at 36 dB gain with filter) | +25°C | III | | 16 | | µV rms |
| Input referred Noise (at -6 dB gain with filter) | +25°C | III | | 684 | | µV rms |
| Common Mode Rejection | +25°C | III | | 40 | | dB |
| ANALOG LOW PASS FILTER Low cutoff | | | | | | |
| Cut-off Frequency | FULL | III | | 12 | | MHz |
| Cut-off Frequency Variation | FULL | III | | ±5 | | % |
| Attenuation @ 22 MHz | FULL | III | | 20 | | dB |
| Passband Ripple | FULL | II | | ±1.0 | tbd | dB |
| Group Delay Ripple | FULL | II | | ±50 | tbd | ns |
| Calibration Glitch | FULL | II | | 4 | tbd | mV |
| Offset Glitch 24 CLK2 Cycles after Cal. | FULL | II | | ±16 | tbd | mV |
| Total Harmonic Distortion at max. Gain (THD) | FULL | I | | -80 | | dB |
| ANALOG LOW PASS FILTER High cutoff | | | | | | |
| Cut-off Frequency | FULL | III | | 29 | | MHz |
| Cut-off Frequency Variation | FULL | III | | ±7 | | % |
| Attenuation @ 35 MHz | FULL | III | | 20 | | dB |
| Passband Ripple | FULL | II | | ±1.2 | tbd | dB |
| Group Delay Ripple | FULL | II | | ±30 | tbd | ns |
| Calibration Glitch | FULL | II | | 4 | tbd | mV |
| Offset Glitch 24 CLK2 Cycles after Cal. | FULL | II | | ±16 | tbd | mV |
| Total Harmonic Distortion at max. Gain (THD) | FULL | I | | -65 | | dB |
| OVERALL RX CHARACTERISTIC | | | | | | |
| Combined ADC Input noise (Filter and PGA) at maximum PGA Gain setting | FULL | III | | 507 | | µV |
| IP3 at 0dB Gain (12.5 MHz Filter) | FULL | III | | -tbd | | dBm |
| IP3 at 36 dB Gain (12.5 MHz Filter) | FULL | III | | -tbd | | dBm |
| IP3 at 0dB Gain (26 MHz Filter) | FULL | III | | tbd | | dBm |
| IP3 at 30 dB Gain (26 MHz Filter) | FULL | III | | tbd | | dBm |
| TIMING CHARACTERISTICS (20pF Load) | | | | | | |
| Power Down Mode | | | | | | |
| DAC Iout off after TX QUIET asserted | +25°C | II | | | 200 | ns |
| DAC active to DAC Power Down | +25°C | II | | | 200+delay | ns |
| PLL active to PLL Power Down | +25°C | II | | | 1+delay | µs |
| ADC active to ADC Power Down | +25°C | II | | | 1+delay | µs |
| PGA active to PGA Power Down | +25°C | II | | | 1+delay | µs |
| LPF active to LPF Power Down | +25°C | II | | | 1+delay | µs |
| Interpolator active to Interpolator Power Down delay | +25°C | II | | | delay | µs |
| VRC active to VRC Power Down | +25°C | II | | | tbd | µs |
| Low Power Mode enable time | +25°C | II | | | tbd | µs |
| DAC Iout on after TX QUIET deasserted | +25°C | II | | | 1 | µs |
| DAC Power Down to DAC active | +25°C | II | | | 40+delay | µs |
| PLL Power Down to PLL active | +25°C | II | | | 10+delay | µs |
| ADC Power Down to ADC active | +25°C | II | | | 1000+delay | µs |
| PGA Power Down to PGA active | +25°C | II | | | 1+delay | µs |
| LPF Power Down to LPF active | +25°C | II | | | 1+delay | µs |
| Interpolator Power Down to Interpolator active delay | +25°C | II | | | delay | µs |
| VRC Power Down to VRC active | +25°C | II | | | tbd | µs |
| Low Power Mode disable time | +25°C | II | | | tbd | µs |
| Complete Power-Down to Full Operation | +25°C | II | | | 100 | µs |
| Wake-Up Time Low Power to Full Operation | +25°C | II | | | 200 | $t_{CLK2}$ Cycles |
| Minimum RESET Pulsewidth Low ($t_{RL}$) | FULL | III | | | 5 | $t_{CLK2}$ Cycles |
| Digital Output Rise-/Fall Time | +25°C | II | 2.8 | | 4 | ns |
| TX- /RX- Interface | | | | | | |
| Maximum Output Nibble rate | +25°C | I | 110 | | | MHz |

($V_S$ = +3.3V ± 10, $f_{OSCIN}$=32 MHz, $f_{SYSCLK}$ = 128 MHz, $R_{SET}$ = 10 k**W**, 100 **W** DAC Load)



| PARAMETER | Temp | Test Level | AD9875/6 Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Maximum Input Nibble Rate, 2x Interp. | +25°C | I | 128 | | | MHz |
| Set up time ($t_{su}$) | +25°C | II | 4 | | | ns |
| Hold time ($t_{hd}$) | +25°C | II | -1.5 | | | ns |
| RX-Data valid time($t_{vt}$) | +25°C | II | | | 3.0 | ns |
| RX-Data hold time ($t_{ht}$) | +25°C | II | 1.5 | | | ns |
| Serial Control Bus | | | | | | |
| Maximum SCLK Frequency ($f_{SCLK}$) | FULL | II | 25 | | | MHz |
| Clock Pulsewidth High ($t_{PWH}$) | FULL | II | 18 | | | ns |
| Clock Pulsewidth Low ($t_{PWL}$) | FULL | II | 18 | | | ns |
| Clock Rise/Fall Time | FULL | II | | | 1 | ms |
| Data/Chip-Select Setup Time ($t_{DS}$) | FULL | II | 25 | | | ns |
| Data Hold Time ($t_{DH}$) | FULL | II | 0 | | | ns |
| Data Valid Time ($t_{DV}$) | FULL | II | | | 20 | ns |
| CMOS LOGIC INPUTS | | | | | | |
| Logic "1" Voltage | +25°C | II | DRVDD -0.7 | | | V |
| Logic "0" Voltage | +25°C | II | | | 0.4 | V |
| Logic "1" Current | +25°C | II | | | 12 | µA |
| Logic "0" Current | +25°C | II | | | 12 | µA |
| Input Capacitance | +25°C | III | | 3 | | pF |
| CMOS LOGIC OUTPUTS (1mA Load) | | | | | | |
| Logic "1" Voltage | +25°C | I | DRVDD -0.6 | | | V |
| Logic "0" Voltage | +25°C | I | | | 0.4 | V |
| POWER SUPPLY | | | | | | |
| All Blocks Powered | | | | | | |
| Supply Current $I_S$ | +25°C | I | | 212 | tbd | mA |
| Supply Current $I_S$ TX QUIET Pin Asserted | +25°C | III | | 202 | | mA |
| Low Power Mode (wait for LAN wake-up) | | | | | | |
| Supply Current $I_S$ | +25°C | I | | 50 | tbd | mA |
| Power Down Mode | | | | | | |
| (Only Voltage Regulator Controller on) | | | | | | |
| Supply Current $I_S$ | +25°C | I | | 200 | tbd | µA |
| Power Consumption of Individual Blocks | | | | | | |
| Normal Mode: | | | | | | |
| DAC | +25°C | III | | 40 | | mA |
| Interpolator | +25°C | III | | 22 | | mA |
| PLL | +25°C | III | | 12 | | mA |
| ADC | +25°C | III | | 21 | | mA |
| PGA+Filter | +25°C | III | | 100 | | mA |
| Voltage Regulator Controller | +25°C | III | | 4 | | mA |
| Low Power Mode: | | | | | | |
| DAC | +25°C | III | | 0 | | mA |
| Interpolator | +25°C | III | | 0 | | mA |
| PLL | +25°C | III | | 12 | | mA |
| ADC | +25°C | III | | 12 | | mA |
| PGA+Filter | +25°C | III | | 21 | | mA |
| Voltage Regulator Controller | +25°C | III | | 200 | | µA |
| Power Supply Rejection | | | | | | |
| DAC | +25°C | III | | 0.04 | | %FSR |
| ADC | +25°C | III | | 0.04 | | %FSR |
| CHANNEL-TO-CHANNEL ISOLATION | | | | | | |
| TX DAC-to-ADC Isolation | | | | | | |
| (5MHz Analog Output) | | | | | | |
| Isolation between DAC and ADCs | +25°C | III | | 60 | | dB |
| Isolation between ADC and DAC | +25°C | III | | tbd | | dB |

NOTES
Specifications subject to change without notice.

# AD9875 / AD9876 – SPECIFICATIONS

($V_S$ = +3.3V ± 10, $f_{OSCIN}$=32 MHz, $f_{SYSCLK}$ = 128 MHz, $R_{SET}$ = 10 k**W**, 100 **W** DAC Load)

## ABSOLUTE MAXIMUM RATINGS*

Power Supply ($V_S$) ..... + 3.9 V
Digital Output Current ..... 5 mA
Digital Inputs ..... -0.3 V to DRVDD + 0.3V
Analog Inputs ..... -0.3V to AVDD +0.3V
Operating Temperature ..... -40ºC to+85 ºC
Maximum Junction Temperature ..... +150 ºC
Storage Temperature..... -65 ºC to 150 ºC
Lead Temperature (Solderring 10 sec) ..... +300 ºC

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

## EXPLANATION OF TEST LEVELS

I - Devices are 100% production tested at +25ºC and guaranteed by design and characterization testing for commercial operating temperature range (0ºC to 70ºC).

II - Parameter is guaranteed by design and /or characterization testing.

III- Parameter is a typical value only.

## ORDERING GUIDE

| Model | Temperature Range | Package Description |
|---|---|---|
| AD9875BST | -40ºC to +85ºC | 48-Lead LQFP |
| AD9876BST | -40ºC to +85ºC | 48-Lead LQFP |
| AD9875-EB | | AD9875 Eval. Board |
| AD9876-EB | | AD9875 Eval. Board |
| AD9875BSTRL | -40ºC to +85ºC | AD9875BST Reel |
| AD9876BSTRL | -40ºC to +85ºC | AD9876BST Reel |
| | | |

## THERMAL CHARACTERISTICS

**Thermal Resistance**

48-Lead LQFP
$\theta_{JA}$ = 91ºC/W
$\theta_{JC}$ = 28ºC/W

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9875/6 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## DEFINITIONS OF SPECIFICATIONS

### DIFFERENTIAL NONLINEARITY ERROR (DNL, NO MISSING CODES)

An ideal converter exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 10-bit resolution indicates that all 1024 codes respectively, must be present over all operating ranges.

### INTEGRAL NONLINEARITY ERROR (INL)

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

### PHASE NOISE

Single-sideband phase noise power density is specified relativ to the carrier (dBc/Hz) at a given frequency offset (1kHz) from the carrier. Phase noise can be measured directly on a generated single tone with a spectrum analyzer that supports noise marker measurements. It detects the relative power between the carrier and the offset (1kHz) sideband noise and takes the resolution bandwidth (rbw) into account by subtracting 10log(rbw). It also adds a correction factor that compensates for the implementation of the resolution bandwidth, log display and detector characteristic.

### OUTPUT COMPLIANCE RANGE

The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation, resulting in nonlinear performance or breakdown.

### SPURIOUS-FREE DYNAMIC RANGE (SFDR)

The difference, in dB, between the rms amplitude of the DACs output signal (or ADC's input signal) and the peak spurious signal over the specified bandwidth (Nyquist bandwidth unless otherwise noted).

### PIPELINE DELAY (LATENCY)

The number of clock cycles between conversion initiation and the associated output data being made available.

### OFFSET ERROR

First transition should occur for an analog value 1/2 LSB above negative full scale. Offset error is defined as the deviation of the actual transition from that point.

### GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

### INPUT REFERRRED NOISE

The rms output nosie is measured using histogram techniques. The ADC output codes' standard deviation is calculated in LSB, and converted to an equivalent voltage. This results in a noise figure that can directly be referred to the Rx input of the AD9875/6.

### SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding DC. The value for SINAD is expressed in decibels.

### EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$N = (SINAD - 1.76)\text{dB}/6.02$

it is possible to get a measure of performance expressed as $N$, the effective number of bits.

### SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

### TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

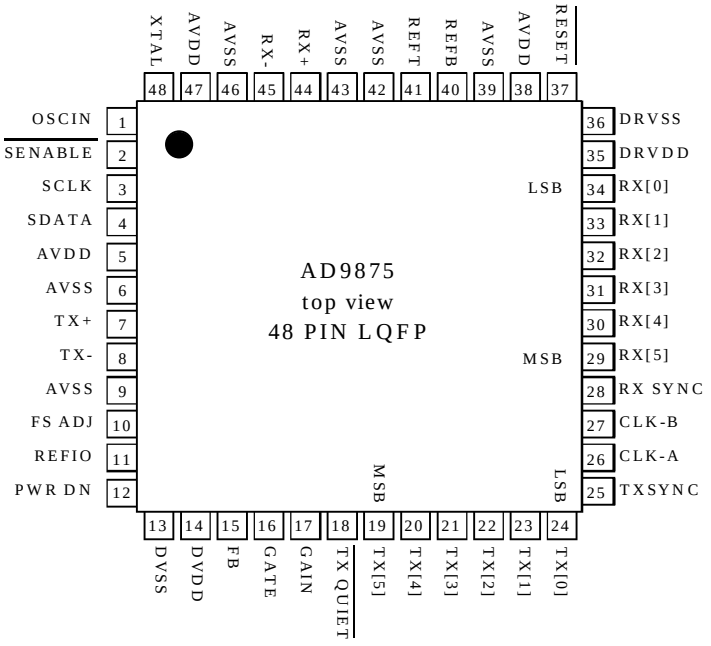
### POWER SUPPLY REJECTION

Power Supply Rejection specifies the converters maximum full-scale change when the supplies are varied from nominal to minimum and maximum specified voltages.

**PIN FUNCTION ASSIGNMENTS**

| PIN # | Pin Name | Pin Function |
|---|---|---|
| 1 | OSC IN | Crystal oscillator inverter Input |
| 2 | $\overline{\text{SENABLE}}$ | Serial Bus Enable Input |
| 3 | SCLK | Serial Bus Clock Input |
| 4 | SDATA | Serial Bus Data I/O |
| 5,38, 47 | AVDD | Analog +3.3V Power Supply |
| 6, 9, 39,42, 43,46 | AVSS | Analog Ground |
| 7 | TX+ | Transmit DAC + Output |
| 8 | TX- | Transmit DAC - Output |
| 10 | FS ADJ | DAC full-scale output current adjust with external resistor |
| 11 | REFIO | DAC bandgap decoupling node |
| 12 | PWR DN | Power Down Input |
| 13 | DVSS | Digital Ground |
| 14 | DVDD | Digital +3.3V Power Supply |
| 15 | FB | VCR Feedback Input |
| 16 | GATE | VCR Output to MOSFET Gate |

| PIN # | Pin Name | Pin Function |
|---|---|---|
| 17 | GAIN | Transmit Data Port (TX[5:0]) Mode Select Input |
| 18 | $\overline{\text{TX QUIET}}$ | Transmit Quiet Input |
| 19..24 | TX[5:0] | Transmit Data Input |
| 25 | TX SYNC | Transmit Synchronization Strobe Input |
| 26 | CLK-A | M x $f_{OSCIN}$ Clock Output |
| 27 | CLK-B | N x $f_{OSCIN}$ Clock Output |
| 28 | RX SYNC | Receive Data Synchronization Strobe Output |
| 29..34 | RX[5:0] | Receive Data Output |
| 35 | DRVDD | Digital I/O +3.3V Power Supply |
| 36 | DRVSS | Digital I/O Ground |
| 37 | $\overline{\text{RESET}}$ | Reset Input |
| 40 | REFB | ADC reference decoupling Node |
| 41 | REFT | ADC reference decoupling Node |
| 44 | RX+ | Receive Path + Input |
| 45 | RX- | Receive Path - Input |
| 48 | XTAL | Crystal oscillator inverter Output |



**AD9875 Register Layout**

| Address (hex) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default (hex) | Type |
|---|---|---|---|---|---|---|---|---|---|---|
| **00** | | LSB/MSB First | Software Reset | | | | | | 00 | rw |
| **01** | Power Down Regulator *at PWR DN Pin Low* | Power Down PLL-B *at PWR DN Pin Low* | Power Down PLL-A *at PWR DN Pin Low* | Power Down DAC *at PWR DN Pin Low* | Power Down Interpolators *at PWR DN Pin Low* | Power Down RX-Reference *at PWR DN Pin Low* | Power Down ADC& FVGA *at PWR DN Pin Low* | Power Down Receive Filter & CVGA *at PWR DN Pin Low* | 00 | rw |
| **02** | Power Down Regulator *at PWR DN Pin High* | Power Down PLL-B *at PWR DN Pin High* | Power Down PLL-A *at PWR DN Pin High* | Power Down DAC *at PWR DN Pin High* | Power Down Interpolators *at PWR DN Pin High* | Power Down RX-Reference *at PWR DN Pin High* | Power Down ADC& FVGA *at PWR DN Pin High* | Power Down Receive Filter & CVGA *at PWR DN Pin High* | 9F | rw |
| **03** | | ADC Clock Source | PLL-B ( x M ) Multiplier < 1:0 > | | PLL-B ( / N ) Divider < 1:0 > | | PLL-A Multiplier < 1:0 > | | 02 | rw |
| **04** | Receive- Filter Tuning Update Disable | Receive- Filter Tuning Update In Progress (read only) | Receiver Offset Correction | Receive- HP-Filter Bypass | Receiver Fast Sampling VGA Setting | Receive LP-Filter High Cutoff | Input Filter One Pole 16 MHz Enable | Receive LP-Filter Bypass | 01 | rw |
| **05** | RX-Filter Tuning Target < 7:0 > | | | | | | | | 40 | rw |
| **06** | | | VGA Gain Setting through Register | RX VGA Gain Control Register < 4:0 > | | | | | 00 | rw |
| **07** | TX- Interpolation Filter Setting < 3:0 > | | | | Power Down Interpolators *at TX QUIET Pin Low* | TX-Input LS Nibble First | TX-Input Port Width 5-bit (/ 6-bit) | TX-Input Multiplexer Bypass | 00 | rw |
| **08** | CLK B Output Invert | CLK A Output Invert | CLK B Output Disable | CLK A Output Disable | RX Tristate | RX-Output LS Nibble First | RX-Output Port Width 5-bit (/ 6-bit) | RX-Output Multipexer Bypass | 00 | rw |
| **0F** | | | | | Version < 3:0 > | | | | 00 | r |

**REGISTER BIT DEFINITIONS**

**00h, Bit 5 - Reset**

Writing a one to this bit resets the registers to their default values and restarts the chip. The Reset bit always reads back zero. Register address 00h bits are not cleared by this software reset. However, a low level at the RESET pin would force all registers including all bits in address 00h to their default state. The content of the interpolator stages is not cleared by software or hardware reset. It is recommended to "flush" the transmit path with zeros before transmitting data.

**00h, Bit 6 - LSB/MSB First**

Active high indicates serial port access of instruction byte and data registers is least significant bit (LSB) first. Default zero indicates most significant bit (MSB) first format.

**01h, 02h Bits 0 ... 7 - Power Down**

The PWR DN pin selects between two sets of individual programmable operation modes.

Sections of the chip that are not used can be put in a power saving mode when the corresponding bits of register 01h are set to one and PWR DN pin is low.

When PWR DN pin is high sections of the chip that are programmed to one in register 02h are in power saving mode.

Register 01h has a default value of 00h with all sections active while Register 02h has a default value of 9F with all sections but the PLLs powered down.

Bit 0: Power Down Receive Filter & CVGA powers down and bypasses the 4th order analog receive filter and coarse variable gain amplifier.

Bit 1: Power Down ADC & FVGA powers down the receive ADC and fine variable gain amplifier (FVGA). It stops the RX SYNC output clock.

Bit 2: Power Down RX Reference powers down the internal receive reference. This bit should be set if an external reference is applied.

Bit 3: Power Down Interpolators powers down the transmit digital interpolators. It doesn't clear the content of the datapath.

Bit 4: Power Down DAC powers down the transmit DAC.

Bit 5: Power Down PLL-A powers down the on chip clock multiplier and stops the CLK-A output (0V CLK-A output if set).

Bit 6: Power Down PLL-B powers down the on chip (x M / N) clock multiplier and stops the CLK-B output (0V CLK-B output if set).

Bit 7: Power Down Regulator powers down the on-chip (1.3V) voltage control regulator .

**03h Bits 0 ... 7 - PLL Settings**

The AD9875/6 integrates two independent programmable PLLs which generate the chip's internal and external clock signals from the Foscin frequency. PLL-A generates the DAC sampling, interpolator and CLK-A frequencies while PLL-B can be used to sample the ADC receive data path. CLK-B output is also derived from PLL-B.

Bit 0 ... Bit 1: PLL-A Ratio determines the DAC sampling frequency $f_{DAC}$ = (PLL-A Ratio) x $f_{OSCIN}$; Valid entries are:

Bit 1,0
- 0,0: 1 x
- 0,1: 2 x
- 1,0: 4 x
- 1,1: 8 x

Bit 2 ... 5 Bit : PLL-B Multiplier M and Divider N determine the CLK-B output frequency.

RX-Output Multiplexed (10-/12-bit) [Reg 08, bit 0 =0]:
$f_{CLK-B} = f_{OSCIN} \times M/N$

RX-Output Non Multiplexed (6-bit), [Reg 08, bit 0 =1]:
$f_{CLK-B} = (f_{OSCIN} / 2) \times M/N$

All combinations between valid M and N values are allowed within the maximum frequency limits.

M
Bit 5,4
- 0,0: 3 x
- 0,1: 4 x
- 1,0: 6 x

N
Bit 3,2
- 0,0: / 2
- 0,1: / 4
- 1,0: / 1

Bit 6: ADC Clock Select defines if Fclk-B /2 is used for ADC sampling. RX SYNC pin is always half of CLK-B output clock frequency and frames the high nibble of the receive data.

This register defaults to 02h for PLL-A Multiplier Ratio=4, PLL-B Ratio M/N=3/2 and ADC sampled directly with Foscin for best phase noise performance.

**04h Receive Filter Selection**

The AD9875/6 integrates linear receive high pass filter, one pole low pass filter and tuned 4th order low pass (LP) filter. Each of the filters can be bypassed.

The linear 4th order Filter is automatically calibrated to one of two selectable cutoff frequencies. The cutoff frequency $f_{cutoff}$ is described as a function of the ADC sampling frequency $f_{ADC}$ and can be influenced (±25%) by the RX-Filter Tuning Target word in register 05h.

$f_{cutoff\ LOW} = 0.375 \times f_{ADC} \times 128 / Target$ (for anti-alias)
$f_{cutoff\ HIGH} = 0.9 \times f_{ADC} \times 128 / Target$

Bit 0: Receive LP-Filter Bypass: The 4th order receive low pass filter has a nominal ($f_{ADC}$=32MHz, Target=128) cutoff frequency of 12 MHz or 29 MHz and can be bypassed by writing a one to this bit. The default is one.

Bit 1: Input Filter One Pole Enable: The AD9875/6's can be configured with an additional first order ~16MHz input filter for applications that require steeper filter roll-off or want to use the ~16 MHz input filter instead of the tuned 4th order receive filter to save in power consumption or increase the bandwidth. Writing a one to this bit enables the one pole ~16 MHz filter. The one pole filters is not trimmed and subject to high cutoff frequency variations.

Bit 2: Receive Filter High Cutoff is used to select between high cutoff $f_{cutoff\ HIGH}$ or low cutoff $f_{cutoff\ LOW}$ filter tuning as described above. A receive LP-filter set to high cutoff frequency limits the maximum VGA gain to 30dB.

Bit 3: Receiver Fast Sampling VGA Setting enables the use of a high ADC sampling frequency (>50MSPS in 6-bit mode).

Bit 4: Receive HP-Filter Bypass disables the receive high pass filter to provide a DC path, save power and enable the use of a high ADC sampling frequency (>50MSPS in 6-bit mode).

Bit 5: Receiver Offset Correction. Writing a One to this bit triggers an immediate receive path offset correction and reads back zero after the completion of the offset correction.

Bit 6: Receive-Filter Tuning Update In Progress indicates when receive filter calibration is in progress. The duration of a receive filter calibration is about 500µs. Writing a one or zero to this bit does not have any effect.

Bit 7: Receive-Filter Tuning Update Disable stops the automatic background receive filter calibration. The AD9875/6 automatically calibrates the receive filter on reset and every few (~2) seconds thereafter to compensate for process and temperature variation, power supply and long term drift. Programming a one to this bit disables this function. Programming a zero triggers an immediate first calibration and enables the periodic update.

**05h - Receive Filter Tuning Target**

This register sets the filter tuning target as a function of Foscin. See register 04h description.

**06h - RX VGA Gain Control**

The AD9875/6 uses a combination of a coarse, continuous time and a fine, switched capacitor variable gain amplifier (VGA) for -6 to 36dB of gain with a minimum step size of 2dB. The VGA gain can be programmed over the serial interface by writing to the RX VGA Gain Control register or directly using the GAIN and msb aligned TX[5:1] bits. The register default value is 00h for lowest gain setting (-6dB). It always reads back the actual gain setting that may also have been programmed through the GAIN and TX[5:1] pins.

Bit 0 ... Bit 4: VGA Gain Control. Bit 3 is msb.
-6 dB=00h
-4 dB=01h
-2dB=02h
0dB=03h
...
36dB=15h(=21d)

VGA Gain Control = (Gain [dB] +6)/2.
A receive LP filter set to high cutoff frequency limits the maximum VGA gain to 30dB (30dB=12h=18d).

Bit 5: VGA Gain Setting through Register. This bit defines if VGA gain setting is programmed using either VGA Gain Control register or TX[5:1] pins. Default is zero for using TX[5:1] pins.

**07h Transmitter Settings**

The AD9875/6 can be programmed to various transmit interface options. The TX DAC uses interpolators that up-sample the incoming data to a two or four times higher DAC sampling frequency. Default is four times over-sampling with low pass filter characteristic.

Bit 0: TX-Input Multiplexer Bypass allows the transmit input demultiplexer to be bypassed for applications that require only six bits of dynamic range.

Bit 1: TX-Input Port Width (only for the 10- bit AD9875 !) defines if five bits are transferred first followed by the remaining five bits. Default is six bit for the most significant nibble and four bit for the less significant nibble. The data is always alligned to the MSB pin TX[5].
Enabling this pin on the AD9875 allows for a 5 pin versus the default 6 pin interface.

Bit 2: TX-Input LSB First reconfigures the AD9875/6 for a transmit mode that expects less significant bits before the most significant bits.

Bit 3: Power Down Interpolators at / TX QUIET Pin Low. / TX QUIET pin is used to shut off the DAC output. If the bit is set to one /TX QUIET pin low also puts the interpolator filters in a power down mode. In most applications the interpolators need to be flushed with zeros before or after being in power down mode.

Bit 4 ... Bit 7: TX-Interpolation Filter Setting defines the TX-filter characteristic and interpolation rate.
Bit 7,6,5,4
0,0,1,0: No Interpolation !
0,0,0,0: see Graph 1. 4 x interpolation, standard LP.
0,0,0,1: see Graph 2. 2 x interpolation, standard LP.
0,1,0,0: see Graph 3. 4 x interpolation Fs/2 mod.
0,1,0,1: see Graph 4. 2 x interpolation Fs/2 mod.
1,0,0,0: see Graph 5. 4 x interpolation, LP immage.
1,1,0,0: see Graph 6. 4 x interpolation, HP immage.
The interpolation rate has a direct influence on the data and CLK-A output frequency.
TX-Input multiplexer enabled (10/12- bit mode):
4x Interpolation: $f_{CLK-A} = f_{DAC} / 2$
2x Interpolation: $f_{CLK-A} = f_{DAC}$
No Interpolation: $f_{CLK-A} = f_{DAC} \times 2$
TX-Input multiplexer disabled (6- bit mode):
4x Interpolation: $f_{CLK-A} = f_{DAC} / 4$
2x Interpolation: $f_{CLK-A} = f_{DAC} / 2$
No Interpolation: $f_{CLK-A} = f_{DAC}$

**08h Receiver and Clock Output Settings**

Bit 0: RX-Output Multiplexer Bypass allows the receive output multiplexer to be bypassed for applications that require only six bits of dynamic range.

Bit 1: RX-Output Port Width (only for the 10- bit AD9875 !) defines if five bits are transferred first followed by the remaining five bits. Default is six bit most significant nibble and four bit least significant nibble. The data is always alligned to the MSB pin RX[5].
Enabling this pin on the AD9875 allows for a 5 pin interface versus the default 6 pin interface.

Bit 2: RX-Output LSB First reconfigures the AD9875/6 for a receive mode that expects less significant bits before the most significant bits.

Bit 3: RX Tristate. This bit sets the receive output RX[5:0] into a high impedance tristate mode. It allows for sharing the bus with other devices.

Bit 4: CLK-A Output Disable sets the CLK-A pin to a fixed low level.

Bit 5: CLK-B Output Disable sets the CLK-B pin to a fixed low level.

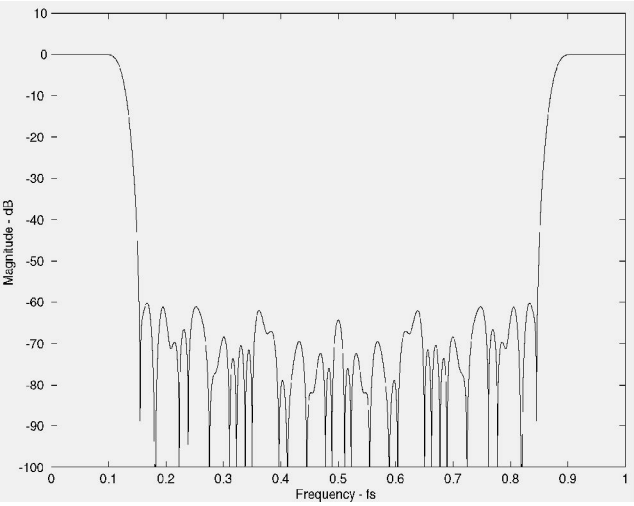
Bit 6: CLK-A Output Invert inverts the CLK-A output clock.

Bit 7: CLK-B Output Invert can be used to change data alignment from rising edge to falling edge of CLK-B.

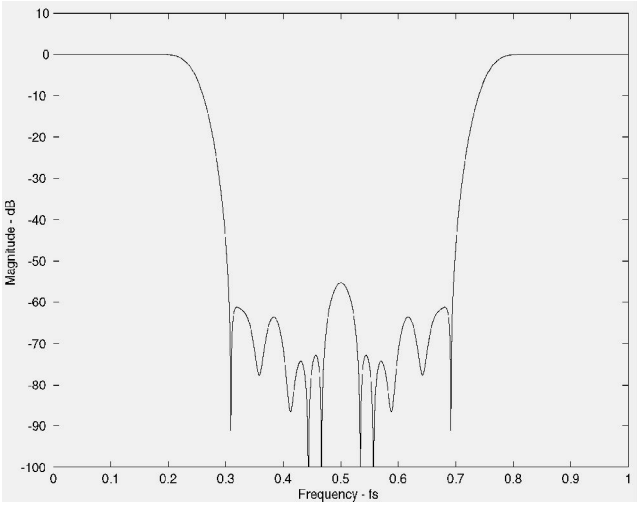
This register defaults to zero for CLK-A and CLK-B output clocks non-inverted and enabled. RX data is by default alligned MSB first and enabled.

**0Fh Version**

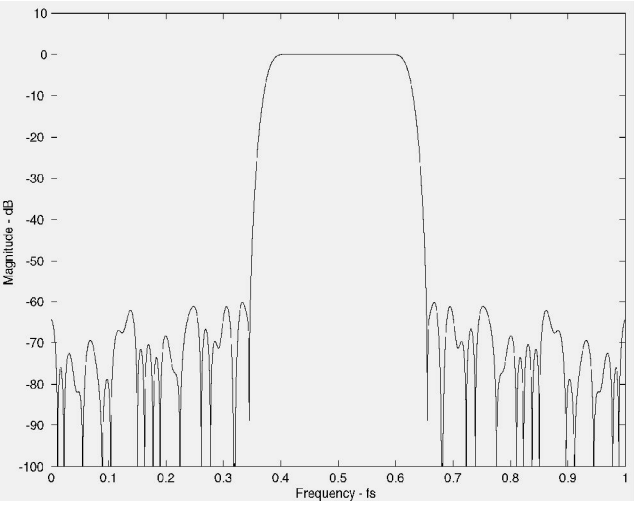
This register stores the die version of the chip. It can only be read.



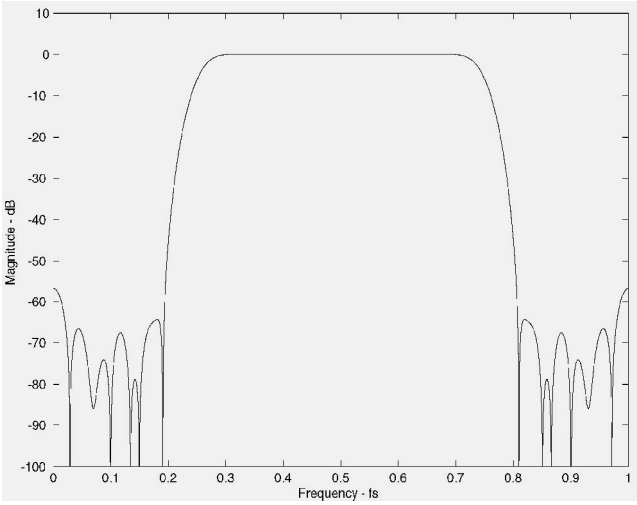

*Graph 1. 4 x Interpolation, Standard Low Pass Filter*



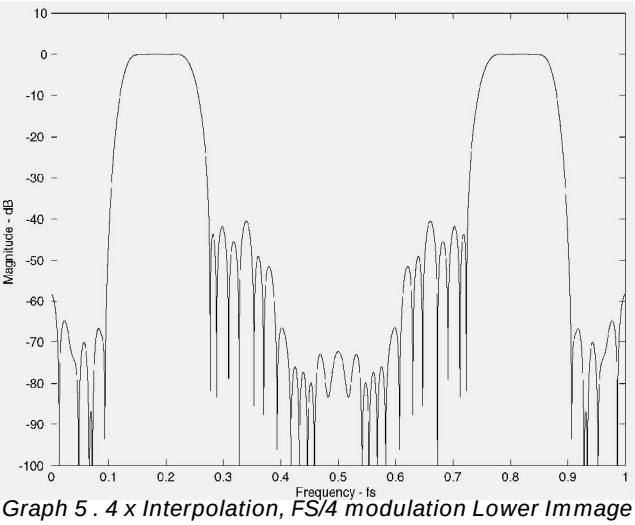

*Graph 2. 2 x Interpolation, Standard Low Pass Filter*



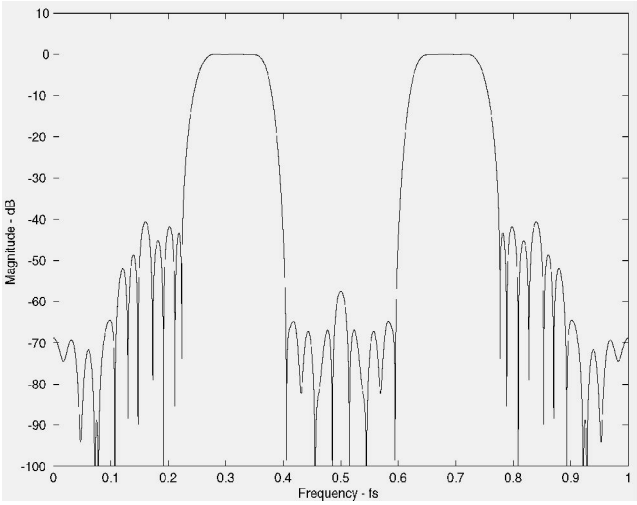

*Graph 3 . 4 x Interpolation, FS/2 modulation, no Filtering of Adjacent Immage*



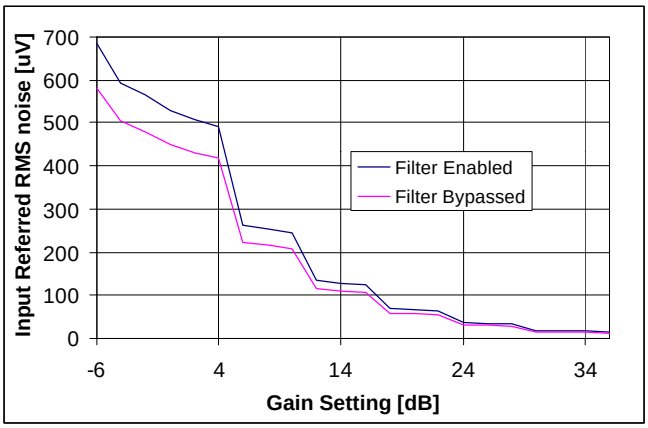

*Graph 4. 2 x Interpolation, FS/2 modulation, no Filtering of Adjacent Immage*



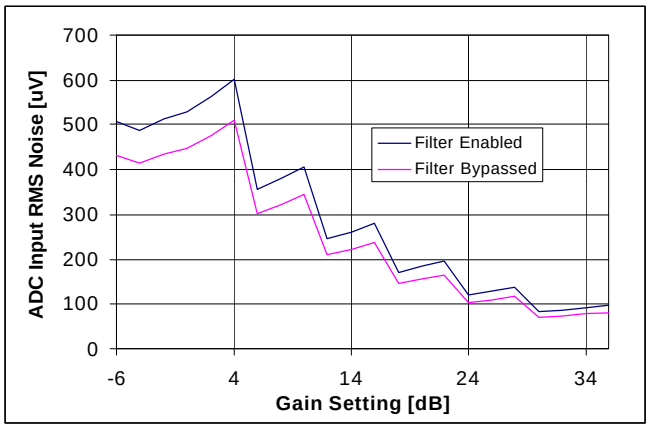

*Graph 5 . 4 x Interpolation, FS/4 modulation Lower Immage Preserved*




*Graph 6. 4 x Interpolation, FS/4 modulation,Upper Immage Preserved*




*Graph 6. RX Input Referred Noise vs. Gain*




*Graph 7. RX ADC Input Noise vs. Gain*

**TRANSMIT PATH**

The AD9875/6 transmit path consists of a Digital Interface Port, an Interpolation Filter and a Transmit DAC. All clock signals required by these blocks are generated from the PLL-A clock generator.

**DIGITAL INTERFACE PORT**

The transmit Digital Interface Port accepts half words through the TX[5:0] and TXSYNC pins and demultiplexes the data before passing it to the Interpolation filter. This interface also can be controlled by the GAIN pin to provide direct access to the PGA gain control register. The timing of the interface is fully described in the "Transmit Timing" section of this datasheet.

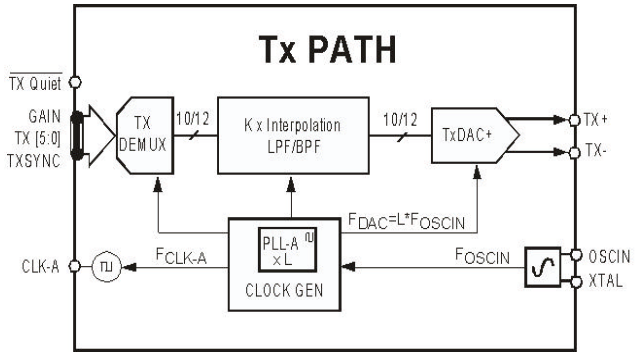



**FIGURE 1 -** Transmit Path Block Diagram

**DPLL-A CLOCK DISTRIBUTION**

Figure 1 shows the clock signals used in the transmit path. The DAC sampling clock, $F_{DAC}$, is generated by DPLL-A. $F_{DAC}$ has a frequency equal to L x $F_{OSCIN}$, where $F_{OSCIN}$ is the internal signal generated either by the crystal oscillator when a crystal is connected between the OSCIN and XTAL pins, or by the clock that is fed into the OSCIN pin, and L is the multiplier programmed through the serial port. L can have the values of 1, 2, 4, or 8.

The transmit path expects a new half-word of data at the rate of $F_{CLK-A}$. When the Tx multiplexer is enabled, the frequency of $F_{CLK-A}$ is equal to $2*F_{DAC}/K$ or $2*L*F_{OSCIN}/K$, where K is the interpolation factor which can be programmed to be 1, 2, or 4. When the Tx multiplexer is disabled, the frequency of $F_{CLK-A}$ is equal to $F_{DAC}/K$ or $L*F_{OSCIN}/K$.

**INTERPOLATION FILTER**

The interpolation filter can be programmed to run at 2x and 4x upsampling ratios in each of three different modes. The transfer functions of these six configurations are shown in Graphs1 through 6. The x-axis of each of these figures shows the frequency normalized to $F_{DAC}$. These transfer functions show just the discrete time tranfer function and do not include the sin(x)/x transfer function of the DAC. Also, the Interpolation Filter can be programmed into a pass-through mode if no interpolation filtering is desired.

**D/A CONVERTER**

A 10-/12-bit digital-to-analog converter (DAC) is used to convert the digitally processed waveform into an analog signal. The worst case spurious signals due to the DAC are the harmonics of the fundamental signal and their aliases (See the AD9851 data sheet for a detailed explanation of aliased images).

The AD9875/6 provides true and complement current outputs. The full-scale output current is set by the $R_{set}$ resistor at Pin x. The value of $R_{set}$ for a particular $I_{OUT}$ is determined using the following equation:

$R_{set}$ = 32 $V_{DACRset}$ /$R_{set}$ = ~ 39.4 / $I_{OUT}$.

For example, if a full-scale output current of 20 mA is desired, then $R_{set}$ = (39.4/0.02) Ω, or approximately 2 kΩ. Every doubling of the $R_{set}$ value will halve the output current. Maximum output current is specified as 20 mA.

The full-scale output current range of the AD9875/6 is 2mA–20mA. Full-scale output currents outside of this range will degrade SFDR performance. SFDR is also slightly affected by output matching, that is, the two outputs should be terminated equally for best SFDR performance. The output load should be located as close as possible to the AD9875/6 package to minimize stray capacitance and inductance. The load may be a simple resistor to ground, an op amp current-to-voltage converter, or a transformer-coupled circuit. It is best not to attempt to directly drive highly reactive loads (such as an LC filter). Driving an LC filter without a transformer requires that the filter be doubly terminated for best performance, that is, the filter input and output should both be resistively terminated with the appropriate values. The parallel combination of the two terminations will determine the load that the AD9875/6 will see for signals within the filter passband. For example, a 100 Ohm terminated input/output low-pass filter will look like a 50 Ohm load to the AD9875/6. The output compliance voltage of the AD9875/6 is –0.5 V to +1.5 V. Any signal developed at the DAC output should not exceed +1.5 V, otherwise, signal distortion will result. Furthermore, the signal may extend below ground as much as 0.5 V without damage or signal distortion. The AD9875/6 true and complement outputs can be differentially combined for common mode rejection using a broadband transformer. Using a grounded center-tap results in signals at the AD9875/6 DAC output pins that are symmetrical about ground. As previously mentioned, by differentially combining the two signals the user can provide some degree of common mode signal rejection.

## ADC THEORY OF OPERATION

The AD9875/6's analog to digital converter implements pipelined multistage architecture to achieve high sample rates while consuming low power. The ADC distributes the conversion over several smaller A/D subblocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, ADCs requires a small fraction of the $2^n$ comparators used in a traditional n-bit flash-type A/D. A sample-and-hold function within each of the stages permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Each stage of the pipeline, excluding the last, consists of a low resolution flash A/D connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash A/D.

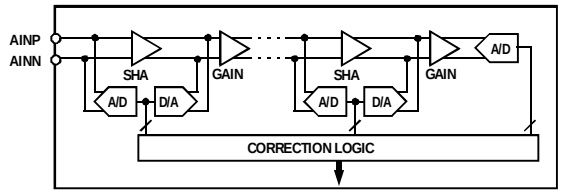



*Figure 1. ADC Theory of Operation*

The digital data outputs of the ADC are represented in 2's complement format. They saturate to full scale or zero when the input signal exceeds the input voltage range.

***2's Complement Data Format***

011..11: MAX ($+2^{n-1}$-1 lsb, n-bit resolution)

000..01: + 1 lsb
000..00: + 0 lsb
111..11: - 1 lsb
111..10: - 2 lsb

100..00: MIN ($-2^{n-1}$ lsb, n-bit resolution)

The data can be translated to offset binary data format by simply inverting the most significant bit. 2's Complement Data Format is usually represented in fractional numbers from -1 to +1 [- 1 lsb] for digital signal processing with a least significant bit (lsb) size of $1/(2^n)$.

**ADC Voltage References**

The AD9875/6 has an internal reference source. Figure xx shows the proper connections of the reference pins REFT and REFB. External references may be necessary for systems that require improvements in absolute accuracy, temperature drift and noise characteristics. External references REFT and REFB need to be centered at AVDD/2 with offset voltages as specified:

REFT: AVDD/2+0.5V
REFB: AVDD/2-0.5V

A differential level of 1V between the reference pins results in a 2V p-p input level at AIN and 2 V p-p input level at RX+/-. A differential level of 0.5V between the reference pins results in a 1 V p-p input level at AIN and 1 V p-p input level at RX+/-.

## CLOCK AND OSCILLATOR CIRCUITRY

The AD9875/6's internal oscillator generates all sampling clocks from a simple, low cost, series resonance, fundamental frequency quartz crystal. Figure xx shows how the quartz crystal is connected between OSC IN (pin x) and XTAL (pin x) with parallel resonant load capacitors as specified by the crystal manufacturer. The internal oscillator circuitry can also be overdriven by a TTL level clock applied to OSC IN with XTAL left unconnected.

**Transmit Timing (Default, Multiplexed TX data)**

The AD9875/6 provides a clock at pin CLK-A of two times the OSCIN frequency ($f_{OSCIN}$) and expects multiplexed TX data on every rising edge. Two nibbles form a complete 10-/12-bit transmit data sample of 2's complement format. Transmit data is framed with the TX SYNC input low for the most significant bits followed by TX SYNC high for the remaining, less significant bits. It can be changed with a register setting to least significant bits first with TX SYNC low followed by the remaining most significant bits and TX SYNC high.

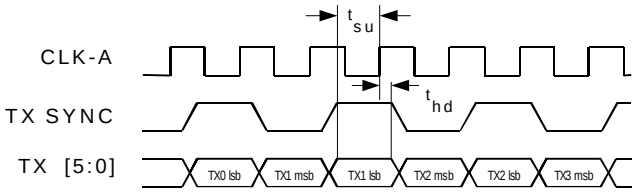



*Figure 3. Transmit Timing Diagram AD9875/6*

If TX SYNC is static low for more than one clock cycle then the last transmit data is continuously being fed into the transmit data path, independent of the TX[5:0] pins, until TX SYNC is brought high for the second nibble of a new transmit word. This feature can be used to "flush" the interpolator filters with zeros.

A register selection allows CLK-A to be inverted so that the AD9875/6 would take data on every falling edge instead of every rising edge.

**VGA Gain Setting (Default)**

The AD9875/6 shares the TX [5:1] pins between transmit data and 5-bit gain setting information for the receive signal variable gain amplifier (VGA). A high level on the GAIN pin with a low level on TX SYNC pin programs the VGA setting on every rising edge of CLK-A whereas a low level on the GAIN pin enables data to be fed to the interpolator and DAC.

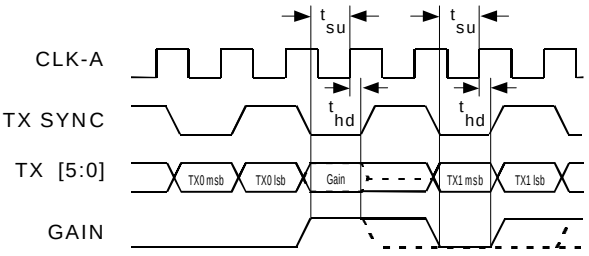



*Figure 4. GAIN Programming*

A register selection allows CLK-A to be inverted so that the AD9875/6 would take data on every falling edge instead of every rising edge.

**Receive Timing (Default, Multiplexed RX data)**

The AD9875/6 sends multiplexed data to the RX [5:0] outputs on every rising edge of CLK-A (CLK-B if $f_{PLL-B}/2$ is used for ADC sampling). RX SYNC low frames the most significant bits of the receive data whereas RX SYNC is high for the remaining, less significant bits. It can also be programmed for less significant bits first with RX SYNC low followed by the remaining most significant bits and RX SYNC high. The ADC is completely read on every second CLK-A cycle. Two nibbles form a complete 10-/12-bit receive data sample of 2's complement format.

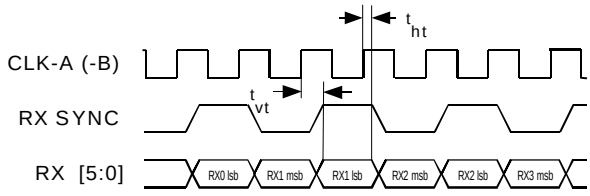



*Figure 5. Receive Timing Diagram*

Register selections allows CLK-A and/or CLK-B to be inverted so that the AD9875/6 would generate data on every falling edge instead of every rising edge.

## SERIAL INTERFACE FOR REGISTER CONTROL

The AD9875/6 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel SSR protocols. The interface allows read/write access to all registers that configure the AD9875/6. Single or multiple byte transfers are supported as well as MSB first or LSB first transfer formats. The AD9875/6's serial interface port uses a single, bidirectional data line (SDATA) .

### General Operation of the Serial Interface

There are two phases to a communication cycle with the AD9875/6. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9875/6, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9875/6 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9875/6.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9875/6 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Normally, using one multibyte transfer is the preferred method. However, single byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change *immediately* upon writing to the last bit of each transfer byte.

### Instruction Byte

The instruction byte contains the following information as shown below:

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| **I7** | **I6** | **I5** | **I4** | **I3** | **I2** | **I1** | **I0** |
| R/W | N1 | N0 | A4 | A3 | A2 | A1 | A0 |

R/W- bit 7 of the instruction byte determines whether a read or a write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic zero indicates a write operation. N1, N0 -Bits 6 and 5 of the instruction byte determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in the table below:

| N1 | N0 | Description |
|---|---|---|
| 0 | 0 | Transfer 1 Byte |
| 0 | 1 | Transfer 2 Bytes |
| 1 | 0 | Transfer 3 Bytes |
| 1 | 1 | Transfer 4 Bytes |

A4, A3, A2, A1, A0—Bits 4, 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9875/6.

### Serial Interface Port Pin Description

SCLK—Serial Clock. The serial clock pin is used to synchronize data to and from the AD9875/6 and to run the internal state machines. SCLK maximum frequency is 15 MHz. All data input to the AD9875/6 is registered on the rising edge of SCLK. All data is driven out of the AD9875/6 on the falling edge of SCLK.

SENABLE—Serial Interface Enable. Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDATA pin will go to a high impedance state when this input is high. SENABLE select should stay low during the entire communication cycle.

SDATA—Serial Data I/O. Data is always written into the AD9875/6 on this pin. However, this pin can be used as a bidirectional data line to read register contents.

### MSB/LSB Transfers

The AD9875/6 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by register address 0h bit 6. The default is MSB first. When this bit is set active high, the AD9875/6 serial port is in LSB first format. That is, if the AD9875/6 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the most significant byte. In MSB first mode, the serial port internal byte address generator decrements for each byte required of the multibyte communication cycle. Multibyte data transfers in LSB first format can be completed by writing an instruction byte that includes the register address of the least significant byte. In LSB first mode, the serial port internal byte address generator increments for each byte required of the multibyte communication cycle.

### Notes on Serial Port Operation

The AD9875/6 serial port configuration bits reside in bits 6 and 7 of register address 00h. It is important to note that the configuration changes *immediately* upon writing to the last bit of the register. For multibyte transfers, writing to this register may occur during the middle of communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

Same considerations apply to setting the reset bit in register address 00h. All other registers are set to their default values but the software reset doesn't affect the bits in register address 00h !

It is recommended to use only single byte transfers when changing serial port configurations (MSB/LSB first) or initiating a software reset.

A write to bits 1, 2 and 3 of address 00h with the same logic levels as for bits 7, 6 and 5 (bit pattern: XY1001YX binary) allows to reprogram a lost serial port configuration and to reset the registers to their default values.

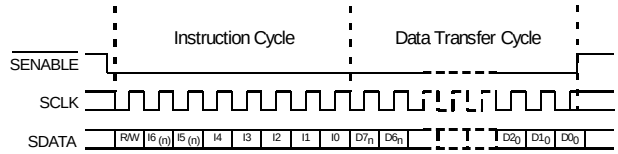



*Figure 6a. Serial Register Interface Timing MSB-First*

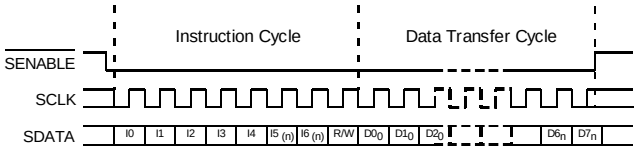



*Figure 6b. Serial Register Interface Timing LSB-First*

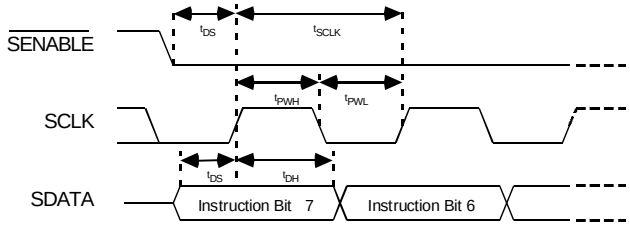



*Figure 7. Timing Diagram Register Write to AD9875/6*

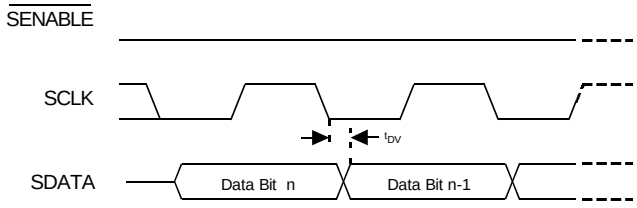



*Figure 8. Timing Diagram Register Read from AD9875/6*

## LAYOUT RECOMMENDATIONS

When designing with mixed signal systems (digital and analog), it is generally important to insure that any noise or current spikes of the digital portion do not couple into the analog portion. To accomplish this, there are two standard methods for approaching the problem.

One method, is to isolate the analog ground plane from the digital ground plane by means of physically isolating the etch of these planes. A commonality ground junction is made between theses planes with a small section of etch. This method is effective as long as there is enough area within the analog ground plane to disperse the energy created by the analog components. If not, this could lead to radiated emissions problems.

The other method, is utilize a common, solid ground plane for both the digital and analog circuitry. This approach requires careful placement of the analog circuitry to insure that it is not in the path of the digital return currents.

Both of the previous methods referred to quieting the analog section via ground plane methods. In either case, any power voltages to the analog devices should be source filtered prior to going into the analog components.

The AD9875/6 is a mixed signal chip and therefore contains analog, digital and mixed signal functionality. Proper decoupling between the power and ground pins, at the AD9875/6 is essential to reduce noise.

In a system that includes digital ASICs and Controllers with high switching currents, the AD9875/6 can be looked at as an analog chip for PCB layout design considerations. At first glance, this might seem somewhat contradictory since the converter has pins assigned to analog ground (AVSS) and digital ground (DVSS and DRVSS). But wirebond inductance and resistance allow rapidly changing digital currents to develop and couple into the analog circuits through stray capacitance between pads. In order to prevent further coupling, analog and digital ground points should be joined together externally to the analog ground plane with minimum lead length. Any extra impedance in the digital ground connection will cause more digital noise to be developed.

Interference between analog return paths and digital return currents should be minimized.

In systems where AD9875/6's driver supply (DRVSS and DRVDD) is directly shared with other fast switching digital logic circuitry it might be necessary to reference the driver supply to digital ground.

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm)

**48-Lead Thin Plastic Quad Flat Pack IC Package**

**(LQFP, ST-48)**