

FEATURES

- 4 Complete 12-Bit D/A Functions
- Double-Buffered Latches
- Simultaneous Update of All DACs Possible
- ± 5 V Output Range
- High Stability Bandgap Reference
- Monolithic BiMOS Construction
- Guaranteed Monotonic over Temperature
- $3/4$ LSB Linearity Guaranteed over Temperature
- 4 μ s max Settling Time to 0.01%
- Operates with ± 12 V Supplies
- Low Power: 720 mW max Including Reference
- TTL/5 V CMOS Compatible Logic Inputs
- 8-Bit Microprocessor Interface
- 24-Pin PDIP or 28-Lead PLCC Package

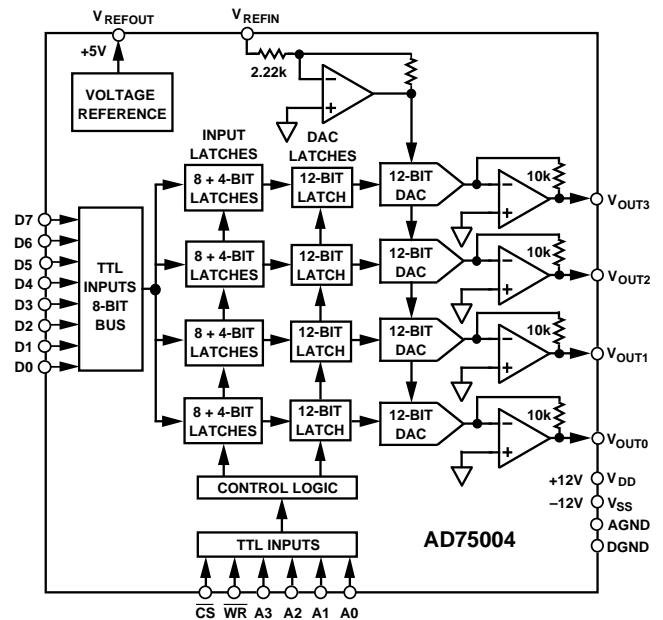
PRODUCT DESCRIPTION

The AD75004 contains four complete, voltage output, 12-bit digital-to-analog converters, a high stability bandgap reference, and double-buffered input latches on a single chip. The converters use 12 precision high speed bipolar current steering switches and laser-trimmed thin-film resistor networks to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latches. The design of the input latches allows direct interface to 8-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 50 ns, allowing use with fast microprocessors.

The functional completeness and high performance of the AD75004 results from a combination of advanced switch design, the BiMOS II fabrication process, and proven laser trimming technology. BiMOS II is an epitaxial BiCMOS process optimized for analog and converter functions. The AD75004 is trimmed at the wafer level and is specified to $\pm 1/2$ LSB maximum linearity error at 25°C and $\pm 3/4$ LSB over the full operating temperature range. The on-chip output amplifiers provide an output range of ± 5 V, with 1 LSB equal to 2.44 mV.

FUNCTIONAL BLOCK DIAGRAM



The bandgap reference on the chip has low noise, long term stability and temperature drift characteristics comparable to discrete reference diodes. The absolute value of the reference is laser trimmed to +5.00 V with 0.6% maximum error. Its temperature coefficient is also laser trimmed.

Typical full-scale gain TC is 15 ppm/°C. With guaranteed monotonicity over the full temperature range, the AD75004 is well suited for wide temperature range performance.

REV. A

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AD75004–SPECIFICATIONS (T_A = +25°C, ±12.0 V power supplies unless otherwise noted)

| Parameter | Symbol | Min | Typ | Max | Units |
|--|-------------------------------------|--------------|----------------------|--------------|--------------|
| DIGITAL INPUTS (D0–D7, A0–A3, \overline{CS}, \overline{WR}) | | | | | |
| Logic Levels (TTL Compatible) | | | | | |
| Input Voltage, Logic “1” | V _{IH} | 2.0 | | 5.5 | V |
| Input Voltage, Logic “0” | V _{IL} | 0 | | 0.8 | V |
| Input Current, V _{IH} = 5.5 V | I _{IH} | | | 10 | μA |
| Input Current, V _{IL} = 0.8 V | I _{IL} | | | 10 | μA |
| Input Capacitance | C _{IN} | | | 10 | pF |
| ACCURACY | | | | | |
| Resolution | | | | 12 | Bits |
| Integral Linearity Error | | | ±1/4 | ±1/2 | LSB |
| Integral Linearity Error, T _{MIN} to T _{MAX} | | | ±1/2 | ±3/4 | LSB |
| Differential Linearity Error | | | ±1/2 | ±3/4 | LSB |
| Differential Linearity Error, T _{MIN} to T _{MAX} | | | Guaranteed Monotonic | | |
| Gain (Full-Scale) Error ¹ | | | ±2 | ±10 | LSB |
| Gain Error Drift, T _{MIN} to T _{MAX} ¹ | | | ±15 | ±30 | ppm/°C |
| Bipolar Zero Error ¹ | | | ±1 | ±2 | LSB |
| Bipolar Zero Error Drift, T _{MIN} to T _{MAX} ¹ | | | ±3 | ±7 | ppm/°C |
| CHANNEL-TO-CHANNEL MISMATCH | | | | | |
| Integral Linearity Error | | | ±1/2 | ±1 | LSB |
| Gain Error ¹ | | | ±1 | ±4 | LSB |
| Bipolar Zero Error ¹ | | | ±1 | ±2 | LSB |
| DYNAMIC PERFORMANCE | | | | | |
| Settling Time to ±0.01% of FSR for FSR Change, 2 kΩ 500 pF Load | | | 2 | 4 | μs |
| Slew Rate, 2 kΩ 500 pF Load | | 5 | | | V/μs |
| Digital Input Crosstalk (Static) ² | | | | -50 | dB |
| ANALOG OUTPUTS | | | | | |
| Full-Scale Range (FSR) | V _{OUT} | | ±5 | | V |
| Output Current | I _{OUT} | ±5 | | | mA |
| Short Circuit Limit Current | | | | ±40 | mA |
| VOLTAGE REFERENCE | | | | | |
| Reference Output Voltage | V _{REFOUT} | 4.97 | 5.00 | 5.03 | V |
| Temperature Coefficient | | | ±15 | ±25 | ppm/°C |
| Reference Output Currents ³ | | 3.0 | 5.0 | | mA |
| Reference Input Voltage | V _{REFIN} | 4.5 | 5.0 | 5.5 | V |
| Reference Input Current @ 5.0 V | I _{REFIN} | | | 3.0 | mA |
| POWER SUPPLY GAIN SENSITIVITY | | | | | |
| ΔGain/ΔV _{DD} , V _{DD} = +10.8 to +13.2 V dc ¹ | | | ±15 | ±25 | ppm of FSR/% |
| ΔGain/ΔV _{SS} , V _{SS} = -10.8 to -13.2 V dc ¹ | | | ±15 | ±25 | ppm of FSR/% |
| POWER SUPPLY REQUIREMENTS | | | | | |
| Voltage Range | V _{DD} , V _{SS} | ±10.8 | ±12 | ±13.2 | V |
| Supply Currents | I _{DD} , I _{SS} | | ±25 | ±30 | mA |
| TEMPERATURE RANGE | | | | | |
| Specification | T _{MIN} , T _{MAX} | 0 | | +70 | °C |
| Storage | | -65 | | +150 | °C |

NOTES

¹Gain and bipolar zero errors are measured using internal voltage reference and include its errors.

²Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2 kΩ || 500 pF load by means of varying the digital input code.

³The internal voltage reference is intended to drive on-chip only; buffer it if using it externally.

⁴All minimum and maximum specifications are guaranteed, and specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

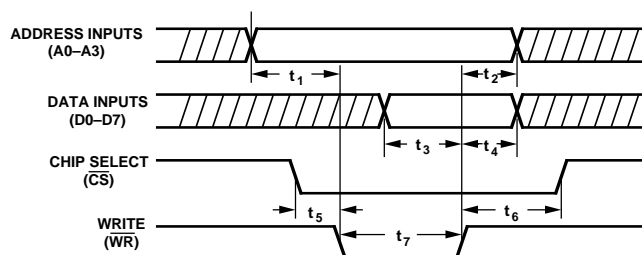
TIMING CHARACTERISTICS¹(T_A = +25°C, ±12.0 V power supplies unless otherwise noted)

| Parameter | Symbol | Min | Units |
|---------------------------------|----------------|-----|-------|
| Address Setup Time | t ₁ | 30 | ns |
| Address Hold Time | t ₂ | 10 | ns |
| Data Setup Time | t ₃ | 10 | ns |
| Data Hold Time | t ₄ | 45 | ns |
| Chip Select to Write Setup Time | t ₅ | 0 | ns |
| Write to Chip Select Hold Time | t ₆ | 0 | ns |
| Write Pulse Width | t ₇ | 50 | ns |

NOTES

¹Timing measurement reference level is 1.5 V.

Specifications subject to change without notice



TRUTH TABLE

| Control and Address Lines | | | | | | Operation |
|---------------------------|----|----|----|-----|-----|--------------------------|
| CS | WR | A3 | A2 | A1 | A0 | |
| 1 | X | X | X | X | X | No operation |
| X | 1 | X | X | X | X | No operation |
| 0 | 0 | 0 | 0 | A1* | A0* | 8 LSBs → one input latch |
| 0 | 0 | 0 | 1 | A1* | A0* | 4 MSBs → one input latch |
| 0 | 0 | 1 | 0 | A1* | A0* | Update one DAC latch |
| 0 | 0 | 1 | 1 | X | X | Update all 4 DAC latches |

NOTE

*The A1 and A0 inputs specify the relevant channel.

| A1 | A0 | Channel |
|----|----|---------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

| | Min | Max | Units | Conditions | |
|------------------------------------|------|-----------------|-------|-----------------------|-----------------------|
| V _{DD} to DGND | -0.3 | +18 | V | T _A ≤ 75°C | |
| V _{SS} to DGND | -18 | +0.3 | V | | |
| V _{DD} to V _{SS} | -0.3 | +26.4 | V | | |
| V _{REFIN} to AGND | -0.3 | V _{DD} | V | | |
| Digital Inputs to DGND | -0.3 | V _{DD} | V | | |
| AGND to DGND | -0.3 | +0.3 | V | | |
| Short to AGND on Analog Outputs | | Indefinite | sec | | |
| Power Dissipation | | 1.0 | W | | |
| Specification Temperature Range | 0 | +70 | °C | | |
| Storage Temperature | -65 | +150 | °C | | |
| Lead Temperature | | +300 | °C | | |
| | | | | | Soldering, 10 seconds |

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD75004 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

| Model | Temperature Range | Package Option* |
|-----------|-------------------|-----------------|
| AD75004KN | 0°C to +70°C | N-24A |
| AD75004KP | 0°C to +70°C | P-28A |

*N = Plastic DIP; P = Plastic Leaded Chip Carrier.

AD75004

PIN DESCRIPTIONS

| PLCC Pin | Plastic DIP Pin | Name | Description |
|----------|-----------------|---------------------|-------------------------------|
| 1 | 1 | D7 | Data Input Bit 7 |
| 2 | 2 | D6 | Data Input Bit 6 |
| 3 | 3 | D5 | Data Input Bit 5 |
| 5 | 4 | D4 | Data Input Bit 4 |
| 6 | 5 | D3 | Data Input Bit 3 or 11 (MSB) |
| 7 | 6 | D2 | Data Input Bit 2 or 10 |
| 9 | 7 | D1 | Data Input Bit 1 or 9 |
| 10 | 8 | D0 | Data Input Bit 0 (LSB) or 8 |
| 11 | 9 | \overline{CS} | Chip Select Input; Active Low |
| 13 | 10 | \overline{WR} | Write Input; Active Low |
| 14 | 11 | A3 | Address Input Bit 3 (MSB) |
| 15 | 12 | A2 | Address Input Bit 2 |
| 16 | 13 | A1 | Address Input Bit 1 |
| 17 | 14 | A0 | Address Input Bit 0 (LSB) |
| 18 | 15 | DGND | Digital Ground |
| 19 | 16 | AGND | Analog Ground |
| 20 | 17 | V _{SS} | -12 V Power Supply |
| 21 | 18 | V _{REFOUT} | +5 V Reference Output |
| 22 | 19 | V _{REFIN} | Reference Input |
| 23 | 20 | V _{OUT0} | Analog Output 0 |
| 24 | 21 | V _{OUT1} | Analog Output 1 |
| 26 | 22 | V _{OUT2} | Analog Output 2 |
| 27 | 23 | V _{OUT3} | Analog Output 3 |
| 28 | 24 | V _{DD} | +12 V Power Supply |
| 4 | - | NC | No Internal Connection |
| 8 | - | NC | No Internal Connection |
| 12 | - | NC | No Internal Connection |
| 25 | - | NC | No Internal Connection |

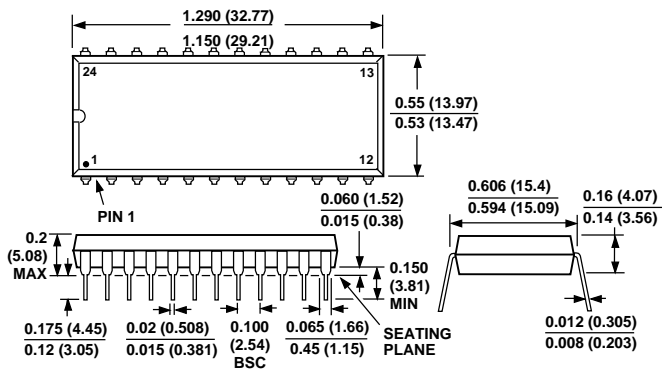
BINARY CODE TABLE

| Twos Complement Value in DAC Latch | | | Analog Output Voltage |
|------------------------------------|------|------|---------------------------|
| MSB | LSB | | |
| 0111 | 1111 | 1111 | $(2047/2048) * V_{REFIN}$ |
| 0000 | 0000 | 0001 | $(1/2048) * V_{REFIN}$ |
| 0000 | 0000 | 0000 | 0 V |
| 1111 | 1111 | 1111 | $-(1/2048) * V_{REFIN}$ |
| 1000 | 0000 | 0000 | $-V_{REFIN}$ |

OUTLINE DIMENSIONS

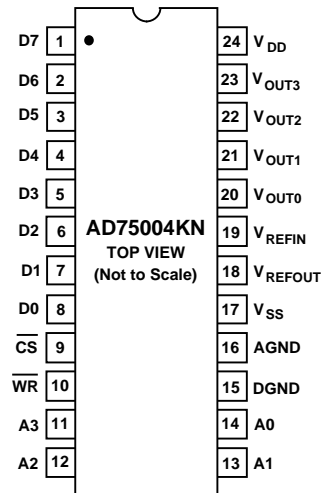
Dimensions shown in inches and (mm).

Plastic DIP (N-24A)

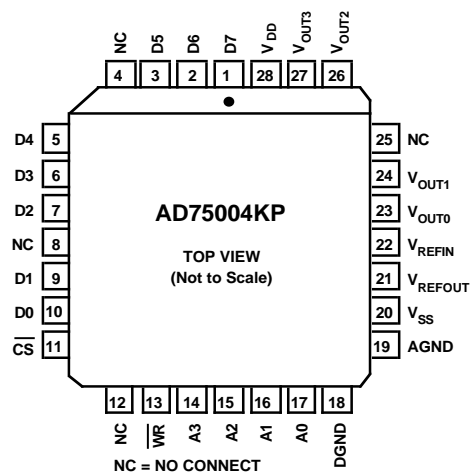


PIN CONFIGURATIONS

24-Pin Plastic DIP



28-Pin PLCC



PLCC (P-28A)

