

# 9601

## RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

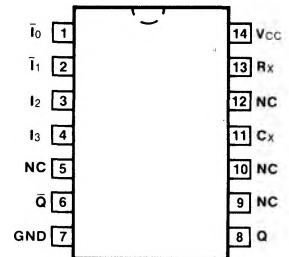
**DESCRIPTION** — The 9601 is a retriggerable one-shot with versatile trigger gating, rapid recovery, internally compensated reference levels, and high speed capability. It is well suited for a broad variety of applications, including pulse delay generators, square wave generators, long delay timers, pulse absence detectors, and clock pulse generators.

- **RETRIGGERABLE, 0% TO 100% DUTY CYCLE**
- **DC LEVEL TRIGGERING, INSENSITIVE TO TRANSITION TIMES**
- **COMPLEMENTARY INPUTS, FOR LEADING OR TRAILING-EDGE TRIGGERING**
- **COMPLEMENTARY OUTPUTS, WITH ACTIVE PULL-UPS FOR DRIVING LOAD CAPACITANCE.**
- **PULSE WIDTH COMPENSATION FOR  $V_{CC}$  AND TEMPERATURE VARIATIONS**
- **50 ns TO  $\infty$  OUTPUT PULSE WIDTH RANGE**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**

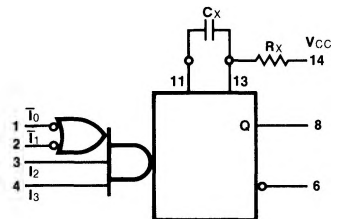
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$ , $T_A = 0^\circ\text{C to } +75^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$ , $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	9601PC		9A
Ceramic DIP (D)	A	9601DC	9601DM	6A
Flatpak (F)	A	9601FC	9601FM	3I

### CONNECTION DIAGRAM PINOUT A



### LOGIC SYMBOL

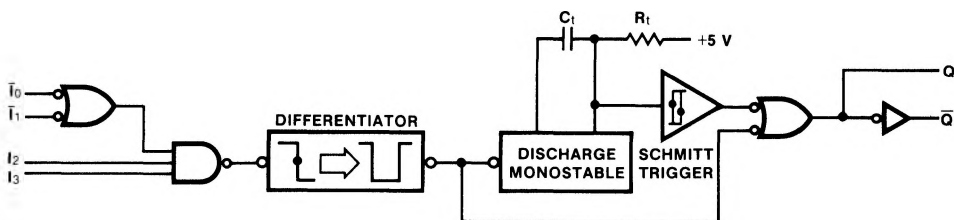


$V_{CC} = \text{Pin } 14$   
 $GND = \text{Pin } 7$

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
$\bar{I}_0, \bar{I}_1$	Trigger Input (Active Falling Edge)	1.5/1.0
$I_2, I_3$	Trigger Input (Active Rising Edge)	1.5/1.0
Q	Positive Pulse Output	24/8.0 (18)/(6.25)
$\bar{Q}$	Complementary Pulse Output	24/8.0 (18)/(6.25)

FUNCTIONAL BLOCK DIAGRAM



TRIGGERING TRUTH TABLE

Pin 1	Pin 2	Pin 3	Pin 4	RESPONSE
H	H	$\int$	X	No Trigger
L	X	$\int$	H	Triggers
L	X	$\int$	L	No Trigger
$\int$	H	H	H	Triggers
$\int$	H	L	X	No Trigger
$\int$	L	X	X	No Trigger

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

OUTPUT  $t_w$  vs  $R_x$  AND  $C_x$

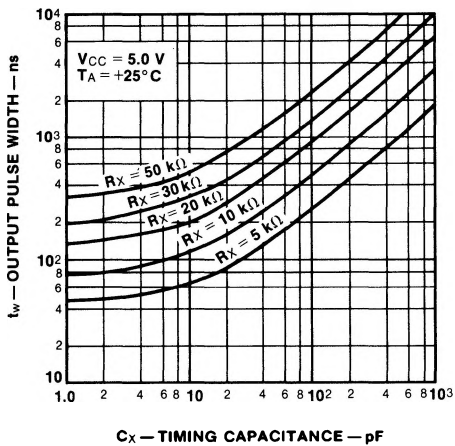
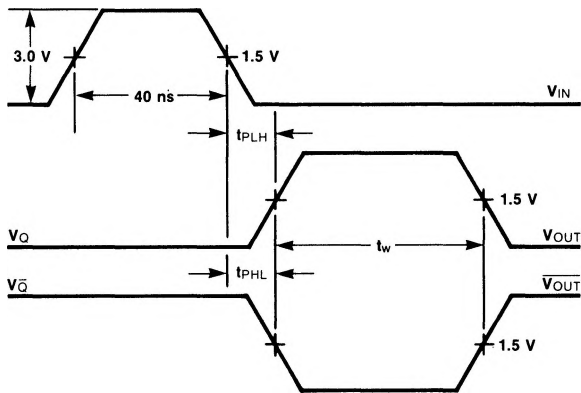


Fig. a



NOTE:  
 Capacitance includes Jig and Probe

Fig. b

**FUNCTIONAL DESCRIPTION** — The 9601 monostable multivibrator has four inputs, two active HIGH and two active LOW. This allows a choice of leading-edge or trailing-edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9601 and result in a continuous true output. Retriggering may be inhibited by tying the negation ( $\bar{Q}$ ) output to an active LOW input. Active pullups are provided on the outputs for good drive capability into capacitive loads.

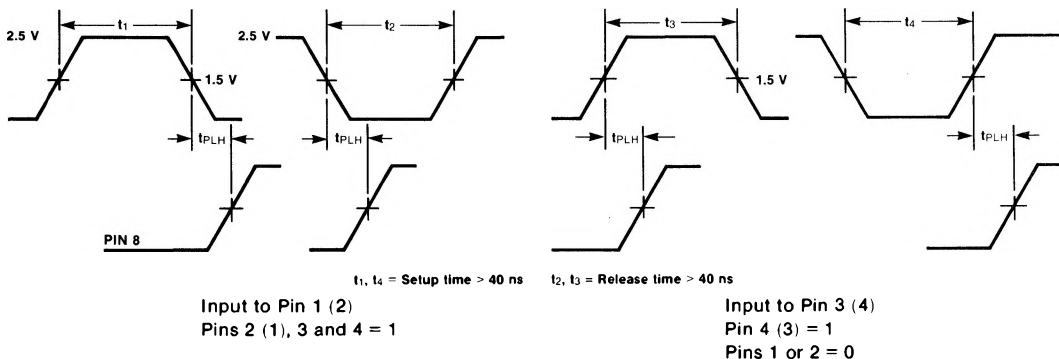
### Operation Notes

- TRIGGERING** — The 9601 has four dc coupled triggering inputs; pins 1 and 2 respond to falling edge signals, while pins 3 and 4 respond to rising edge signals. Triggering occurs as the input signal passes through the threshold region. Triggering logic is outlined in the Table. Input signals can be interchanged between pins 1 and 2, since they are logically identical; the same relationship holds for pins 3 and 4.
- RETRIGGERING** — In a normal cycle, triggering initiates a rapid discharge of the external timing capacitor, followed by a ramp voltage run-up at pin 13. The delay will time out when the ramp voltage reaches the upper trigger point of the Schmitt circuit, causing the outputs to revert to the quiescent state. If another trigger occurs before the ramp voltage reaches the Schmitt threshold, the capacitor will be discharged and the ramp will start again without having disturbed the outputs. The delay period can therefore be extended for an arbitrary length of time by insuring that the interval between triggers is less than the delay time, as determined by the external capacitor and resistor.
- NON-RETRIGGERABLE OPERATION** — Retriggering can be inhibited logically, by connecting pin 6 back to pin 3 or 4, or by connecting pin 8 back to both pins 1 and 2.
- OUTPUT PULSE WIDTH** — An external resistor  $R_X$  and an external capacitor  $C_X$  are required, as shown in the functional block diagram; to minimize stray capacitance and noise pickup,  $R_X$  and  $C_X$  should be located as close as possible to the circuit. In applications which require remote trimming of the pulse width, as with a variable resistor,  $R_X$  should consist of a fixed resistor in series with the variable resistor; the fixed resistor should be located as close as possible to the circuit. The output pulse width  $t_w$  is defined as follows, where  $R_X$  is in  $k\Omega$ ,  $C_X$  is in  $pF$  and  $t_w$  is in  $ns$ .

$$t_w = 0.32 R_X C_X (1 + 0.7/R_X) \quad (\text{for } C_X > 10^3 \text{ pF; see also Figure a.})$$

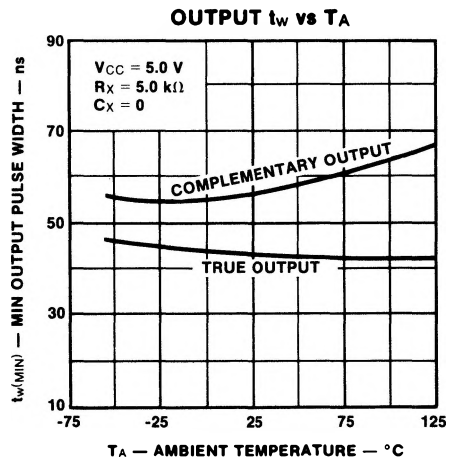
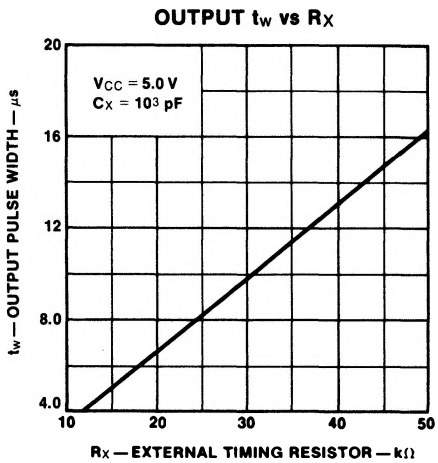
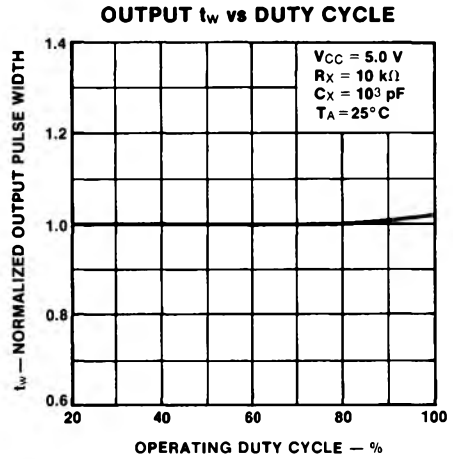
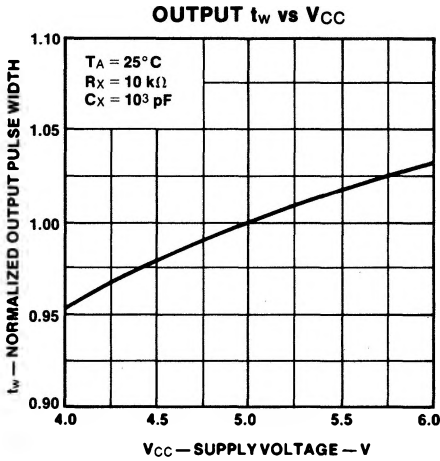
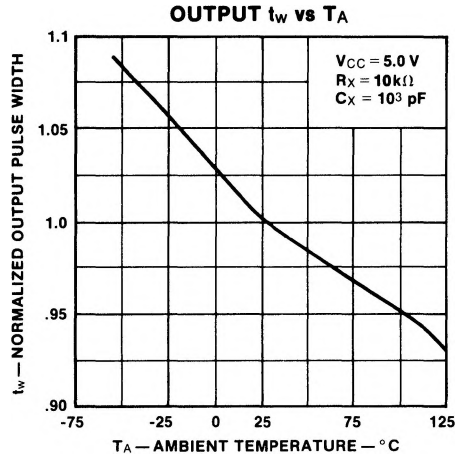
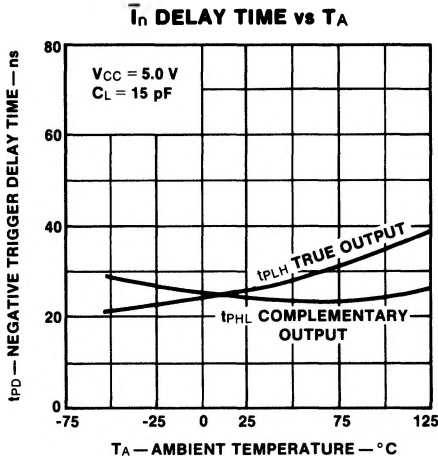
The values of  $R_X$  may vary from 5.0  $k\Omega$  to 50  $k\Omega$  for  $0^\circ$  to  $+75^\circ C$  operation, and 5.0  $k\Omega$  to 25  $k\Omega$  for  $-55^\circ$  to  $+125^\circ C$  operation.  $C_X$  may vary from 0 to any value.

### 5. SETUP AND RELEASE TIMES



- CAPACITOR LEAKAGE** — Recommendations on electrolytic capacitors and larger values of  $R_X$  are discussed in the 9600 data sheet.

TYPICAL CHARACTERISTICS



DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE:  $V_{CC} = +5.0$  V except as noted.

SYMBOL	PARAMETER	0°C		+25°C		+75°C		UNITS	CONDITIONS <sup>1</sup>
		Min	Max	Min	Max	Min	Max		
$V_{OH}$	Output HIGH Voltage <sup>2</sup>	2.4		2.4		2.4		V	$V_{CC} = 4.75$ V $I_{OH} = -0.96$ mA
$V_{OL}$	Output LOW Voltage <sup>2</sup>		0.45		0.45		0.45	V	$V_{CC} = 4.75$ V $I_{OL} = 12.8$ mA
$V_{IH}$	Input HIGH Voltage <sup>3</sup>	1.9		1.8		1.6		V	
$V_{IL}$	Input LOW Voltage <sup>3</sup>		0.85		0.85		0.85	V	
$I_{IL}$	Input LOW Current		-1.6		-1.6		-1.6	mA	$V_{CC} = 5.25$ V $V_{IN} = 0.45$ V
$I_{IH}$	Input HIGH Current				60		60	$\mu$ A	$V_{CC} = 5.25$ V $V_{IN} = 4.5$ V
$I_{OS}$	Output Short Circuit Current <sup>2</sup>			-10	-40			mA	$V_{OUT} = 0$ V
$I_{CC}$	Power Supply Current		25		25		25	mA	$V_{CC} = 5.25$ V Gnd Pins 1, 2
$t_{PLH}$	Propagation Delay $\bar{I}_n$ to Q				40			ns	$R_X = 5.0$ k $\Omega$ $C_L = 15$ pF $C_X = 0$ , Fig. b
$t_{PHL}$	Propagation Delay $\bar{I}_n$ to $\bar{Q}$				40			ns	$R_X = 5.0$ k $\Omega$ $C_L = 15$ pF $C_X = 0$ , Fig. b
$t_w$ (min)	Minimum True Output Pulse Width				65			ns	$R_X = 5.0$ k $\Omega$ $C_L = 15$ pF $C_X = 0$ , Fig. b
$t_w$	Pulse Width			3.08	3.76			$\mu$ s	$R_X = 10$ k $\Omega$ $C_X = 1000$ pF Fig. b
$C_{STRAY}$	Maximum Allowable Wiring Cap. (Pin 13)		50		50		50	pF	Pin 13 to Gnd
$R_X$	Timing Resistor	5.0	50	5.0	50	5.0	50	k $\Omega$	

(1) Unless otherwise noted, 10 k $\Omega$  resistor placed between Pin 13 and  $V_{CC}$ , for all tests. ( $R_X$ )(2) Ground Pin 11 for  $V_{OL}$  Pin 6 or  $V_{OH}$  Pin 8 or  $I_{OS}$  Pin 8. Open Pin 11 for  $V_{OL}$  Pin 8 or  $V_{OH}$  Pin 6 or  $I_{OS}$  Pin 6.(3) Pulse Test to determine  $V_{IH}$  and  $V_{IL}$  (Min  $t_w$  40 ns).

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE:  $V_{CC} = +5.0$  V except as noted

SYMBOL	PARAMETER	-55°C		+25°C		+125°C		UNITS	CONDITIONS <sup>1</sup>
		Min	Max	Min	Max	Min	Max		
$V_{OH}$	Output HIGH Voltage <sup>2</sup>	2.4		2.4		2.4		V	$V_{CC} = 4.5$ V $I_{OH} = -0.72$ mA
$V_{OL}$	Output LOW Voltage <sup>2</sup>		0.4		0.4		0.4	V	$V_{CC} = 4.5$ V $I_{OL} = 10$ mA
$V_{IH}$	Input HIGH Voltage <sup>3</sup>	2.0		1.7		1.5		V	
$V_{IL}$	Input LOW Voltage <sup>3</sup>		0.85		0.9		0.85	V	
$I_{IL}$	Input LOW Current		-1.6		-1.6		-1.6	mA	$V_{CC} = 5.5$ V $V_{IN} = 0.4$ V
$I_{IH}$	Input HIGH Current				60		60	$\mu$ A	$V_{CC} = 5.5$ V $V_{IN} = 4.5$ V
$I_{OS}$	Output Short Circuit Current			-10	-40			mA	$V_{OUT} = 0$ V
$I_{CC}$	Power Supply Current		25		25		25	mA	$V_{CC} = 5.5$ V Gnd Pins 1, 2
$t_{PLH}$	Propagation Delay $\bar{I}_n$ to Q				40			ns	$R_X = 5.0$ k $\Omega$ $C_L = 15$ pF $C_X = 0$ , Fig. b
$t_{PHL}$	Propagation Delay $\bar{I}_n$ to $\bar{Q}$				40			ns	$R_X = 5.0$ k $\Omega$ $C_L = 15$ pF $C_X = 0$ , Fig. b.
$t_w$ (min)	Minimum True Output Pulse Width				65			ns	$R_X = 5.0$ k $\Omega$ $C_L = 15$ pF $C_X = 0$ , Fig. b
$t_w$	Pulse Width			3.08	3.76			$\mu$ s	$R_X = 10$ k $\Omega$ $C_X = 1000$ pF Fig. b
$C_{STRAY}$	Maximum Allowable Wiring Cap. (Pin 13)		50		50		50	pF	Pin 13 to Gnd
$R_X$	Timing Resistor	5.0	25	5.0	25	5.0	25	k $\Omega$	

(1) Unless otherwise noted, 10 k $\Omega$  resistor placed between Pin 13 and  $V_{CC}$ , for all tests. ( $R_X$ )

(2) Ground Pin 11 for  $V_{OL}$  Pin 6 or  $V_{OH}$  Pin 8 or  $I_{OS}$  Pin 8. Open Pin 11 for  $V_{OL}$  Pin 8 or  $V_{OH}$  Pin 6 or  $I_{OS}$  Pin 6.

(3) Pulse Test to determine  $V_{IH}$  and  $V_{IL}$  (Min  $t_w$  40 ns).