

# 4-INPUT/4-OUTPUT ADDRESSABLE I/O PORT

**8X382**

## FEATURES

- Bidirectional 8-bit MicroController ( $\overline{IV}$ ) bus
- User bus—four input bits and four output bits
- Independent bus operation
- Synchronous user data input
- Programmed MicroController port address
- Three-state TTL outputs with high-drive capabilities
- Power-up to predetermined logic state
- Directly compatible with 8X305 or 8X300 MicroControllers
- Single +5V supply
- 0.4 inch 24-pin DIP

## PRODUCT DESCRIPTION

The 8X382 I/O Port is an addressable, three-state device designed for use as an interface element in systems that use TTL-compatible busses. Typically, the 8X382 is used with the 8X305 MicroController and its associated Interface Vector ( $\overline{IV}$ ) bus; however, it can also be used with the 8X300 MicroController or an equivalent microprocessor. The 8X382 is functionally the same and pin-for-pin compatible with the older 8X42; however, the new port features better performance, increased drive current, and improved programming procedures.

As shown in the logic diagram of Figure 1, the I/O port

consists of eight data latches—bits 0 through 7. These latches are accessed through either of two busses—an 8-bit bidirectional  $\overline{IV}$  bus connected to the MicroController and a User Data (UD) bus consisting of four dedicated inputs (bits UD0 through UD3) and four dedicated outputs (bits UD4 through UD7). All eight bits may be read from or four data bits ( $\overline{IV}4$ – $\overline{IV}7$ ) can be written into via the  $\overline{IV}$  bus; eight bits of I/O address can be written from the  $\overline{IV}$  bus. Separate controls are provided for each bus and both busses operate independently. The I/O data latches are transparent, in that, when either bus is enabled for input, all transitions in input data are propagated to the other bus, if that bus is enabled for output.

The 8X382 is available with preprogrammed addresses (0<sub>10</sub> through 255<sub>10</sub>); it can also be field-programmed over the same address range. Input/output operations can begin once the I/O port is selected and appropriate control signals are generated. Port selection is implemented by putting the I/O port address (0<sub>10</sub>–255<sub>10</sub>) on the  $\overline{IV}$  bus; once selected, the I/O port remains selected until a different "port address" is put on the bus. Thus, software overhead is minimized. Data is accessible on the UD bus at all times. A Master Enable ( $\overline{ME}$ ) input, which is typically connected to the Left Bank ( $\overline{LB}$ ) or Right Bank ( $\overline{RB}$ ) output of the MicroController, provides the capability of organizing the  $\overline{IV}$  bus into two separate and independent banks of I/O devices.

## 8X382 PACKAGE and PIN DESIGNATIONS

N, I PACKAGE		PIN NO.	IDENTIFIER	FUNCTION
		1-4	UD7-UD4	Three-state, dedicated output lines for user data, UD7 corresponds to $\overline{IV}7$
		5-8	UD3-UD0	Dedicated input lines for user data, UD0 corresponds to $\overline{IV}0$
		9	$\overline{UOC}$	User Output Control—active low input to enable data output to UD4-UD7
		10	$\overline{UIC}$	User Input Control—active low input to enable data input to UD0-UD3
		11	$\overline{ME}$	Master Enable—active low input to enable the $\overline{IV}$ bus for data input, data output, or $\overline{IV}$ address selection/deselection, UD-bus operations are unaffected
		12	GND	Ground
		13	MCLK	Master Clock—active high input (from MicroController) used to strobe data into data latches from the $\overline{IV}$ bus and bits UD0-UD3 of the UD bus, MCLK also synchronizes $\overline{IV}$ address selection
		14	SC	Select Command—active high input (from MicroController) to enable $\overline{IV}$ address input from the $\overline{IV}$ bus for device selection
		15	WC	Write Command—active high (from MicroController) to enable the writing of data into the data latches from the $\overline{IV}$ bus, provided $\overline{UIC}$ is not low
		16-23	$\overline{IV}0$ - $\overline{IV}7$	Interface Vector (Input/Output Bus)—three-state, bidirectional, data bus, $\overline{IV}0$ corresponds to UD0
		24	Vcc	Supply Voltage

**ORDER NUMBERS**  
 N8X382N, N8X382I  
 S8X382I/883B, 8X382I/883C

# 4-INPUT/4-OUTPUT ADDRESSABLE I/O PORT

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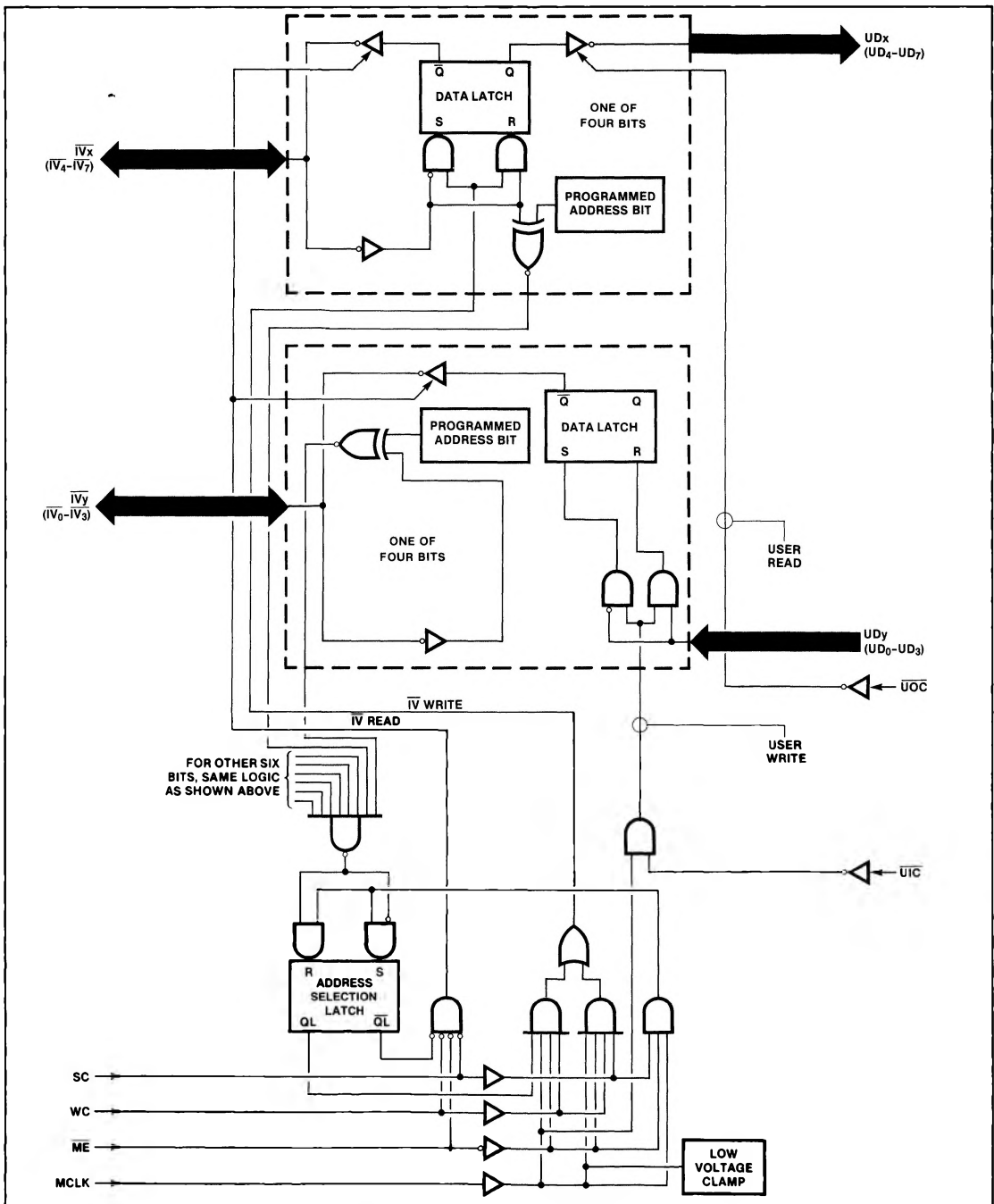


Figure 1. Logic Diagram for 8X382 I/O Port

**FUNCTIONAL OPERATION**

**UD Bus Control**

As shown in Table 1, the User Data-bus interface is controlled by the  $\overline{UIC}$  and  $\overline{UOC}$  inputs. Data input to UD0-UD3 is synchronous with MCLK, that is, with  $\overline{UIC}$  low, information is written into the data latches only when MCLK is high. The output drivers of UD4-UD7 bus are enabled when  $\overline{UOC}$  is low

**Table 1. INPUT/OUTPUT CONTROL OF UD BUS**

UIC	UOC	MCLK	FUNCTION OF UD BUS	
			UD0-UD3	UD4-UD7
H	L	X	Inactive	Output Data
L	X	H	Input Data	Inactive
L	X	L	Inactive	Inactive
H	H	X	Inactive	Inactive

X = don't care

**IV Bus Control**

Input/output control of the  $\overline{IV}$  bus is shown in Table 2; this bus is controlled by SC, WC,  $\overline{ME}$ , MCLK and the current state of an internal address selection latch. The address selection latch in the I/O port stores the result of the most recent  $\overline{IV}$  address selection. The latch is set when the internally preprogrammed address of the port matches the address on the  $\overline{IV}$  bus during an address-selection operation (SC=MCLK=High/WC=Low). The latch is cleared when the two 8-bit address patterns are in disagreement. The  $\overline{IV}$  bus can transfer data only when the selection latch is set. The MicroController Left Bank ( $\overline{LB}$ ) and Right Bank ( $\overline{RB}$ ) outputs can control the  $\overline{ME}$  inputs for two banks of I/O devices, thus, acting as ninth address bit.

Data is written into the data latches of a selected device from the  $\overline{IV}$  bus when WC = MCLK = High and  $\overline{ME}$  = Low. Output drivers on the  $\overline{IV}$  bus of the device with the address latch set are enabled with  $\overline{ME}$ , WC, and SC low. With SC and WC both high (shaded entry of Table 2), the bit pattern present on  $\overline{IV0-IV7}$  is interpreted as both input data ( $\overline{IV4-IV7}$  only) and  $\overline{IV}$  address. The data in  $\overline{IV4-IV7}$  is latched in whether or not the I/O port has been previously selected. If the preprogrammed address of the I/O port matches the bit pattern on  $\overline{IV0-IV7}$  when SC and WC are both high, the selection latch is set; otherwise, it is reset. (Note. *The MicroController never drives both SC and WC high at the same time.*)

**Table 2. INPUT/OUTPUT CONTROL OF IV BUS**

$\overline{ME}$	SC	WC	MCLK	SEL LATCH	FUNCTION OF IV BUS
L	L	L	X	Set	Output Data
L	L	H	H	Set	Input Data ( $\overline{IV4-IV7}$ only)
L	H	L	H	X	Input Address*
L	H	H	H	X	Input Data ( $\overline{IV4-IV7}$ only) and address*
L	X	H	L	X	Inactive
L	H	X	L	X	Inactive
L	L	X	X	Not set	Inactive
H	X	X	X	X	Inactive

X = don't care

\* Selection latch is updated

**Bus Logic Levels**

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note. A logic "1" in MicroController software corresponds to a high level on the UD bus even though the IV bus is inverted). The 8X382 wakes up in the unselected state with all data bits latched at the "logic 1" level (UD bus outputs high if enabled).

**ADDRESS PROGRAMMING AND ADDRESS PROTECT**

**Programming Procedures**

The 8X382 can be programmed to respond to any address within a range of 0<sub>10</sub> through 255<sub>10</sub>. In an unprogrammed state, low level ( $\leq 0.8V$ ) inputs on all  $\overline{IV}$  bus lines (address 255<sub>10</sub>) will select the device. To program a given address bit to match a high level ( $\geq 2.0V$ ) input on the corresponding  $\overline{IV}$  pin (a logical "0" to the MicroController), the counterpart UD-bus pin must be pulsed according to Table 3 and the following procedures:

- Step 1: Set all control inputs to the inactive state— $\overline{UIC} = \overline{UOC} = \overline{ME} = V_{CC}$  and  $SC = WC = MCLK = GND$ ; leave the UD and  $\overline{IV}$  bus pins open.
- Step 2: Increase  $V_{CC}$  to  $V_{CCP}$ .
- Step 3: After  $V_{CC}$  has stabilized, apply a single programming pulse (Figure 2) to the user-bus bit that corresponds to the desired high-level  $\overline{IV}$  address bit. The I/O port is programmed from the user bus (UD0-UD7) for addressing from the MicroController bus ( $\overline{IV0-IV7}$ ).

**Table 3. PROGRAMMING SPECIFICATIONS**

PARAMETERS	LIMITS			UNITS	
	Min	Typ	Max		
$V_{CCP}$ — Programming supply voltage:	Address	8.75	9.0	9.25	V
	Protect		0		V
Maximum time $V_{CCP} > 5.25V$			1.0		Sec
Programming voltage:	Address	8.75	9.0	9.25	V
	Protect	8.75		9.25	V
Programming current:	Address			5	mA
	Protect			50	mA
$t_r$ — Programming pulse rise time:	Address	10		100	$\mu S$
	Protect	10		100	$\mu S$
$t_w$ — Programming pulse width	0.5		1.0		mS

- Step 4: Return  $V_{CC}$  to 0-volts. (Note. *If the programming of all address bits is completed in less than 1-second,  $V_{CC}$  can remain at 9.0-volts for the required interval of time.*)

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- Step 5: Steps 1 through 3 are applicable to the programming of each address bit that requires a high-level IV match.
- Step 6: To verify that the address is properly programmed, return  $V_{CC}$  to +5V, set  $\overline{IV0}$ - $\overline{IV7}$  to the desired (inverted) binary address pattern, set  $\overline{ME} = \overline{WC} = \text{Low}$  and  $\overline{SC} = \overline{MCLK} = \text{High}$ . If there are no programming errors, subsequent data written from  $\overline{IV4}$ - $\overline{IV7}$  ( $\overline{WC} = \text{High}$ ) will appear inverted on UD4-UD7.

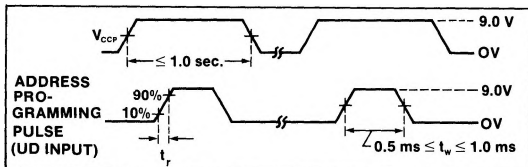


Figure 2. Address Programming Pulse

### Address Protect

After programming the I/O Port, steps should be taken to isolate the address circuits and make these circuits permanently immune to further change.

- Step 1: Set  $V_{CC}$  and all control inputs to 0-volts ( $\overline{VIC} = \overline{UOC} = \overline{ME} = \overline{SC} = \overline{WC} = \overline{MCLK} = \overline{GND} = 0.0V$ );  $\overline{IV0}$ - $\overline{IV7} = \text{open circuit}$ .
- Step 2: Taking one pin at a time, apply a protect programming pulse (Figure 3) to each user-bus bit (UD0-UD7)—refer to Table 3 for min/max specifications pertaining to voltage and current.
- Step 3: Verify that the address circuits for each bit is isolated by applying 9-volts, in turn, to each user-bus pin (UD0-UD7) and measuring less than 200 microamperes of input current. (Note. Setup conditions are the same as those in Step 1.)

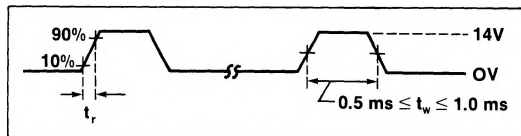


Figure 3. Protect Programming Pulse

## DC ELECTRICAL CHARACTERISTICS

COMMERCIAL:  $4.75V \leq V_{CC} \leq 5.25V$ ,  $0^\circ C \leq T_A \leq 70^\circ C$   
 MILITARY:  $4.5V \leq V_{CC} \leq 5.5V$ ,  $-55^\circ C \leq T_C \leq 125^\circ C$

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
$V_{CC}$ Power supply voltage <sup>3</sup>	+7	Vdc
$V_{IN}$ Input voltage <sup>3</sup>	+5	Vdc
$T_{STG}$ Storage temperature range	-65 to +150	$^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
		Min	Typ	Max	Min	Typ	Max	
$V_{CC}$ Supply Voltage		4.75	5	5.25	4.5	5	5.5	V
$V_{IH}$ High Level Input Voltage		2.0			2.0			V
$V_{IL}$ Low Level Input Voltage				0.8			0.8	V
$V_{CL}$ Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -10\text{mA}$			-1.5			-1.5	V
$I_{IH}$ High Level Input Current <sup>1</sup>	$V_{CC} = \text{Max}$ , $V_{IH} = 2.7V$		5.0	100		5.0	100	$\mu A$
$I_{IL}$ Low Level Input Current <sup>1</sup>	$V_{CC} = \text{Max}$ , $V_{IL} = 0.5V$		-350	-550		-350	-550	$\mu A$
$I_{OZH}$ High-Z State Output Current—High Level <sup>4</sup>	$V_{CC} = \text{Max}$ , $V_{OH} = 2.5V$			100			100	$\mu A$
$I_{OZL}$ High-Z State Output Current—Low Level <sup>4</sup>	$V_{CC} = \text{Max}$ , $V_{OL} = 0.5V$			-100			-100	$\mu A$
$V_{OL}$ Low Level Output Voltage IV Bus ( $\overline{IV0}$ - $\overline{IV7}$ ) User Bus (UD4-UD7)	$V_{CC} = \text{Min}$ ; $I_{OL} = 16\text{mA}$			0.55			0.55	V
	$V_{CC} = \text{Min}$ , $I_{OL} = 24\text{mA}$			0.55			0.55	V
$V_{OH}$ High Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OH} = -3.2\text{mA}$	2.4			2.4			V
$I_{OS}$ Short Circuit Output Current <sup>2</sup> IV Bus ( $\overline{IV0}$ - $\overline{IV7}$ ) UD Bus (UD4-UD7)	$V_{CC} = \text{Max}$	-20			-20			mA
	$V_{CC} = \text{Max}$	-10			-10			mA
$I_{CC}$ Supply Current	$V_{CC} = \text{Max}$ , $\overline{ME} = \overline{UOC} = V_{CC}$		90	150		90	150	mA

Notes

- 1 The input current includes the Three-state leakage current of the output driver on the data lines
- 2 Only one output may be shorted at a time
- 3 These limits do not apply during address programming
- 4 Applies only to pins UD4-UD7

# 4-INPUT/4-OUTPUT ADDRESSABLE I/O PORT

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## AC ELECTRICAL CHARACTERISTICS

COMMERCIAL:  $4.75V \leq V_{CC} \leq 5.25V$ ,  $0^\circ C \leq T_A \leq 70^\circ C$

MILITARY:  $4.5V \leq V_{CC} \leq 5.5V$ ,  $-55^\circ C \leq T_C \leq 125^\circ C$

LOADING: See TEST LOADING CIRCUITS

PARAMETER	REFERENCES <sup>1</sup>		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
	FROM	TO		Min	Typ	Max	Min	Typ	Max	
<b>Pulse Widths:</b>										
tw1 Clock High	↑MCLK	↓MCLK		35			35			ns
tw2 User Input Control	↓UIC	↑UIC	MCLK = High	35			35			ns
<b>Propagation Delays:</b>										
tpD1 UD Propagation Delay	UD0-3	$\overline{IV}$ 0-3	MCLK = High SC = WC = ME = UIC = Low			30			30	ns
tpD2 UD Clock Delay	↑MCLK	$\overline{IV}$ 0-3	UD0-3 = Stable, MCLK = High; SC = WC = ME = UIC = Low			50			50	ns
tpD3 UD Input Delay	↓UIC	$\overline{IV}$ 0-3	UD0-3 = Stable; MCLK = High, SC = WC = ME = Low			50			50	ns
tpD4 $\overline{IV}$ Data Propagation Delay	$\overline{IV}$ 4-7	UD4-7	MCLK = WC = High; ME = UOC = SC = Low			45			45	ns
tpD5 $\overline{IV}$ Data Clock Delay	↑MCLK	UD4-7	$\overline{IV}$ 4-7 = Stable, WC = High; ME = UOC = SC = Low			55			55	ns
<b>Output Enable Timing:</b>										
toE1 UD Output Enable	↓UOC	UD4-7				30			30	ns
toE3 $\overline{IV}$ Data Master Enable	↓ME	$\overline{IV}$	WC = SC = Low			22			25	ns
toE5 $\overline{IV}$ Data Write Recovery	↓WC	$\overline{IV}$	SC = ME = Low			25			25	ns
toE6 $\overline{IV}$ Data Select Recovery	↓SC	$\overline{IV}$	WC = ME = Low			25			25	ns
<b>Output Disable Timing:</b>										
toD1 UD Output Disable	↑UOC	UD4-7				25			25	ns
toD3 <sup>2</sup> $\overline{IV}$ Data Master Disable	↑ME	$\overline{IV}$	WC = SC = Low			25			25	ns
toD5 <sup>2</sup> $\overline{IV}$ Data Write Override	↑WC	$\overline{IV}$	SC = ME = Low			20			20	ns
toD6 <sup>2</sup> $\overline{IV}$ Data Select Override	↑SC	$\overline{IV}$	WC = ME = Low			20			20	ns
<b>Setup Times:</b>										
ts1 UD Clock Setup Time	UD0-3	↓MCLK	$\overline{UIC}$ = Low	15			15			ns
ts2 UD Control Setup Time	UD0-3	↑UIC	MCLK = High	15			15			ns
ts3 User Input Control Setup Time	↓UIC	↓MCLK		25			25			ns
ts4 $\overline{IV}$ Data Setup Time	$\overline{IV}$	↓MCLK	WC = High or SC = High; ME = Low,	35			35			ns
ts5 <sup>3</sup> $\overline{IV}$ Master Enable Setup Time	↓ME	↓MCLK	WC = High or SC = High	30			30			ns
ts6 $\overline{IV}$ Write Control Setup Time	↑WC	↓MCLK	SC = ME = Low;	30			30			ns
ts7 $\overline{IV}$ Select Control Setup Time	↑SC	↓MCLK	WC = ME = Low	30			30			ns

**4-INPUT/4-OUTPUT ADDRESSABLE I/O PORT****8X382****AC ELECTRICAL CHARACTERISTICS (Cont'd)**

PARAMETER	REFERENCES		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
	FROM	TO		Min	Typ	Max	Min	Typ	Max	
<b>Hold Times:</b> t <sub>H1</sub> UD Clock Hold Time	↓MCLK	UD	$\overline{UIC} = \text{Low}$	15			15			ns
t <sub>H2</sub> UD Control Hold Time	↑ $\overline{UIC}$	UD	MCLK = High	15			15			ns
t <sub>H3</sub> User Input Control Hold Time	↓MCLK	↑ $\overline{UIC}$		0			0			ns
t <sub>H4</sub> Data Hold Time	↓MCLK	$\overline{IV}$	WC = High or SC = High, $\overline{ME} = \text{Low}$	5			5			ns
t <sub>H5</sub> <sup>3</sup> Master Enable Hold Time	↓MCLK	↑ $\overline{ME}$	WC = High or SC = High;	0			0			ns
t <sub>H6</sub> $\overline{IV}$ Write Control Hold Time	↑MCLK	↓WC	SC = $\overline{ME} = \text{Low}$	0			0			ns
t <sub>H7</sub> $\overline{IV}$ Select Control Hold Time	↑MCLK	↓SC	WC = $\overline{ME} = \text{Low}$	0			0			ns

## Notes:

- 1 All measurements to the  $\overline{IV}$  bus assumes the address selection latch is set
- 2 These parameters are measured with a capacitive loading of 50 pF and represent the output driver turn-off time.
- 3 If  $\overline{ME}$  is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port

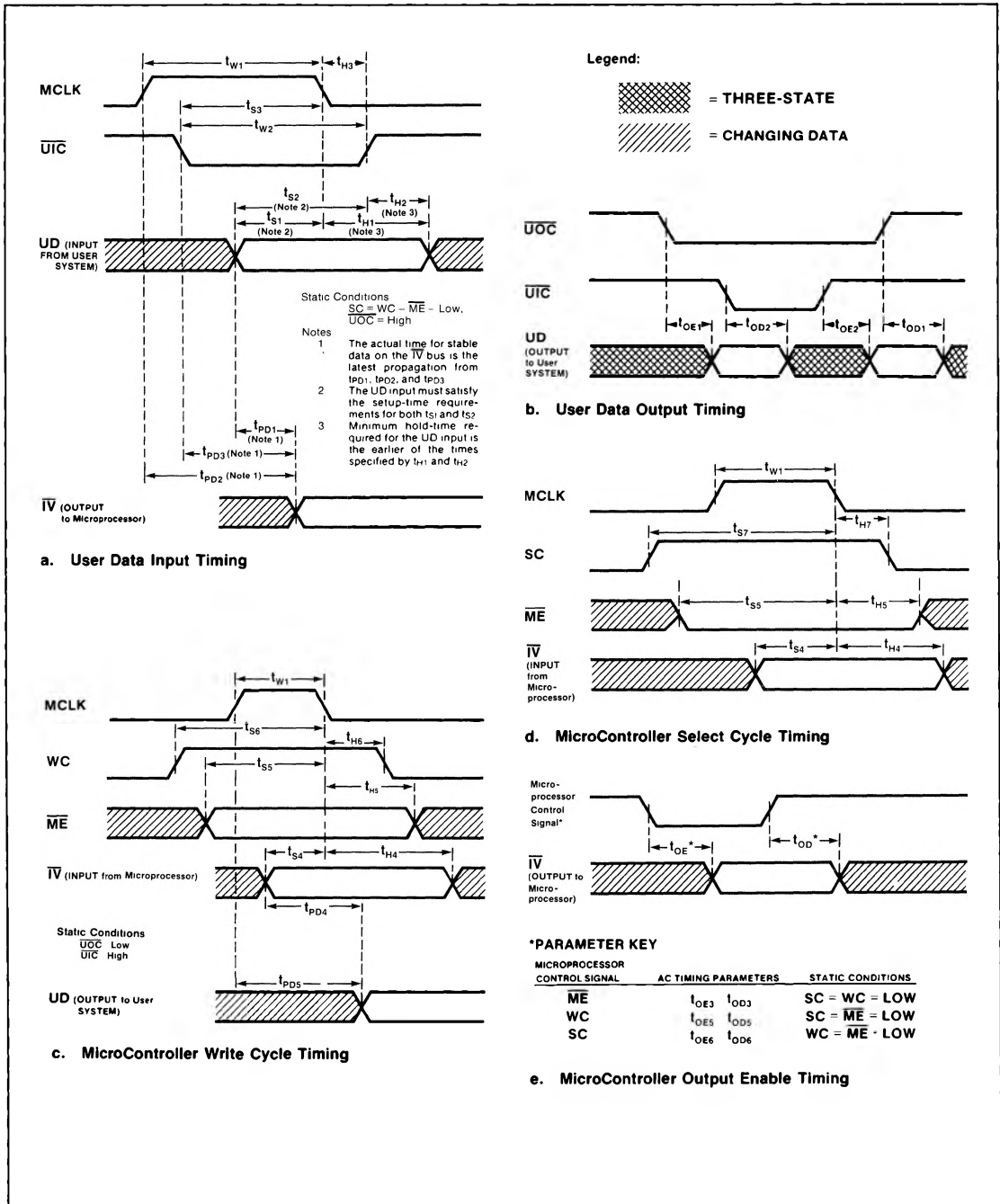
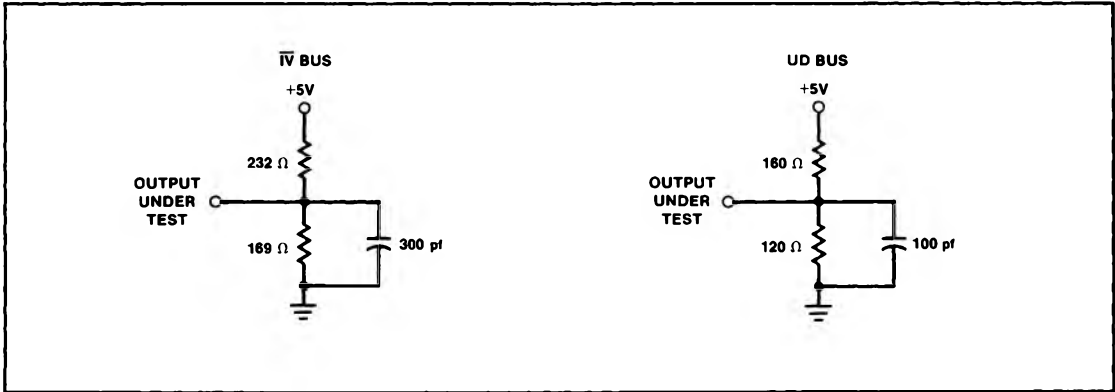


Figure 4. Timing Diagrams

TEST LOADING CIRCUITS



**APPLICATIONS**

When compared to other MicroController ports in the 8X370 series, the 8X382 has some unique features that provide real design advantages in certain applications. Connection of the I/O port to the MicroController is simple and straightforward in that like pin names are tied together. The system designer must also decide on which bank of the MicroController to place the 8X382 and then connect the  $\overline{ME}$  pin of the port to either the LB (Left Bank) or RB (Right Bank) of the MicroController.

The 8X382 is unique because it can be used for both dedicated input and output operations. In the system

shown below, the user interface requires nine (9) dedicated inputs and eleven (11) dedicated outputs. Observe that by using an 8X382, the problem is solved by three devices, whereas, four 8X372 ports are required for the same solution.

Another important use of the 8X382 is in implementing a handshake interface. Since both input and output bits reside in the same port, I/O operations can be performed without port re-addressing. Users may also find the 8X382 an advantage in the layout of Printed Circuit boards, since random control/status signals can be grouped within the same device position.

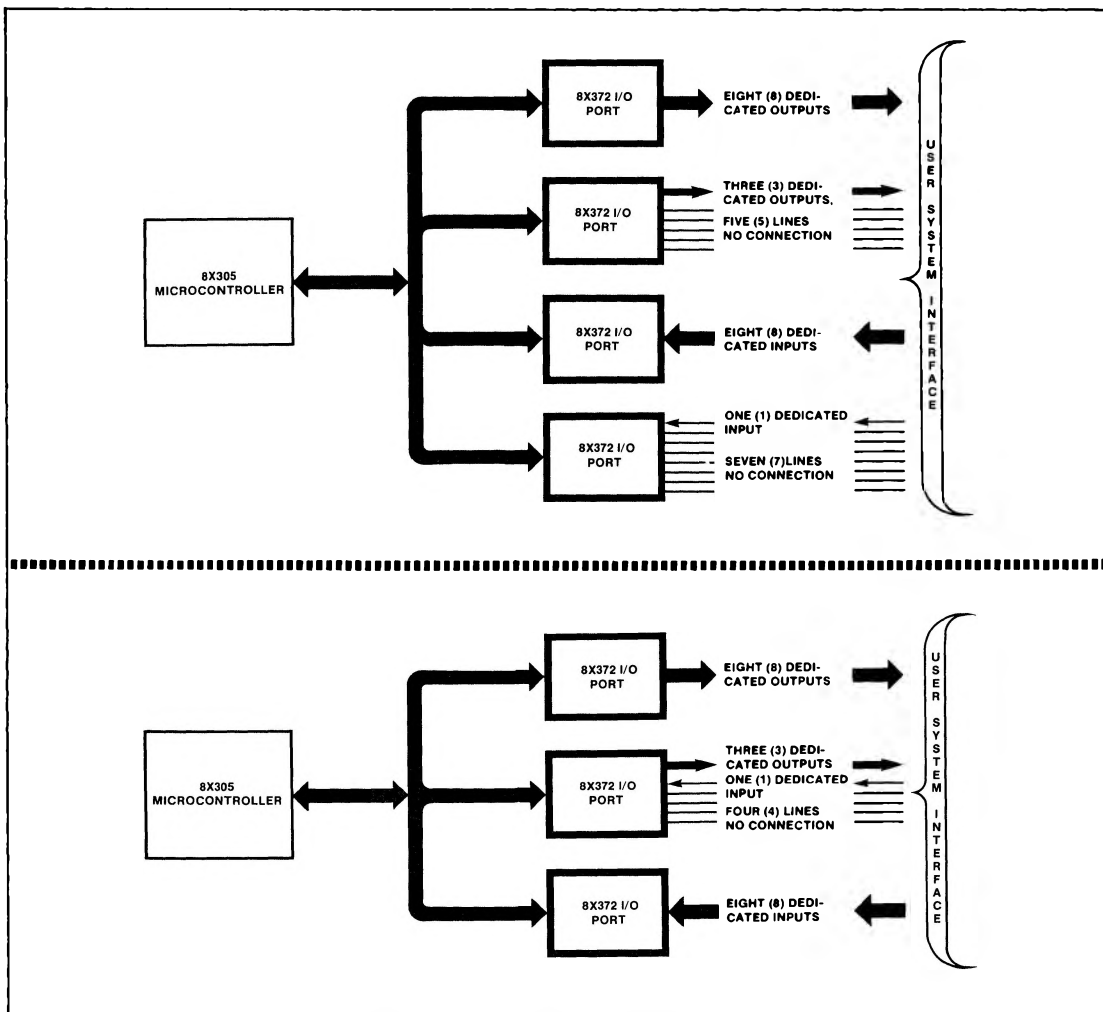


Figure 5. Logic Diagram for 8X382 I/O Port