DESCRIPTION

The Bus Expander is specifically designed to increase the I/O capability of 8X300 systems previously limited by fanout considerations. The bus expander serves as a buffer between the 8X300 and blocks of I/O devices. Each bus expander can buffer a block of 16 I/O ports while only adding a single load to the 8X300.

FEATURES

- **15ns max propagation delay**
- **Bidirectional**
- **Three-state outputs on both ports**
- **Pre-programmed address range**

APPLICATIONS

The 8T39 Bus Expander is designed to be used with the 8X300 microprocessor to allow increased I/O capability in those systems previously limited by fanout considerations. Figure 1 shows a typical arrangement of the bus expander in an 8X300 system. Each expander services I/O ports whose address is within the range of the expander. Other I/O ports or working storage may be directly connected to the bus as shown.

The bus expander is not limited to use with the 8X300, but may be applied in any system which uses a combined address/data bus.

8T39 ADDRESSING

During normal operation of the 8X300 when an I/O port address is being sent on the IV Bus (SC is high), the I/O port will examine all eight bits of the microprocessor bus for an address compare. Since the 8T39 is used to buffer blocks of I/O ports, only the four most significant bits are examined by the 8T39 for an address compare.

Note that redundant addresses are not programmed into separate devices. Rather, a discrete device (such as the 8T39-03) may be wired for any address requiring two 1 bits and two 0 bits in the address. The various address ranges for this same device are obtained by permuting the high order (DI0 and DO0 are MSB) data lines accordingly. Both input and output lines must be redefined in order to maintain data and address integrity on the extended bus. Table 1 summarizes the 8T39 addressing.

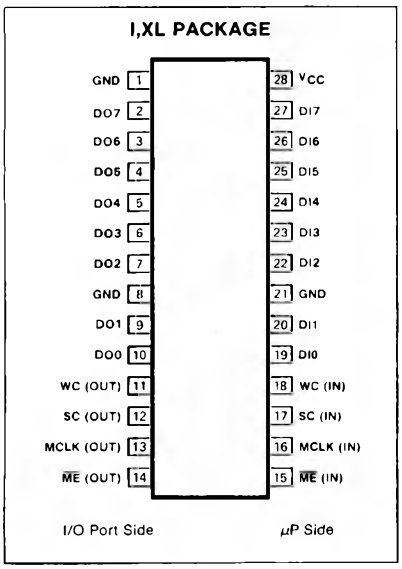
Address functions are specified with the convention that bit 0 is the MSB and bit 7 is the LSB. The DI microprocessor bus address decoding is active low.

FUNCTIONAL DESCRIPTION

The Bus Expander contains eight sets of non-inverting bidirectional tri-state drivers for the bus data bits, four non-inverting unidirectional drivers for I/O port control, and necessary control logic. The control logic is required to maintain the proper directional transfer of bus data as dictated by the states of the I/O port control signals and the currently enabled I/O port. Each bus expander is programmed during manufacturing to respond to a specific block of I/O port addresses. Only I/O ports with addresses in the range of a given bus expander may be connected to that expander. A bus expander may be used on either left bank or right bank. Multiple expanders on the same bank must have different address ranges; however, expanders with the same address range can be connected if they are on different banks. Systems may be configured with I/O ports connected directly to the 8X300, as well as I/O ports connected through a bus expander; however, no unbuffered I/O port may have an address within the span of a bus expander on the same bank.

Addition of bus expanders may impact system cycle time due to the added delay in the data path. For the purposes of calculating allowable cycle time as described in the 8X300 data sheet, the bus expander delays may be considered additive to the I/O port delays so that a buffered I/O port simply appears as a slower I/O port.

PIN CONFIGURATION



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
2-7,9,10	DO0-DO7	I/O port data bus	Active low, three-state
11	WC(OUT)	Write command output	Active high
12	SC(OUT)	Select command output	Active high
13	MCLK(OUT)	Master clock output	Acitve high
14	$\overline{ME}$(OUT)	Master enable output	Active low
15	$\overline{ME}$(IN)	Master enable input	Active low
16	MCLK(IN)	Master clock input	Active high
17	SC(IN)	Select command output	Active high
18	WC(IN)	Write command output	Active high
19,20,22-27	DI0-DI7	Microprocessor data bus	Active low, three-state
1,8,21	GND	Ground	
28	V_{CC}	+5 volt supply	

PART TYPE	ADDRESS PATTERN MSB(0) LSB(7)	ADDRESS BLOCKS Octal
8T39-00	0000XXXX	0-17
8T39-01	0001XXXX	20-37, 40-57, 100-117, 200-217
8T39-03	0011XXXX	60-77, 120-137, 220-237, 140-157, 240-257, 300-317
8T39-07	0111XXXX	160-177, 260-277, 320-337, 340-357
8T39-17	1111XXXX	360-377

Table 1 8T39 ADDRESSING SUMMARY

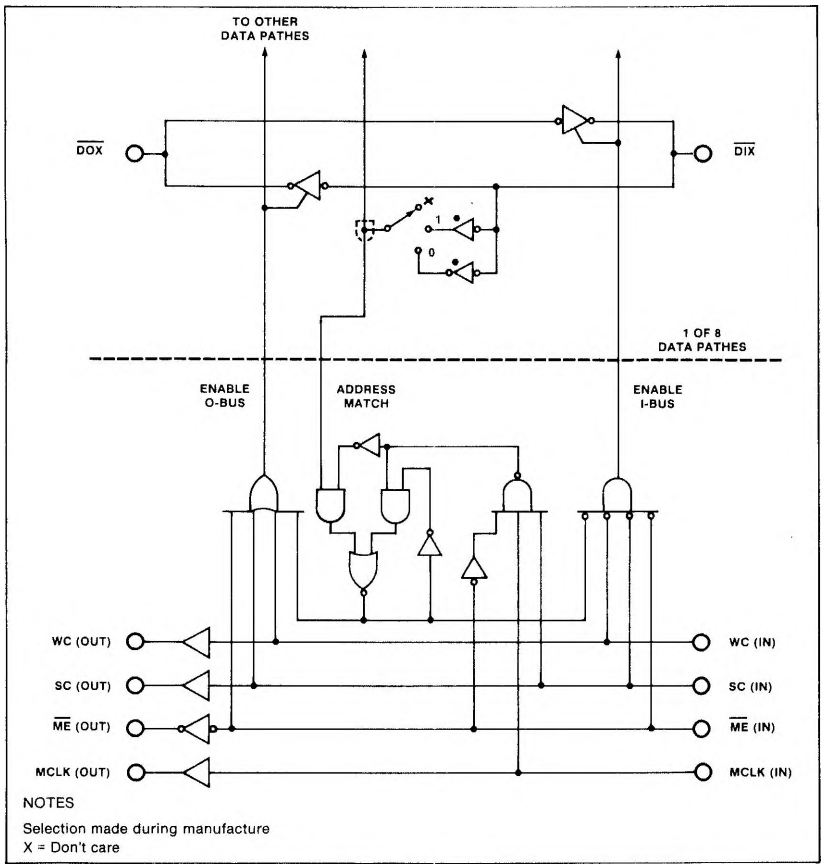
TRUTH TABLE

$\overline{ME}$	SC	WC	MCLK	SELECT LATCH	DATA TRANSFER DIRECTION	ADDRESS* COMPARISON
L	L	L	X	Set	DI Bus ← DO Bus	No
L	L	L	X	Not set	DI Bus → DO Bus	No
L	L	H	X	X	DI Bus → DO Bus	No
L	H	X	L	X	DI Bus → DO Bus	No
L	H	X	H	X	DI Bus → DO Bus	Yes
H	X	X	X	X	DI Bus → DO Bus	No

NOTES

*When an address comparison is made, the select latch is set if the data on the DI Bus is within the manufactured address range of the IV Bus Expander. Otherwise, the select latch is cleared.

FUNCTIONAL BLOCK DIAGRAM



NOTES

Selection made during manufacture

X = Don't care

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

ORDERING INFORMATION

The Bus Expander is ordered by specifying the following part number:

N8T39-XX P

- P = { I - Ceramic Package; XL - Epoxy Package
- Address Range As Determined From Table 1

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage					V
V_{IL}	Low	-5mA at V_{CC} min			.8	
V_{IH}	High		2.0			
V_{IC}	Clamp				-1	
	Output voltage	V_{CC} = 4.75V				V
V_{OL}	Low	I_{OL} = 16mA			.55	
V_{OH}	High	I_{OH} = -3.2mA	2.4			
	Input current	V_{CC} = 5.25V				uA
I_{IL}	Low*	V_{IL} = .5V			-250	
I_{IH}	High*	V_{IH} = 5.25V		< 10	100	
I_{OS}	Short circuit output current	V_{CC} = 4.75V	-40			mA
I_{CC}	Supply current	V_{CC} = 5.25V			200	mA

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C, C_L[1] = 300pF[2]

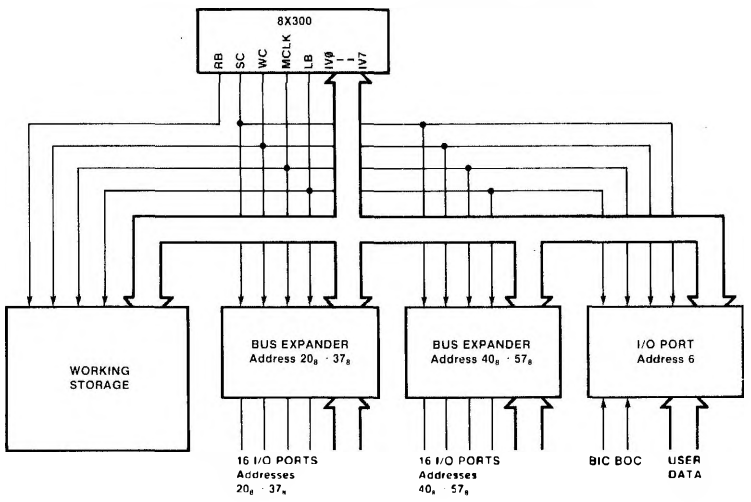
	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_{pd}	Propagation Delay Data	DOX DIX	DIX DOX				15	ns
t_{pd}	Control Propagation Delay	$\overline{ME}$ (out) MCLK (out) SC (out) WC (out)	$\overline{ME}$ (in) MCLK (in) SC (in) WC (in)				15	
t_{oe}	Data Output Enable	DIX DOX	$\overline{ME}$ (in) SC (in) WC (in)		28		56	ns
t_{od}	Data Output Disable	DIX DOX	$\overline{ME}$ (in) SC (in) WC (in)		15			ns
t_{setup}	Adverse Setup Time[3]	DIX DOX	DIX $\overline{ME}$ (in) MCLK (in) SC (in) WC (in)		54			ns
t_{hold}	Address Hold Time[3]	DIX DOX	DIX $\overline{ME}$ (in) MCLK (in) SC (in) WC (in)		3			ns

NOTES

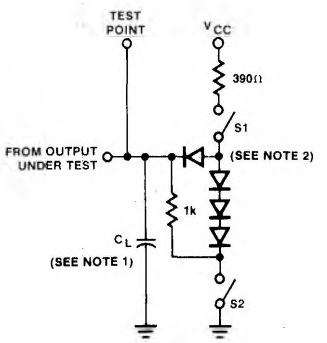
1. Includes tri-state leakage.
2. Minimum clock width ≈ 50ns.
3. All set up and hold times are referenced to the trailing edge of the clocking input MCLK.

TYPICAL APPLICATIONS

USING 2 BUS EXPANDERS TO GIVE 33 I/O PORTS PLUS WORKING STORAGE



TEST LOAD CIRCUIT



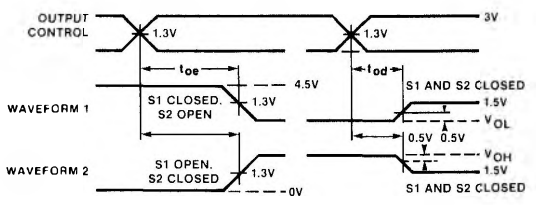
All resistors values are typical and in ohms.

NOTES

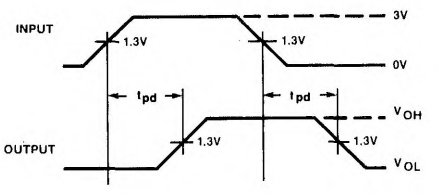
1. C_L includes probe and jig capacitance.
2. All diodes are 1N916 or 1N3064.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TO THREE-STATE OUTPUTS



PROPAGATION DELAY TIMES



PRELIMINARY SPECIFICATION

Manufacturer reserves the right to make design changes and improvements.