ISL GATE ARRAY 8A1864

FEATURES

- **Customer programmable LSI**
- **1740 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **60 Schottky buffers**
- **72 I/O buffers**
- **LS TTL compatible**
- **Standard PNP inputs**
- **8-, or 24-milliamperes output current sink**
- **−55°C to +125°C ambient temperature**
- **4-nanosecond gate speed (typical)**
- **Speed-power product — 0.7 picojoules**
- **40-, 44-, 50- or 68-pin packages**

PRODUCT DESCRIPTION

The 8A1864 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2). Schottky buffers (Figure 3) and LSTTL-compatible I/O cells. Thus, up to 1740 gates and 60 buffers can be interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1864 array is based on a technological subset of LSI called ISL (integrated Schottky Logic). ISL combines the features of Schottky and the density of I^2L Bipolar technologies.

Designing with the 8A1864 is easy and fast, requiring no more than conventional logic design, logic simulation, and coding of metal interconnections between preprocessed logic gates on the array. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting up to 1740 ISL NAND gates, and up to 60 buffers, using two layers of metal routing. Sixty Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 64 LS TTL I/O buffers can be specified. Each 8-milliampere I/O site can be configured as 1-of-6 input/internal buffers or as 1-of-8 output buffers; each 24-milliampere I/O site can also be configured as 1-of-6 input/internal buffers but the output buffer configuration can be 1-of-12. For a transceiver, either I/O site can be connected in combinations of one input and one output buffer.

ORDERING INFORMATION

Contact Local Sales Representative

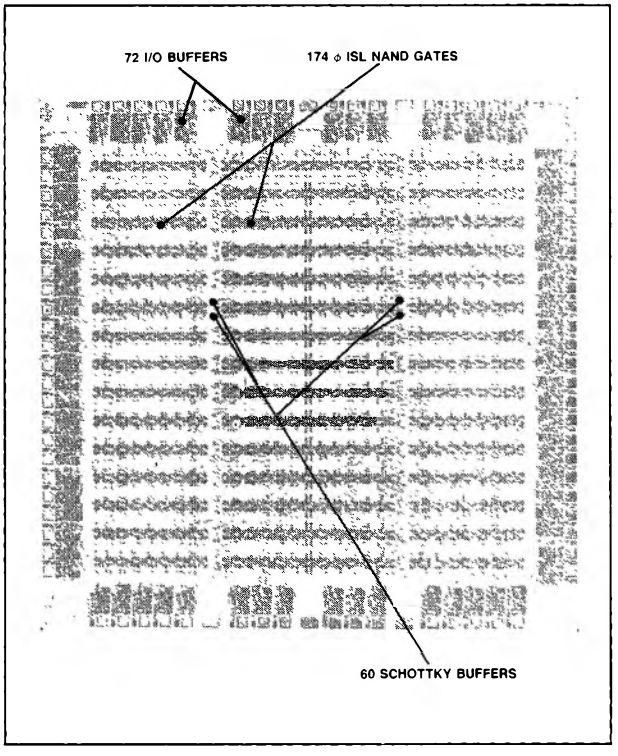

Figure 1. Internal Configuration of 8A1864

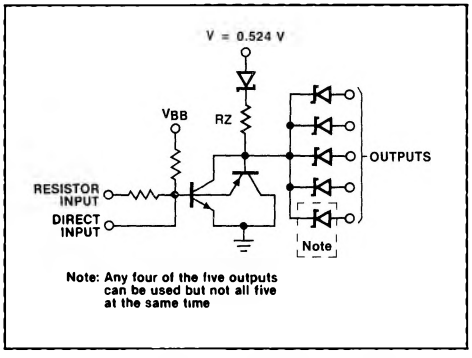

Figure 2. ISL Gate — Schematic Diagram

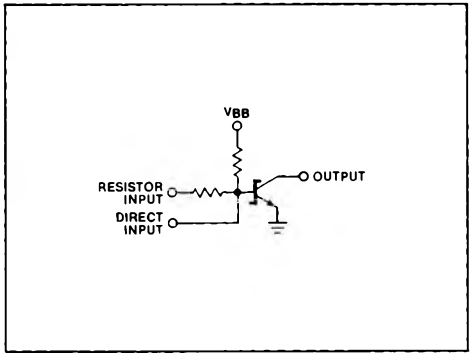

Figure 3. Schottky Buffer — Schematic Diagram