

Document No.	853-0154
ECN No.	86487
Date of Issue	November 11, 1986
Status	Product Specification
Memory Products	

# 82S23 82S123

## 256-bit TTL bipolar PROM

### DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23 and 82S123 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in based organizations.

Ordering information can be found on the following page.

The 82S23 and 82S123 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.

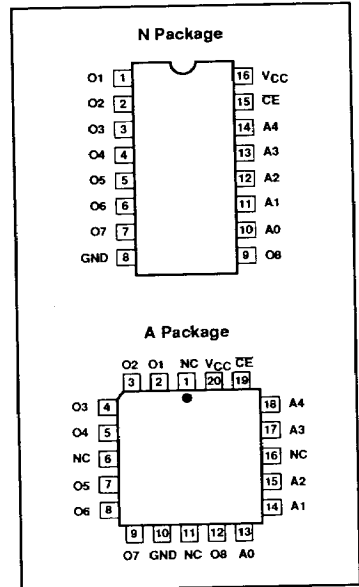
### FEATURES

- Address access time: 50ns max
- Power dissipation: 1.3mW/bit typ
- Input loading: -100µA max
- On-chip address decoding
- One Chip Enable input
- Output options:
  - N82S23: Open Collector
  - N82S123: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

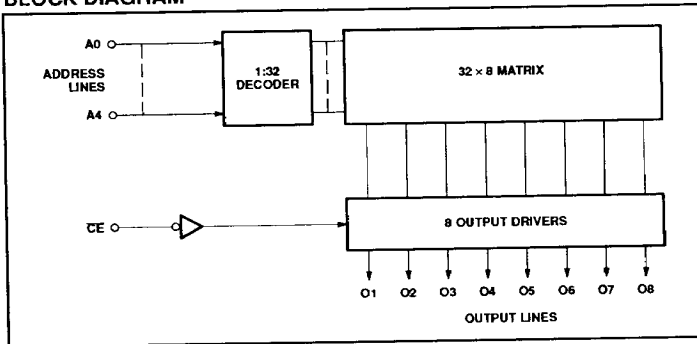
### APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

### PIN CONFIGURATIONS



### BLOCK DIAGRAM



**256-bit TTL bipolar PROM (32 × 8)****82S23 / 82S123****ORDERING INFORMATION**

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N82S23 N, N82S123 N
20-Pin Plastic Leaded Chip Carrier 350mil-square	N82S23 A, N82S123 A

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	+7.0	$V_{DC}$
$V_{IN}$	Input voltage	+5.5	$V_{DC}$
$V_{OH}$	Output voltage High (82S23)	+5.5	$V_{DC}$
$V_O$	Output voltage Off-State (82S123)	+5.5	$V_{DC}$
$T_{amb}$	Operating temperature range	0 to +75	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

**DC ELECTRICAL CHARACTERISTICS**
 $0^{\circ}\text{C} \leq T_{amb} \leq +75^{\circ}\text{C}$ ,  $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1,2</sup>	LIMITS			UNIT
			MIN	TYP <sup>3</sup>	MAX	
<b>Input voltage</b>						
$V_{IL}$	Low	$V_{CC} = 4.75\text{V}$	2.0		0.8	V
$V_{IH}$	High	$V_{CC} = 5.25\text{V}$				
$V_{IC}$	Clamp	$I_{IN} = -12\text{mA}$				
<b>Output voltage</b>						
$V_{OL}$	Low	$CE = \text{Low}$	2.4		0.45	V
$V_{OH}$	High	$I_{OUT} = 16\text{mA}$ $I_{OUT} = -2.0\text{mA}$				
<b>Input current</b>						
$I_{IL}$	Low	$V_{IN} = 0.45\text{V}$			-100	$\mu\text{A}$
$I_{IH}$	High	$V_{IN} = 5.5\text{V}$				
<b>Output current</b>						
$I_{OLK}$	Leakage (82S23)	$CE = \text{High}, V_{OUT} = 5.5\text{V}$	-15		40	$\mu\text{A}$
$I_{OZ}$	Hi-Z state (82S123)	$CE = \text{High}, V_{OUT} = 5.5\text{V}$				
$I_{OS}$	Short circuit (82S123) <sup>4</sup>	$CE = \text{High}, V_{OUT} = 0.5\text{V}$				
<b>Supply current<sup>5</sup></b>						
$I_{CC}$		$V_{CC} = 5.25\text{V}$			96	$\text{mA}$
<b>Capacitance</b>						
$C_{IN}$	Input	$CE = \text{High}, V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$			5	$\text{pF}$
$C_{OUT}$	Output	$V_{OUT} = 2.0\text{V}$			8	$\text{pF}$

**NOTES:**

- Positive current is defined as into the terminal referenced.
- All voltages with respect to network ground terminal.
- Typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = +25^{\circ}\text{C}$ .
- Duration of short circuit should not exceed 1 second.
- Measured with all inputs grounded and all outputs open.

# 256-bit TTL bipolar PROM (32 × 8)

82S23 / 82S123

## AC ELECTRICAL CHARACTERISTICS

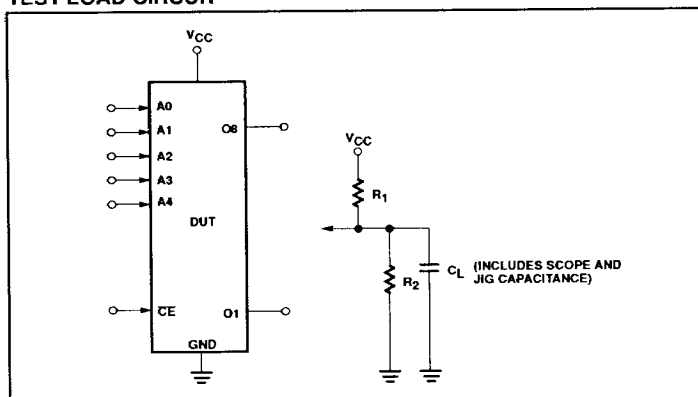
$R_1 = 270\Omega$ ,  $R_2 = 600\Omega$ ,  $C_L = 30\text{pF}$ ,  $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$ ,  $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				MIN	TYP <sup>1</sup>	MAX	
<b>Access time<sup>2</sup></b>							
$t_{AA}$		Output	Address		45	50	ns
$t_{CE}$		Output	Chip Enable			35	ns
<b>Disable time<sup>3</sup></b>							
$t_{CD}$		Output	Chip Disable			35	ns

### NOTES:

1. Typical values are  $V_{\text{CC}} = 5\text{V}$ ,  $T_{\text{amb}} = +25^\circ\text{C}$ .
2. Tested at an address cycle time of  $1\mu\text{s}$ .
3. Measured at a delta of 0.5V from Logic Level with  $R_1 = 750\Omega$ ,  $R_2 = 750\Omega$  and  $C_L = 5\text{pF}$ .

## TEST LOAD CIRCUIT



## VOLTAGE WAVEFORM

