DESCRIPTION

Data is stored in a single storage matrix which is addressed via 2 independent sets of address inputs, designated respectively as Port A and Port B.

Data can be read from memory via either Port A or B, through their respective output sets. However, input data (latched on the leading edge of write enable in the input data latches) is written only in memory locations specified by the address on Port A, regardless of Port B.

When both Port addresses are equal, data from the same location can be read in either or both Port output sets by means of output select lines S_A and S_B. During Write, new data stored in memory is immediately transferred on both Port output sets.

When both Port addresses are different, 2 different locations can be simultaneously read from memory. It is also possible to simultaneously read through Port B while writing new input data through Port A by utilizing the "A_N" address to specify the location of the word to be written, and the "B_N" address to specify the word to be read.

Both devices are ideally suited for high speed accumulator and buffer memories, and can be readily expanded to form larger arrays by means of their output select and write enable lines.

Both the 82S12 and 82S112 are available over the limited temperature range of +10°C to +75°C. Over this temperature range, specify N82S12/82S112F,N.

FEATURES

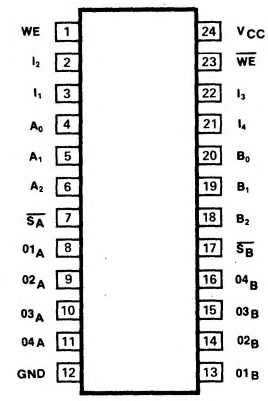
- **Address access time: 40ns max**
- **Write cycle time: 65ns max**
- **Power dissipation: 8.5mW/bit typ**
- **Input loading: −250μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S12 Open collector**
  - **82S112 Tri-state**
- **Non-inverting outputs**
- **Input data latches**
- **Two write enable lines**
- **Separate output enable lines**
- **Output follows data input during write**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Accumulator register**
- **Data routing/shifting**
- **ALU control**
- **Multiprocessor memory management**
- **Bandwidth increase by multi-operand fetch**
- **Communication controllers**
- **I/O data packing/unpacking**
- **Large FIFO memories**

PIN CONFIGURATION

F,N PACKAGE*



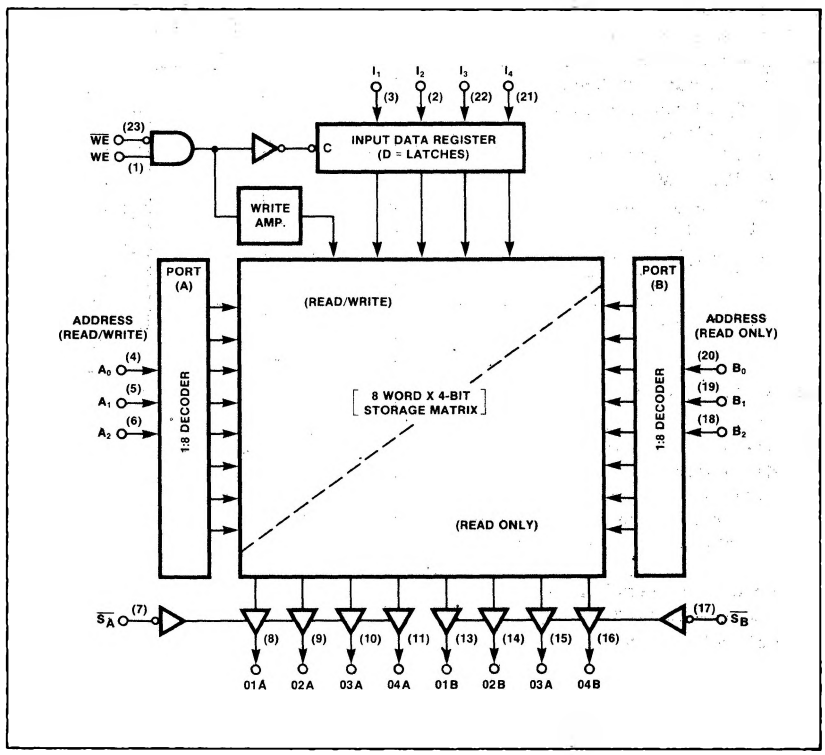
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	WE	$\overline{WE}$	I_N	$\overline{S_A}$	$\overline{S_B}$	PORT ADDRESS	82S12 $(O_N)A$	82S12 $(O_N)B$	82S112 $(O_N)A$	82S112 $(O_N)B$
Disabled				1	1	X	1	1	Hi-Z	Hi-Z
Read	0 or X	X or 1	X	0	1	A = B	Stored Data	1	Stored Data	Hi-Z
				1	0		1	Stored Data	Hi-Z	Stored Data
				0	0		Stored Data	Stored Data	Stored Data	Stored Data
				0	1	A ≠ B	[A_N]	1	[A_N]	Hi-Z
				1	0		1	[B_N]	Hi-Z	[B_N]
				0	0		[A_N]	[B_N]	[A_N]	[B_N]
Write	1	0	1/0	1	1	A = B	1	1	Hi-Z	Hi-Z
				0	1		I_N	1	I_N	Hi-Z
				1	0		1	I_N	Hi-Z	I_N
				0	0		I_N	I_N	I_N	I_N
				1	1	A ≠ B	1	1	Hi-Z	Hi-Z
				0	1		I_N	1	I_N	Hi-Z
				1	0		1	[B_N]	Hi-Z	[B_N]
				0	0		I_N	[B_N]	I_N	[B_N]

X = Don't care
[ ] = Contents of

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S12)	+5.5	
V_O	Off-state (82S112)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $+10°C \le T_A \le 75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER[1]		TEST CONDITIONS	82S12			82S112			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IH}	High[1]	V_{CC} = 5.25V	2			2			
V_{IL}	Low[1]	V_{CC} = 4.75V			0.85			0.85	
V_{IC}	Clamp[1,3]	V_{CC} = 4.75V, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = 4.75V							V
V_{OH}	High[1,4]	I_{OH} = -2mA				2.4			
V_{OL}	Low[1,5]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.45	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		1	25		1	25	
I_{IL}	Low	V_{IN} = 0.45V		-10	-250		-10	-250	
	Output current	V_{CC} = 5.25V							
I_{OLK}	Leakage[6]	V_{OUT} = 5.25V		1	40				μA
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.25V					1	40	μA
		V_{OUT} = 0.45V					-1	-40	
I_{OS}	Short circuit[3,7]	V_{OUT} = 0V				-20		-70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = 5.25V		110	160		110	160	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
V_{OUT}	Output	V_{OUT} = 2.0V		8			8		

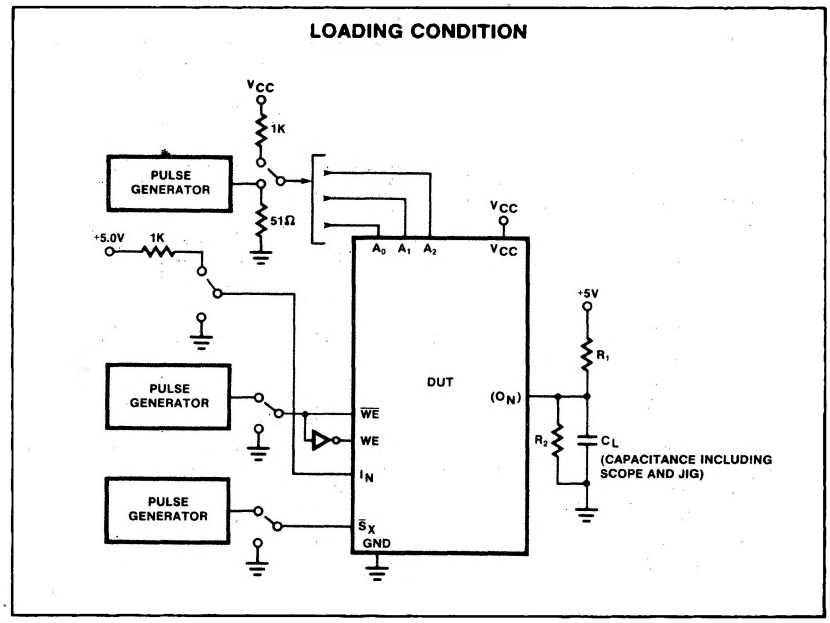
AC ELECTRICAL CHARACTERISTICS $+10°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
	Access time						ns
T_{AA}	Address	Output	Address			40	
T_{SE}	Port select	Output	Output enable			30	
	Disable time						ns
T_{SD}	Port deselect	Output	Output enable			30	
T_{WD}	Valid time	Output	Write enable			40	ns
	Setup and hold time						ns
T_{WSA}	Setup time	Write enable	Address	15	10		
T_{WHA}	Hold time			5	0		
T_{WSD}	Setup time	Write enable	Data in	15			
T_{WHD}	Hold time			10			
	Pulse width						ns
T_{WP}	Write enable			45			

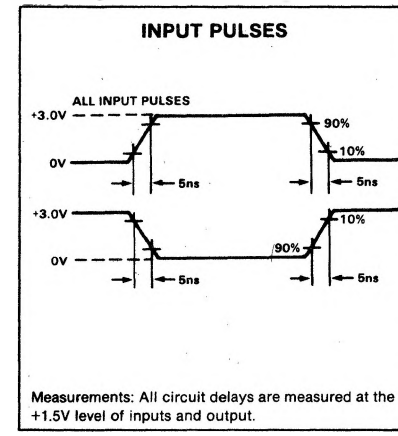
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test one at the time.
4. Measured with V_{IL} applied to $\overline{S_X}$ and a logic high stored.
5. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{S_X}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with all inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

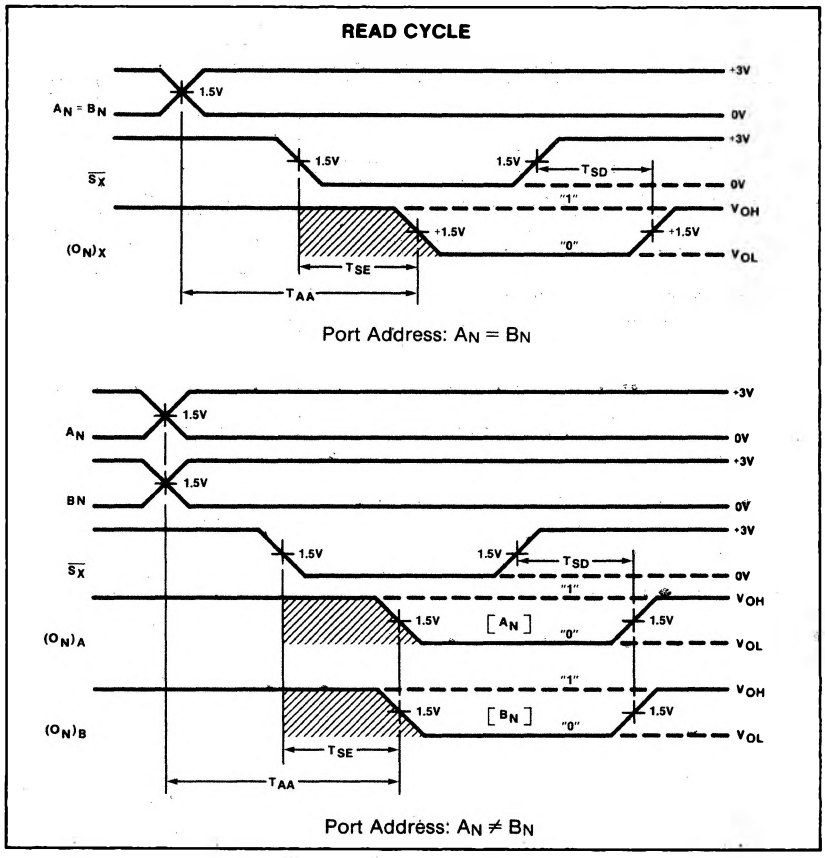


VOLTAGE WAVEFORM



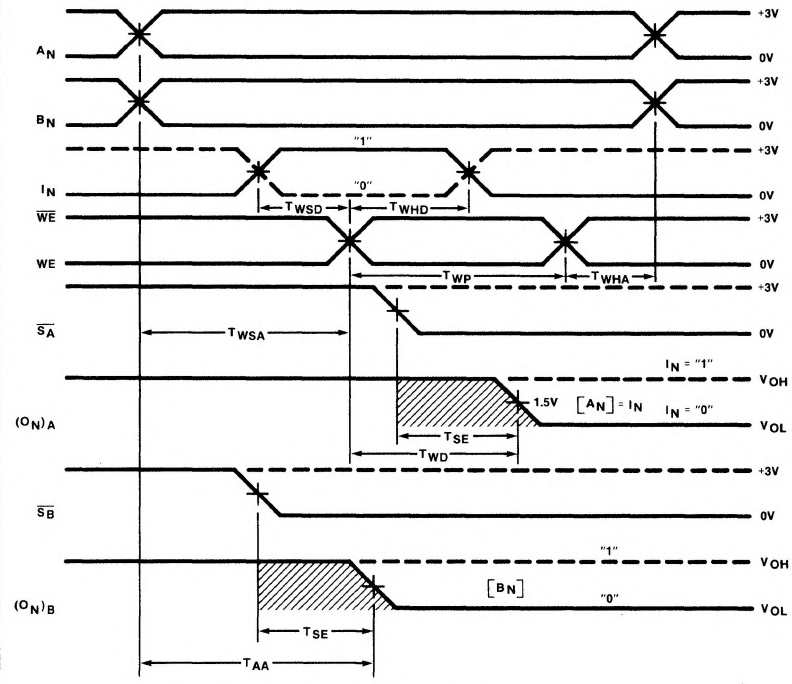
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS



TIMING DIAGRAMS (Cont'd)

SIMULTANEOUS READ/WRITE CYCLE

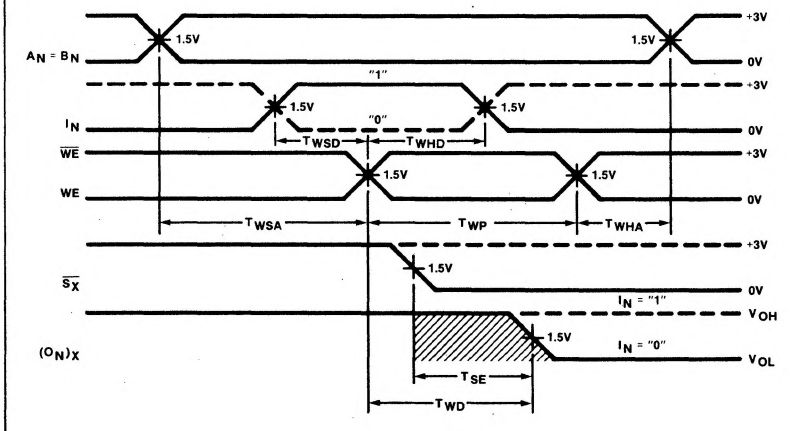


Port Address: $A_N \neq B_N$

A_N = Write

B_N = Read

PORT A WRITE CYCLE



Port Address: $A_N = B_N$

MEMORY TIMING DEFINITIONS

T_{SE}	Delay between beginning of Output Enable low (with Address valid) and when Data Output becomes valid.
T_{SD}	Delay between when Output Enable becomes high and Data Output is in Hi-Z or high state.
T_{AA}	Delay between beginning of valid Address (with Output Enable low) and when Data Output becomes valid.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects the Data Input.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.