

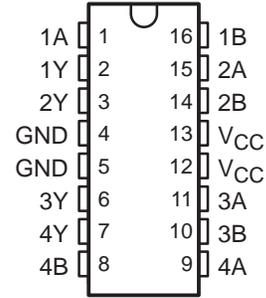
# 74AC11132

## QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT-TRIGGER

SCAS113 – D3482, MARCH 1990 – REVISED APRIL 1993

- Operation From Very Slow Input Transitions
- Temperature-Compensated Threshold Levels
- High Noise Immunity
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Both Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

D OR N PACKAGE  
(TOP VIEW)



### description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. It performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A + B}$  in positive logic.

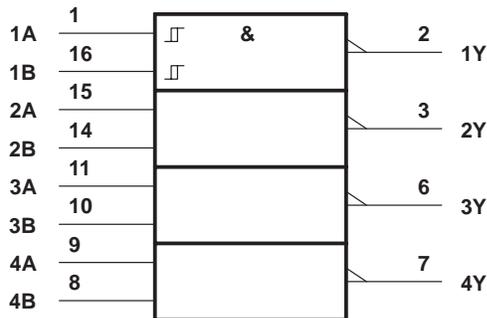
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The 74AC11132 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

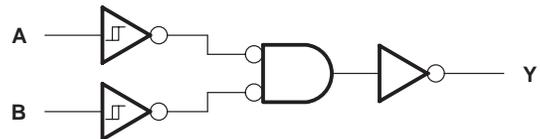
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	– 0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	– 0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	– 0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 100$ mA
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3$ V	2.2		V
		$V_{CC} = 4.5$ V	3.2		
		$V_{CC} = 5.5$ V	3.9		
$V_{IL}$	Low-level input voltage	$V_{CC} = 3$ V		0.5	mA
		$V_{CC} = 4.5$ V		0.9	
		$V_{CC} = 5.5$ V		1.1	
$V_I$	Input voltage			– 24	mA
$V_O$	Output voltage			– 24	
$I_{OH}$	High-level output current	$V_{CC} = 3$ V	0	$V_{CC}$	V
		$V_{CC} = 4.5$ V	0	$V_{CC}$	
		$V_{CC} = 5.5$ V		– 4	
$I_{OL}$	Low-level output current	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	ns/V
$T_A$	Operating free-air temperature	– 40		85	°C

# 74AC1132

## QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT-TRIGGER

SCAS113 – D3482, MARCH 1990 – REVISED APRIL 1993

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>T+</sub>		3 V	2.2			2.2		V
		4.5 V	3.2			3.2		
		5.5 V	3.9			3.9		
V <sub>T-</sub>		3 V	0.5			0.5		V
		4.5 V	0.9			0.9		
		5.5 V	1.1			1.1		
V <sub>hys</sub> (V <sub>T+</sub> - V <sub>T-</sub> )		3 V	1.2			0.3	1.2	V
		4.5 V	1.4			0.4	1.4	
		5.5 V	1.6			0.5	1.6	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
I <sub>OH</sub> = -24 mA	5.5 V	4.94			4.8			
I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V				3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V	0.1			0.1		V
		4.5 V	0.1			0.1		
		5.5 V	0.1			0.1		
	I <sub>OL</sub> = 12 mA	3 V	0.36			0.44		
		4.5 V	0.36			0.44		
	I <sub>OL</sub> = 24 mA	5.5 V	0.36			0.44		
I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V				1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	± 0.1			± 1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	4			40		μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	3.5					pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	2.2	6.2	9.2	2.2	10.3	ns
t <sub>PHL</sub>			2.8	6.8	9.8	2.8	10.5	

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	1.8	4.2	6.9	1.8	7.5	ns
t <sub>PHL</sub>			2.3	4.8	7.3	2.3	8	



# 74AC11132

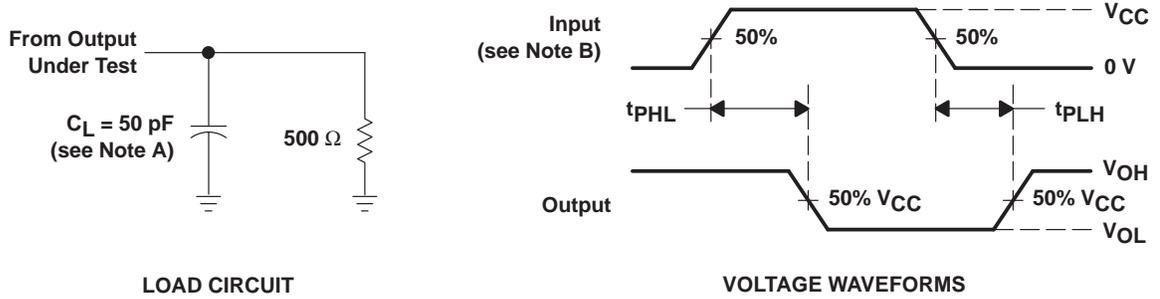
## QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT-TRIGGER

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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	27	pF

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74AC11132D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
74AC11132N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
74AC11132N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

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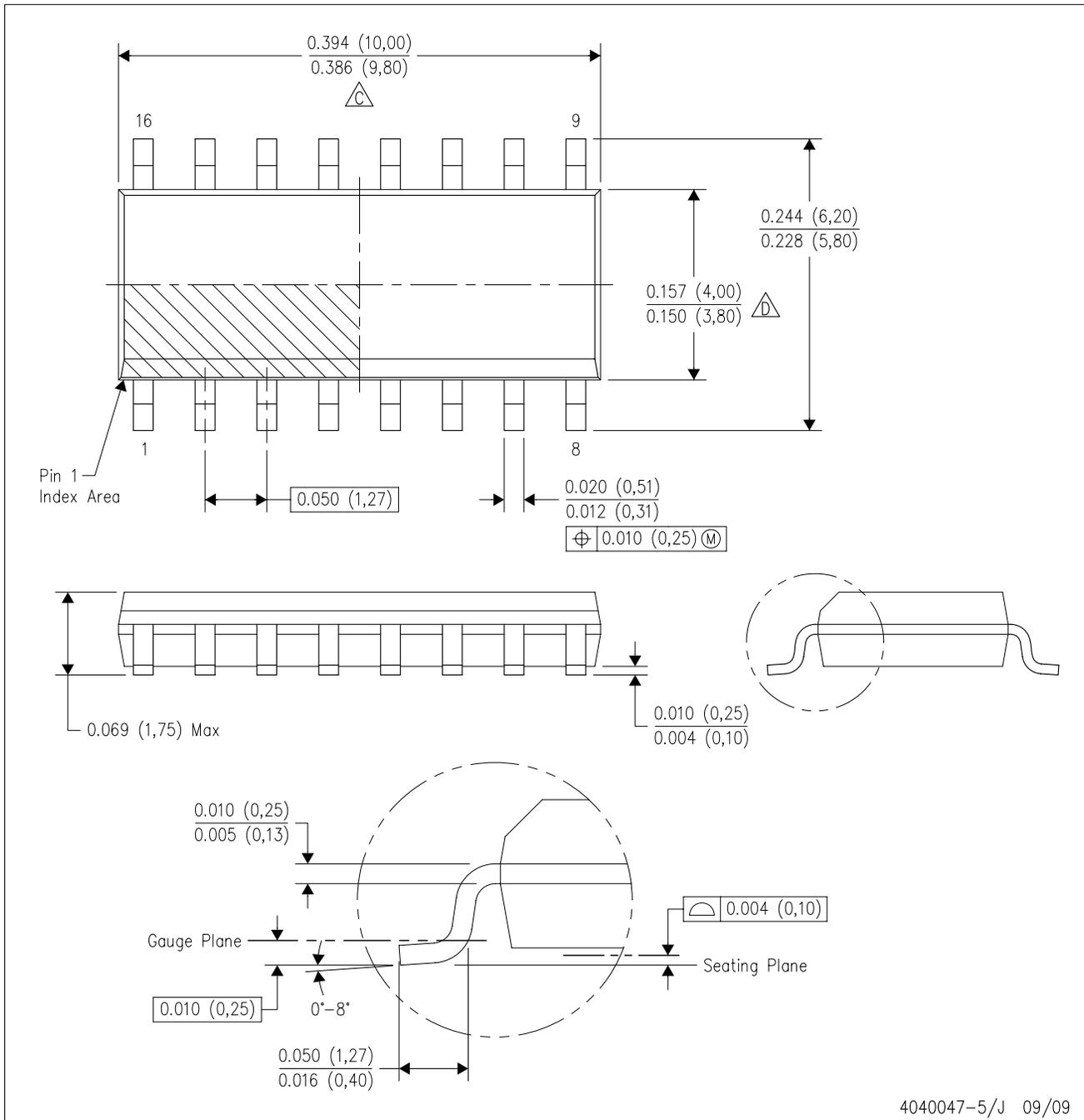
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



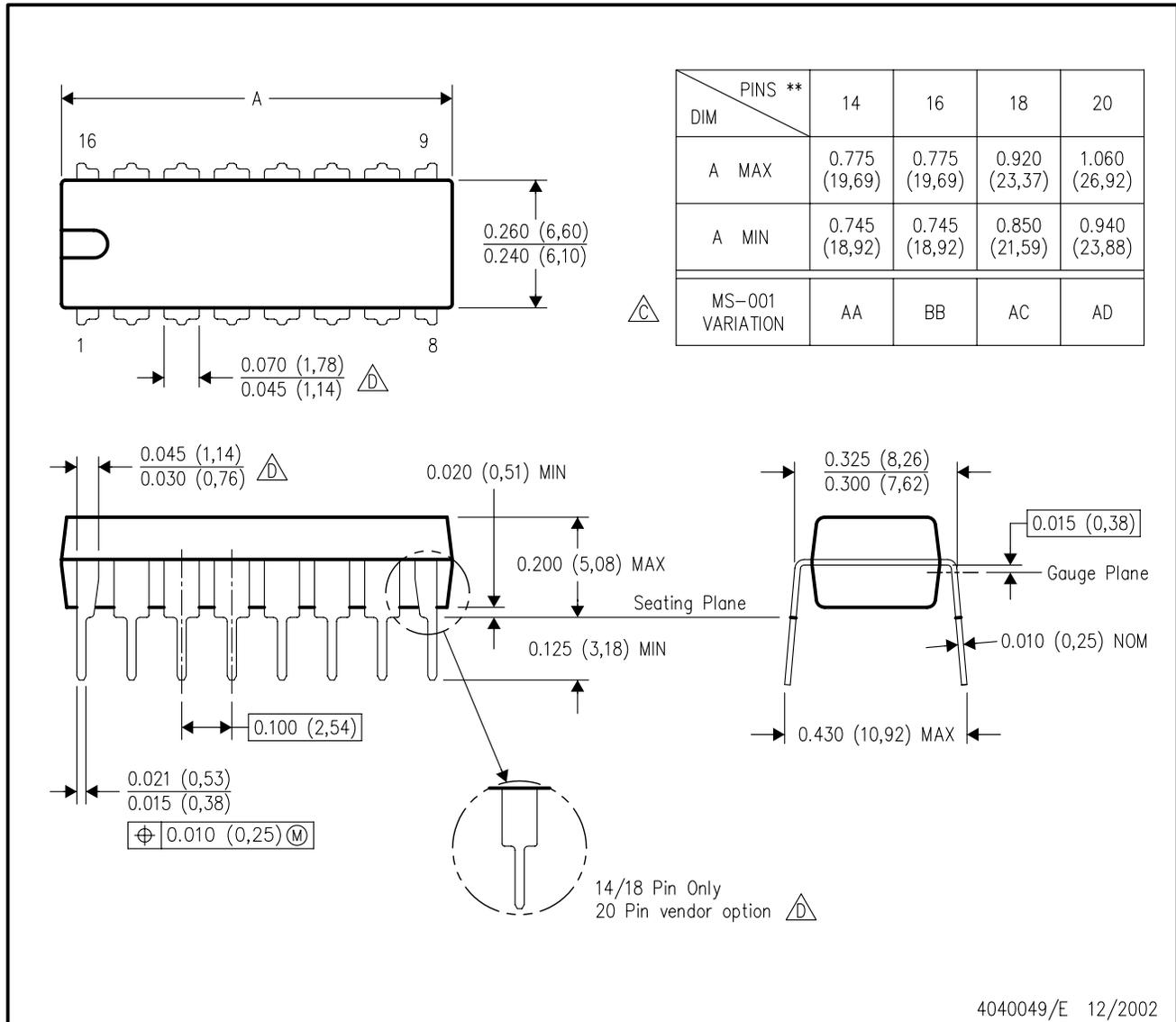
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- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

**PACKAGING INFORMATION**

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

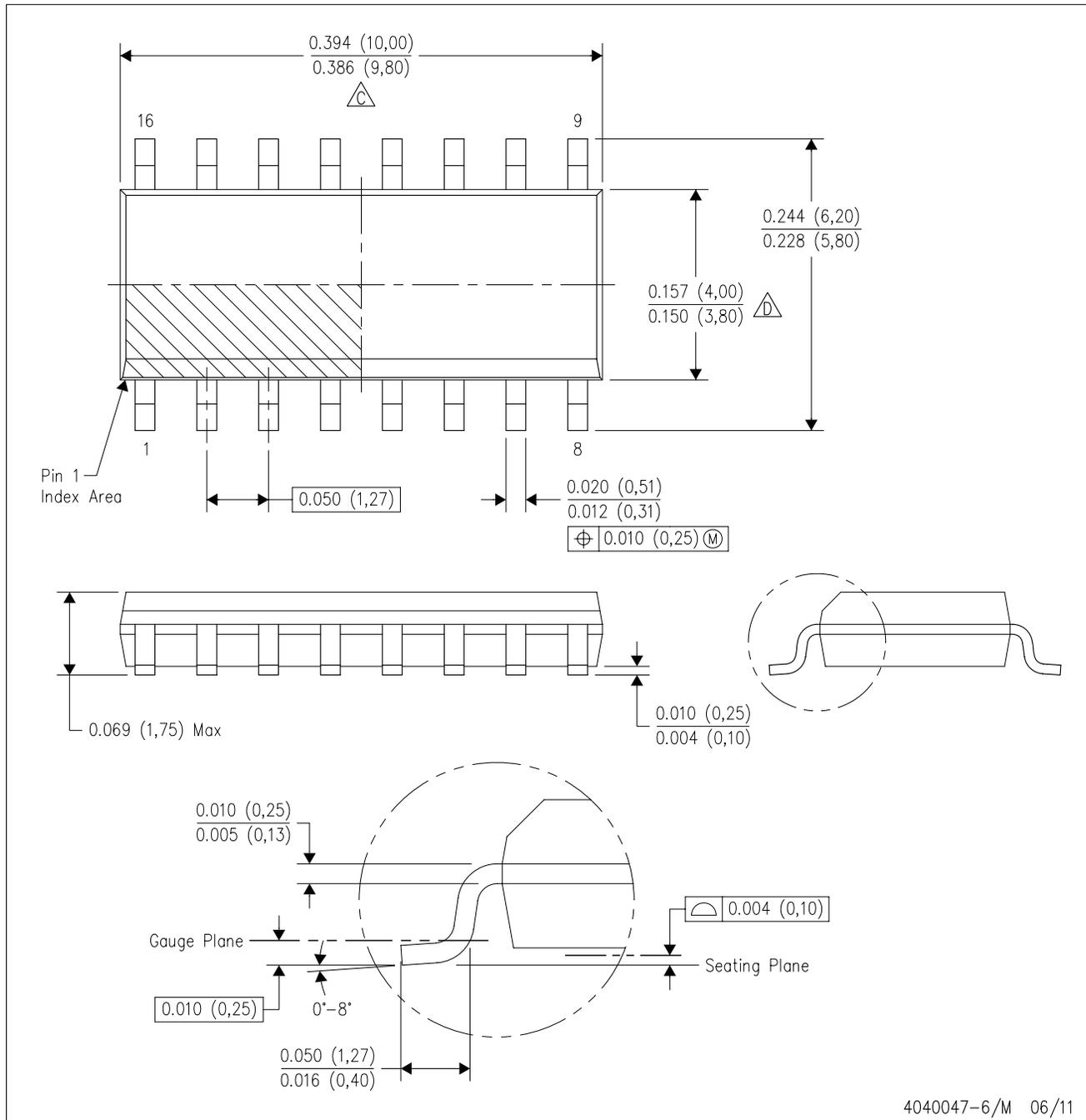


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- NOTES:
- A. All linear dimensions are in inches (millimeters).
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  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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