DESCRIPTION

The 511 is a monolithic dual high frequency differential amplifier with associated constant current source transistors and biasing diode. It is useful from DC to 100 MHz. The circuit arrangement provides for connection as two completely independent emitter coupled (differential) or cascode amplifiers. The bias diode allows stabilization of the current source currents over a large temperature range.

FEATURES

- **LOW INPUT OFFSET VOLTAGE = ±2mV**
- **LOW INPUT OFFSET CURRENT = ±3μA**
- **AGC CAPABILITY**
- **HIGH FORWARD TRANSADMITTANCE**
- **LOW FEEDBACK CAPACITANCE**
- **SINGLE POWER SUPPLY**

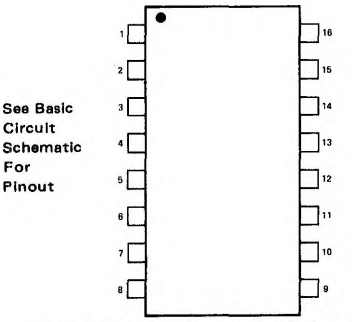
ABSOLUTE MAXIMUM RATINGS

Applied Voltage (V+)	20V
Output Collector Voltage	25V
Current (All Pins)	±15mA
Storage Temperature	-65°C to +150°C
Operating Temperature	
SE511Q, SE511B	-55°C to +125°C
NE511B, NE511Q	0°C to +75°C
Junction Temperature	150°C

Maximum ratings are limiting values above which serviceability may be impaired.

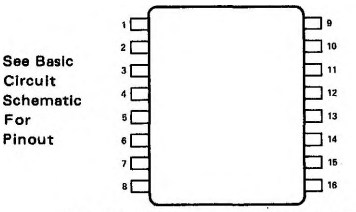
PIN CONFIGURATIONS

B PACKAGE
(Top View)



ORDER PART NOS. SE511B/NE511B

Q PACKAGE



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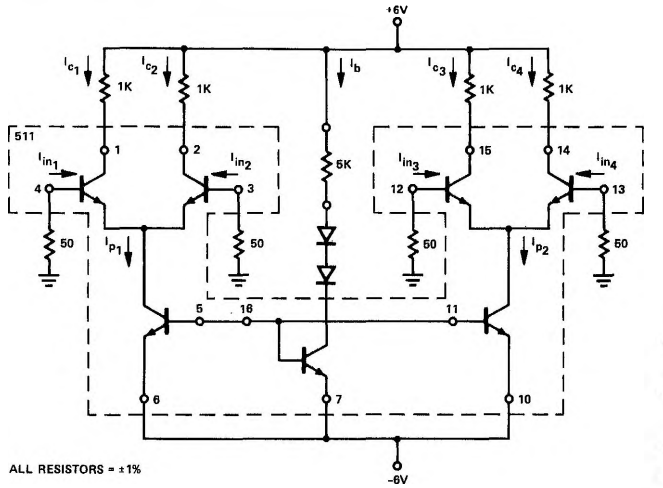
ELECTRICAL CHARACTERISTICS (Standard Test Circuit)

ACCEPTANCE TEST SUBGROUP	PARAMETERS	SYMBOL	LIMITS MIN SE511	LIMITS MIN NE511	LIMITS TYP SE511	LIMITS TYP NE511	LIMITS MAX SE511	LIMITS MAX NE511	UNITS	TEMPERATURE	TEST CONDITIONS
A-3	Input Offset Voltage	ΔV_{in}			0.5	0.5	2	3	mV	+25°C	
A-4		ΔV_{in}				1.0		4.0		0°C to +75°C	
A-5		ΔV_{in}			1.5		3.5			-55°C to +125°C	
A-3	Input Offset Current	ΔI_{in}			2.0	2.0	3.5	6	μA	+25°C	
A-4		ΔI_{in}				2.5		9		0°C to +75°C	
A-5		ΔI_{in}			2.5		7.5			-55°C to +125°C	
A-3	Input Bias Current	I_{in}			8.0	8.0	20	25	μA	+25°C	
A-4		I_{in}				10.0		40		0°C to +75°C	
A-5		I_{in}			16.0		40			-55°C to +125°C	
A-3	Differential Collector Current	ΔI_c			45	45	62.5	75	μA	+25°C	V_{in} = 0;
A-4	per differential pair	ΔI_c				50		100		0°C to +75°C	I_p = 2mA
A-5		ΔI_c			60		100			-55°C to +125°C	
A-3	Differential Current in the	ΔI_p			30	30	62.5	75	μA	+25°C	
A-4	Current Sources	ΔI_p				35		100		0°C to +75°C	
A-5		ΔI_p			35		100			-55°C to +125°C	
A-2	Total Current	I_{cc}			11.0	11.0	15.0	15.0	mA	+25°C	
A-3	Common Mode Rejection Ratio	CMRR	60	60	80	80			dB	+25°C	
A-3	Output Conductance	G_{22}			0.01	0.01			mmho	+25°C	
C-2	Output Capacitance	C_{ob}			2.5	2.5			pF	+25°C	
C-2	Input Capacitance	C_{ib}			10	10			pF	+25°C	

STANDARD TEST CIRCUIT



$\Delta I_{ih} = I_{in_1} - I_{in_2}$ or $I_{in_3} - I_{in_4}$

$\Delta I_c = I_{c_1} - I_{c_2}$ or $I_{c_3} - I_{c_4}$

$\Delta I_p = I_{p_1} - I_{p_2}$

$I_{cc} = I_{c_1} + I_{c_2} + I_{c_3} + I_{c_4} + I_b$.

BASIC CIRCUIT SCHEMATIC