2660-F,I,N • 2660-1 - F,I,N • 2660-2 - F,I,N • 2660-3 - F,I,N

DESCRIPTION

The 2660 is fabricated with n-channel silicon gate technology for high performance and high functional density, and uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2660 allows it to be packaged in the industry standard 16-pin in-line package, which provides the highest system bit densities and is compatible with widely available automated handling equipment.

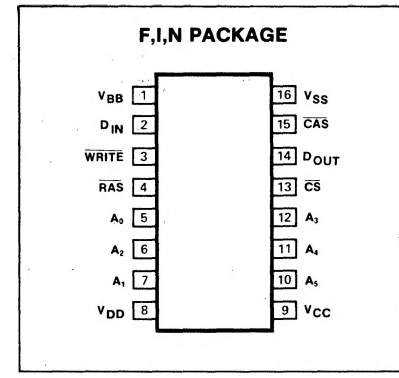
The use of the 16-pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2660 on 6 address input pins. The two 6-bit address words are latched into the device by the 2 TTL clocks, Row Address Strobe (RAS) and Column Address Strobe (CAS). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention, and this is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2ms.

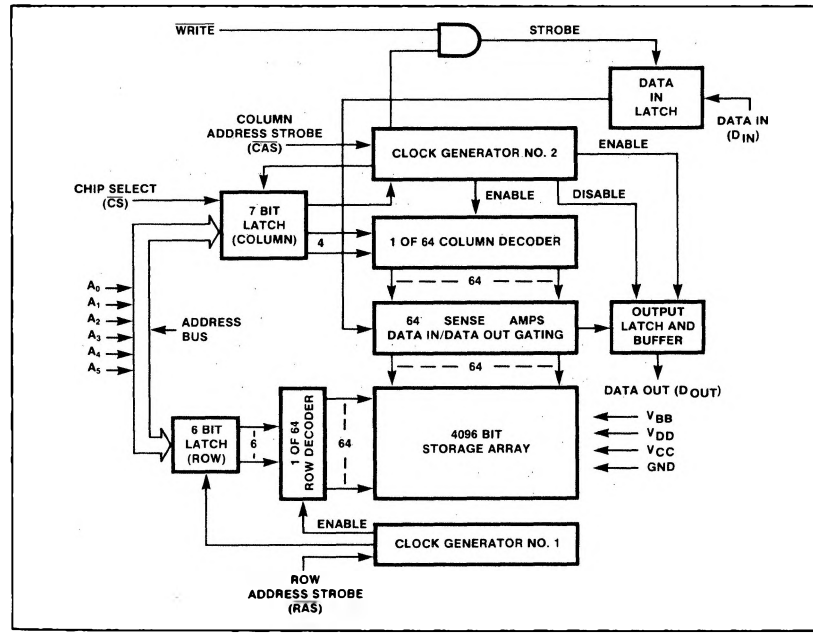
FEATURES

- **Standard 16-pin DIP**
- **All inputs including clocks TTL compatible**
- **On chip latches for address, chip select and data in**
- **Tri-state TTL compatible output**
- **Output data is latched and valid into next cycle**
- **Read and write cycle time:**
  - **2660: 375ns**
  - **2660-1: 425ns**
  - **2660-2: 500ns**
  - **2660-3: 375ns**
- **Access time:**
  - **2660: 250ns**
  - **2660-1: 300ns**
  - **2660-2: 350ns**
  - **2660-3: 250ns**
- **Low power:**
  - **Operating: <380mW**
  - **Standby: <24mW**
- **RAS only refresh (no dummy cycles required)**
- **Page mode addressing: 2660-3**
- **±10% power supply margins: 2660-3**
- **TRPW = $\overline{RAS}$ pulse width of 32μs: 2660-3**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
T_{STG}	Temperature range Storage	-55 to 150	°C
	All input or output voltages with respect to the most negative supply voltage V_{BB}	+25 to -.5	V
	Supply voltages V_{DD}, V_{CC} and V_{SS} with respect to V_{BB}	+20 to -.5	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD}[2] = 12V ± 5% (10%), V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = OV unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[3]	Any input				V
V_{IL}	Low		-1.0		0.8	
V_{IH}	High		2.4		7.0	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA	0.0		0.4	
V_{OH}	High	I_{OH} = -5.0mA	2.4		V_{CC}	
	Leakage current	Any input				μA
I_{IL}	Input[4]				5	
I_{OL}	Output[5]				10	
	V_{DD} current					mA
I_{DD1}	Average[6]				35	
I_{DD2}	Supply	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}		1	1.5	
I_{CC}	V_{CC} supply current[7]	Deselected			10	μA
I_{BB}	Average V_{BB} current				75	μA
	Capacitance					pF
C_{AD}	Address				10	
C_C	$\overline{CAS}$,$\overline{RAS}$,$\overline{CS}$,DIN,$\overline{WRITE}$				7	
C_{OUT}	Output				8	

AC ELECTRICAL CHARACTERISTICS[8]

T_A = 0°C to 70°C, V_{DD}[2] = 12V ± 5% (10%), V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise specified.

	PARAMETER	TO	FROM	2660			2660-1			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ, WRITE AND READ MODIFY WRITE CYCLES									
t_{REF}	Time between refresh					2			2	ms
t_{RP}	$\overline{RAS}$ precharge time			115			125			ns
t_{CP}	Column precharge time									ns
	Lead time									ns
t_{RCL}	Leading edge[9]	$\overline{CAS}$	$\overline{RAS}$	60		110	80		135	
t_{CRL}	Trailing edge[10]			-40		40	-50		50	
	Access time									ns
t_{CAC}[11]		Output	$\overline{CAS}$			140			165	
t_{RAC}[12]		Output	$\overline{RAS}$			250			300	
t_T	Rise and fall time[13]			3		50	3		50	ns
t_{OFF}	Output buffer turnoff delay			0		65	0		80	ns
	Setup and hold time									ns
t_{AS}	Setup time	$\overline{CAS}$	Address or $\overline{CS}$	0			0			
t_{AH}	Hold time	Address or $\overline{CS}$	$\overline{CAS}$	60			80			
	READ CYCLE									
t_{RC}	Random read cycle time[12,14]			375			425			ns
	Pulse width									ns
t_{CPW}	$\overline{CAS}$			140		10000	165		10000	
t_{RPW}	$\overline{RAS}$			250		10000	300		10000	
	Setup and hold time									ns
t_{RCS}	Setup time	$\overline{CAS}$ low	$\overline{WE}$ high	0			0			
t_{RCH}	Hold time	$\overline{WE}$ low	$\overline{CAS}$ high							
t_{RSH}	Hold time	$\overline{RAS}$ high	$\overline{CAS}$ low	140			165			
t_{CSH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	210			250			
	WRITE CYCLE									
t_{RC}	Random write cycle time[12,14]			375			425			ns
	Pulse width									ns
t_{CPW}	$\overline{CAS}$			140		10000	165		10000	
t_{RPW}	RAS			250		10000	300		10000	
t_{WP}	Write command			110			130			
	Setup and hold time									ns
t_{DS}	Setup time[15]	$\overline{CAS}$	Data in	0			0			
t_{DH}	Hold time[15]	Data in	$\overline{CAS}$	110			130			
t_{RSH}	Hold time	$\overline{RAS}$ high	$\overline{CAS}$ low	140			165			
t_{CSH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	210			250			
t_{WCH}	Hold time[16]	$\overline{WE}$ high	$\overline{CAS}$ low	110			130			
t_{CWL}	Lead time	$\overline{CAS}$ high	$\overline{WE}$ low	110			130			ns
	READ MODIFY WRITE CYCLE									
t_{RMW}	Read modify write cycle time[12,14]			475		10000	555	10000		ns
	Cycle width									ns
t_{CRW}	$\overline{CAS}$			250		10000	295	10000		
t_{RRW}	$\overline{RAS}$			360		10000	430	10000		
	Pulse width									ns
t_{WP}	Write command			110			130			
	Setup and hold time									ns
t_{DS}	Setup time	$\overline{CAS}$	Data in	0			0			
t_{DH}	Hold time	Data in	$\overline{CAS}$	110			130			
t_{RCS}	Setup time	$\overline{CAS}$ low	$\overline{WE}$ high	0			0			
t_{RWH}	Hold time	$\overline{RAS}$ high	$\overline{WE}$ low	110			130			
t_{CWH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	360			430			
t_{CWL}	Lead time	$\overline{CAS}$ high	$\overline{WE}$ low	110			130			ns
t_{MOD}	Modify time	$\overline{WE}$ low	Data out	0			0			ns

AC ELECTRICAL CHARACTERISTICS[8]

(Cont'd) T_A = 0°C to 70°C, V_{DD}[2] = 12V ± 5% (10%), V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise specified.

	PARAMETER	TO	FROM	2660-2			2660-3			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ, WRITE AND READ MODIFY WRITE CYCLES									
t_{REF}	Time between refresh					2			2	ms
t_{RP}	$\overline{RAS}$ precharge time			150			115			ns
t_{CP}	Column precharge time						110			ns
	Lead time									ns
t_{RCL}	Leading edge[9]	$\overline{CAS}$	$\overline{RAS}$	110		150	60		110	
t_{CRL}	Trailing edge[10]			-50		50	-40		40	
	Access time									ns
t_{CAC}[11]		Output	$\overline{CAS}$			200			140	
t_{RAC}[12]		Output	$\overline{RAS}$			350			250	
t_T	Rise and fall time[13]			3		50	3		50	ns
t_{OFF}	Output buffer turnoff delay			0		100	0		65	ns
	Setup and hold time									ns
t_{AS}	Setup time	$\overline{CAS}$	$\overline{Address}$ or $\overline{CS}$	0			0			
t_{AH}	Hold time	Address or $\overline{CS}$	CAS	100			60			
	READ CYCLE									
t_{RC}	Random read cycle time[12,14]			500			375			ns
	Pulse width									ns
t_{CPW}	$\overline{CAS}$			200		10000	140		32000	
t_{RPW}	$\overline{RAS}$			350		10000	250		32000	
	Setup and hold time									ns
t_{RCS}	Setup time	$\overline{CAS}$ low	$\overline{WE}$ high	0			0			
t_{RCH}	Hold time	$\overline{WE}$ low	$\overline{CAS}$ high							
t_{RSH}	Hold time	$\overline{RAS}$ high	$\overline{CAS}$ low	200			140			
t_{CSH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	350			210			
	WRITE CYCLE									
t_{RC}	Random write cycle time[12,14]			500			375			ns
	Pulse width									ns
t_{CPW}	$\overline{CAS}$			200		10000	140		32000	
t_{RPW}	$\overline{RAS}$			350		10000	250		32000	
t_{WP}	Write command			150			110			
	Setup and hold time									ns
t_{DS}	Setup time[15]	$\overline{CAS}$	Data in	0			0			
t_{DH}	Hold time[15]	Data in	$\overline{CAS}$	150			110			
t_{RSH}	Hold time	$\overline{RAS}$ high	$\overline{CAS}$ low	200			140			
t_{CSH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	300			210			
t_{WCH}	Hold time[16]	$\overline{WE}$ high	$\overline{CAS}$ low	150			110			
t_{CWL}	Lead time	CAS high	$\overline{WE}$ low	150			110			ns
	READ MODIFY WRITE CYCLE									
t_{RMW}	Read modify write cycle time[12,14]			650		10000	475		32000	ns
	Cycle width									ns
t_{CRW}	$\overline{CAS}$			350		10000	250		32000	
t_{RRW}	$\overline{RAS}$			500		10000	360		32000	
	Pulse width									ns
t_{WP}	Write command			150			110			
	Setup and hold time									ns
t_{DS}	Setup time	$\overline{CAS}$	Data in	0			0			
t_{DH}	Hold time	Data in	$\overline{CAS}$	150			110			
t_{RCS}	Setup time	$\overline{CAS}$ low	$\overline{WE}$ high	0			0			
t_{RWH}	Hold time	$\overline{RAS}$ high	$\overline{WE}$ low	150			110			
t_{CWH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	500			360			
t_{CWL}	Lead time	$\overline{CAS}$ high	$\overline{WE}$ low	150			110			ns
t_{MOD}	Modify time	$\overline{WE}$ low	Data out	0			0			ns

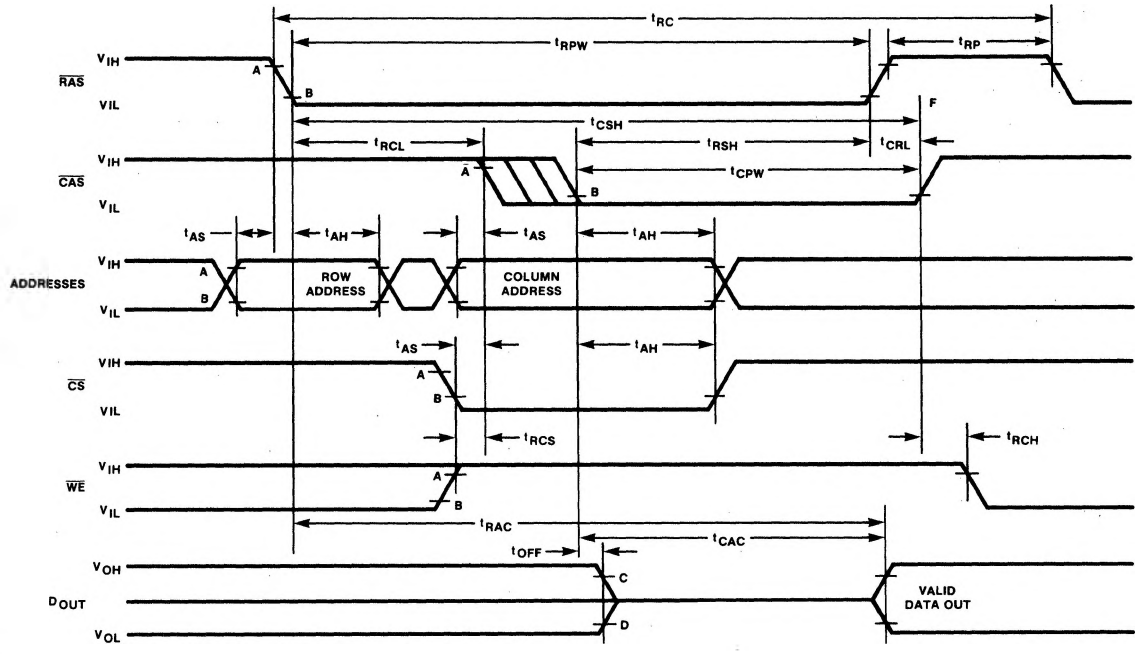
NOTES on following page.

NOTES

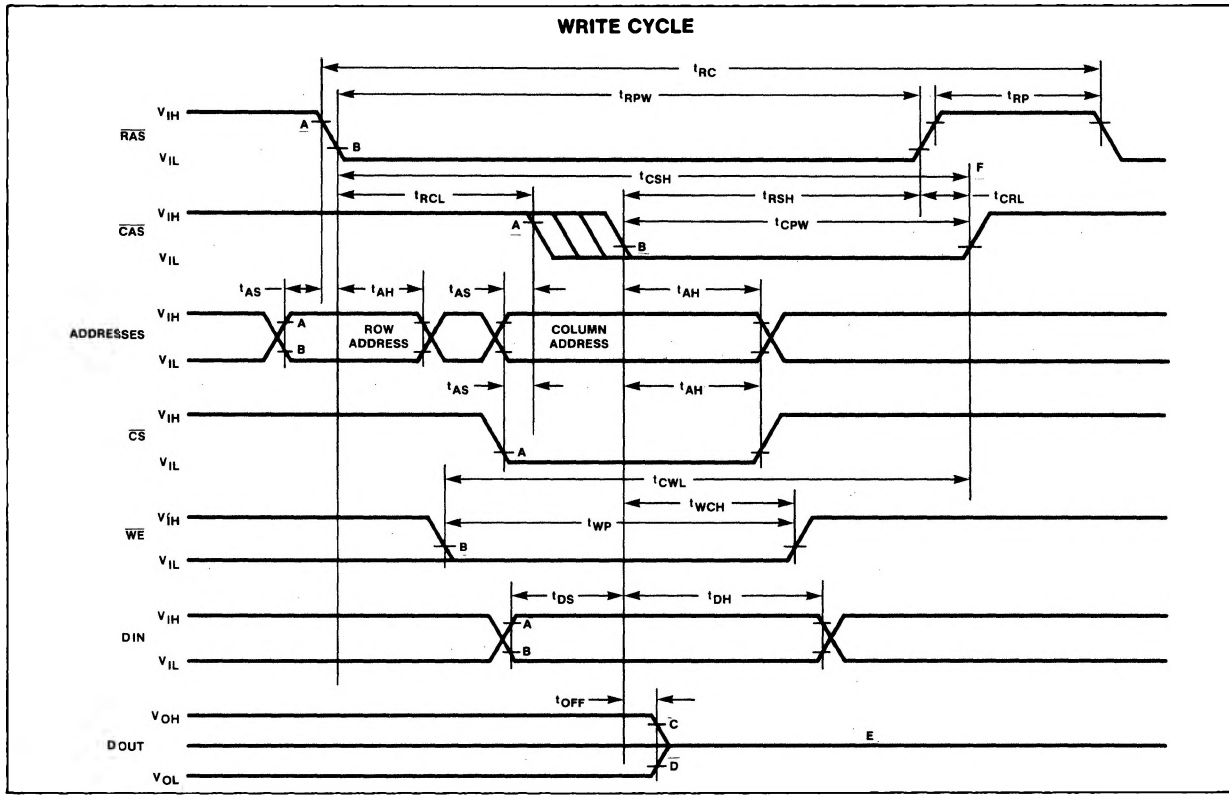
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. V_{DD} = 12 ± 10% for the 2660-3.
3. Input voltages greater than TTL levels (0 to 5V) require device operation at reduced speed.
4. All device pins at 0V except V_{BB} at -5V and pin under test which is at +10V.
5. Output disabled by chip select input.
6. Current is proportional to clock speed with maximum current measured at fastest cycle rate.
7. Depends upon output loading. The V_{CC} supply is connected to the output buffer only.
8. Assumes t_T = 5ns.
9. For minimum cycle, t_{RCL} has a maximum value of 110ns.
10. Implies $|t_{CRL}| \leq$ 40ns only for minimum cycle time; otherwise $|t_{CRL}| \gg$ 40ns is legal for other than minimum cycle time.
11. Assumes $t_{RCL} + t_T > t_{RCL}$ (max). If not, the access time is controlled by t_{RAC}.
12. Assumes that $t_{RCL} + t_T < t_{RCL}$ (max). If $t_{RCL} + t_T > t_{RCL}$ (max), then t_{RC} and t_{RAC} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).
13. Rise and fall times measured between V_{IH} and V_{IL}.
14. The minimum cycle time is achieved by compensating for RAS rise and fall times with t_{CRL}. The minimum cycle time is then constrained by t_{RCL} (max) + t_{CPW} + t_{RP}.
15. These parameters are referenced to the CAS leading edge in random write cycle operation and to the Write leading edge in read-write or read-modify-write cycle.
16. Write command hold time is important only when performing normal random write cycles. During read-write or read-modify-write cycles, the write command pulse width is the limiting parameter.
17. All voltages reference to V_{SS}.
18. Output voltage will swing from V_{SS} to V_{CC} independent of differential between V_{SS} and V_{CC}.

TIMING DIAGRAMS

READ CYCLE

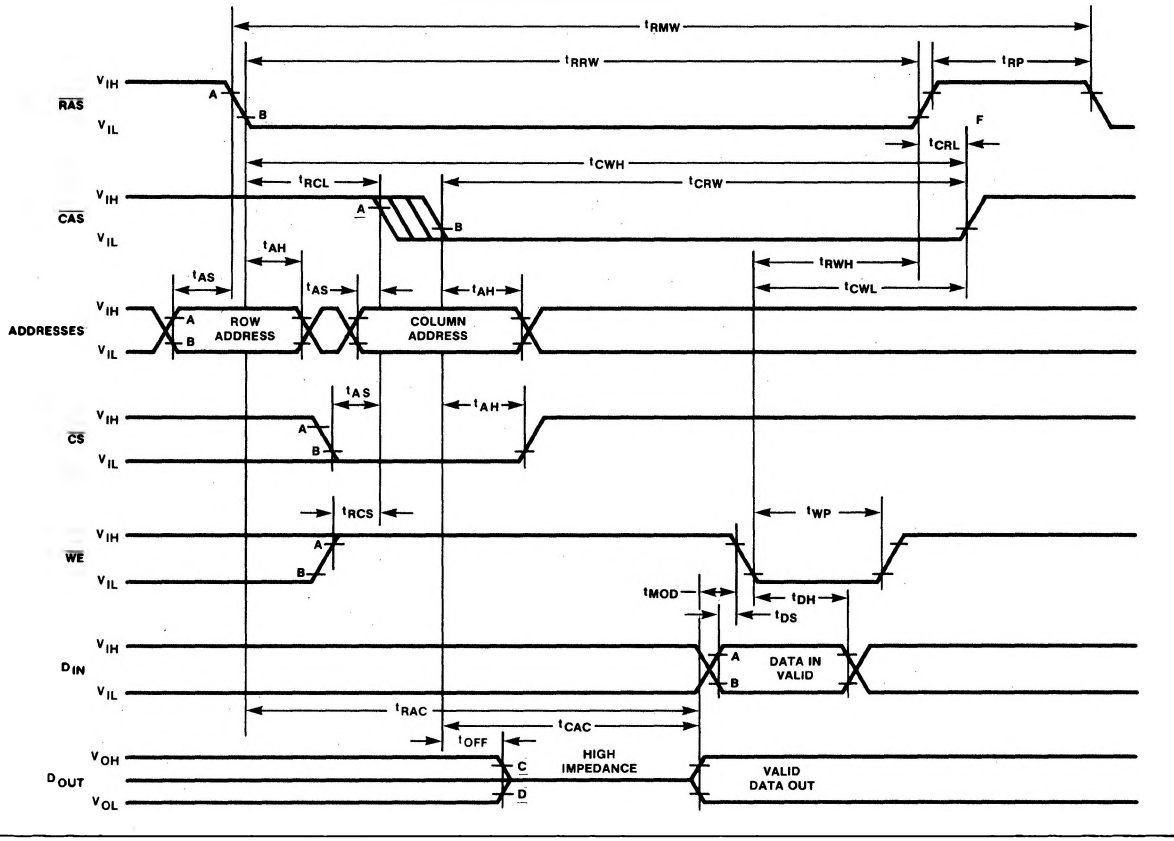


TIMING DIAGRAMS (Cont'd)



TIMING DIAGRAMS (Cont'd)

READ MODIFY WRITE CYCLE



NOTES

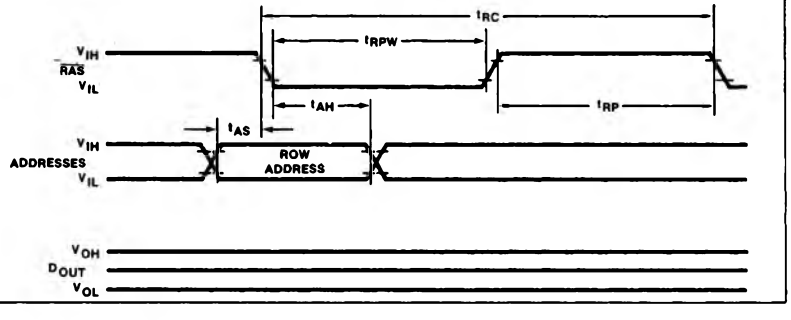
A,B. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.

C,D. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT} with 100pf load.

E. If $\overline{WE}$ goes low while $\overline{CAS}$ is low, D_{OUT} could go either V_{OL} or V_{OH} after t_{CAC}. D_{OUT} will be in open circuit state (write cycle waveforms), if $\overline{WE}$ goes Low before $\overline{CAS}$ goes low. In a read-modify-write cycle D_{OUT} is data read and does not change during modify-write portion of the cycle.

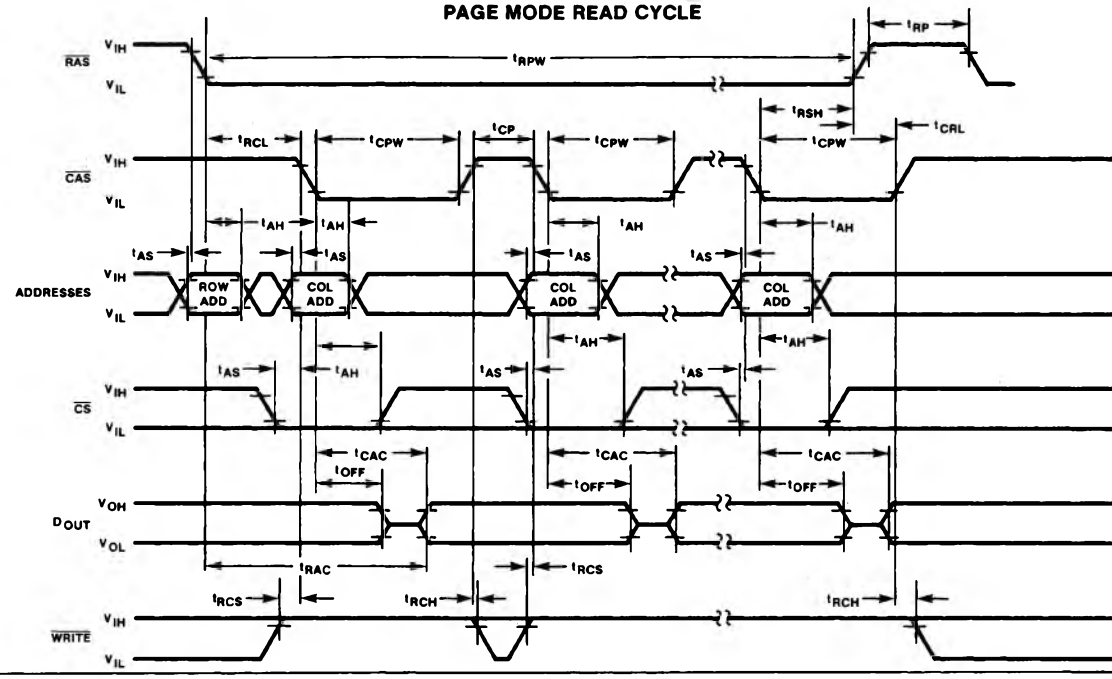
F. For minimum cycle timing, t_{CRL} must be 0 to 40ns for the 2660 and 2660-3; 0 to 50ns for the 2660-1 and 2660-2.

RAS ONLY REFRESH CYCLE



TIMING DIAGRAMS (Cont'd)

2660-3
PAGE MODE READ CYCLE



2660-3
PAGE MODE WRITE CYCLE