

DUAL 50-BIT STATIC SHIFT REGISTER (50X2)
DUAL 100-BIT STATIC SHIFT REGISTER (100X2)
DUAL 200-BIT STATIC SHIFT REGISTER (200X2)

2509
2510
2511

2509-N,K • 2510-N,K • 2511-N,K

DESCRIPTION

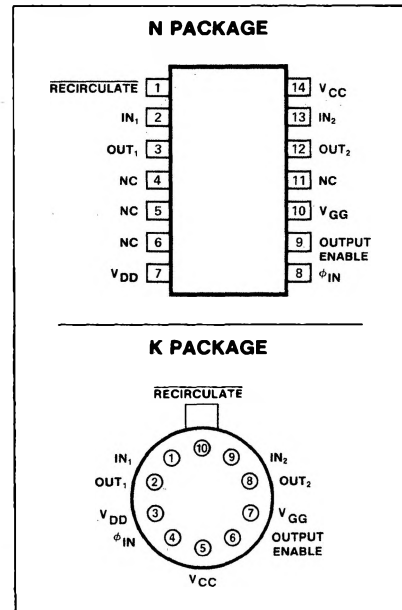
The 2509 50-bit, 2510 100-bit, and the 2511 200-bit recirculating static shift registers consist of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals plus tri-state outputs are provided for maximum interfacing ease.

TRUTH TABLE

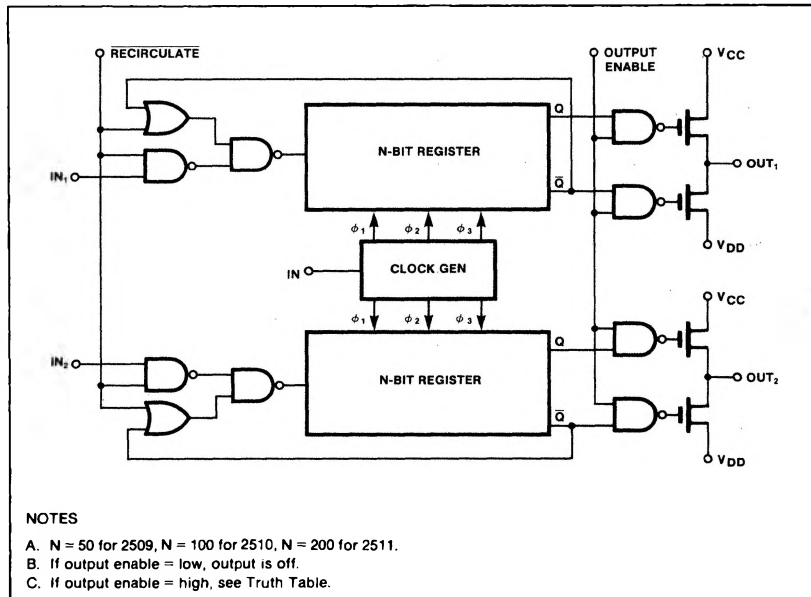
RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

"0" = OV; "1" = +5V.

PIN CONFIGURATIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
T _A Temperature range		°C
Operating ²	0 to 70	
Storage	-65 to 150	
P _D Power dissipation at T _A = 70°C ²	535	mW
Data and clock input voltages and supply voltages with respect to V _{CC} ³	0.3 to -20	V

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DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V}$, $V_{DD} = -5\text{V} \pm 5\%$, $V_{GG} = -12\text{V} \pm 5\%$
 unless otherwise specified^{5,6,7,8}

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IL} Input voltage ⁴ Low				0.6	V
V_{IH} High		3.4		5.3	
V_{ILC} Clock low		-5		0.6	
V_{IHC} Clock high		3.4		5.3	
V_{OL} Output voltage Low	$I_{OL} = 1.6\text{mA}$ $I_{OH} = 100\mu\text{A}$			0.5	V
V_{OH} High Driving MOS		3.8	3.5		
I_{LO} Leakage current Output	$T_A = 25^\circ\text{C}$ $V_{CE} = 1.05\text{V}$, $V_{OUT} = -5\text{V}$ $V_{ILC} = \text{GND}$			1000	nA
I_{LC} Clock				500	
I_{DD} Supply current Dual 50 Dual 100 Dual 200	Continuous operation, $T_A = 25^\circ\text{C}$, $f = 1.5\text{MHz}$			15	mA
I_{GG}			6.5	30	
			20	40	
			4.5	7.5	
I_{LI} Input load current	$V_{IN} = -5.5\text{V}$, $T_A = 25^\circ\text{C}$		10	500	nA
C_{IN} Capacitance Input	At 1MHz; $V_{AC} = 25\text{mV p-p}$ $V_{IN} = V_{CC}$ $V_{OUT} = V_{CC}$ $V_{\phi} = V_{CC}$			5	pF
C_{OUT} Output				5	
C_{ϕ} Clock				5	

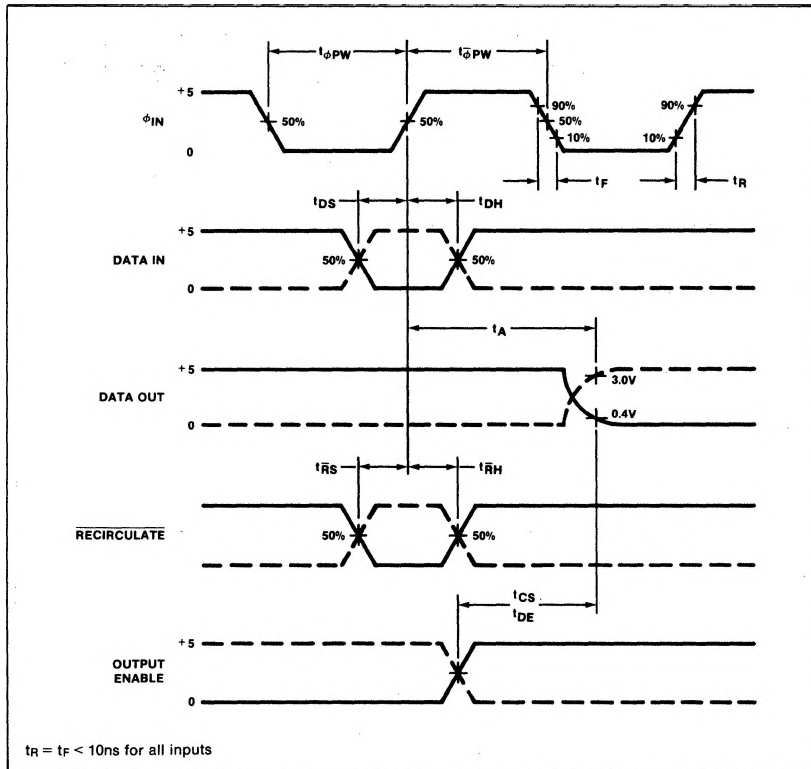
AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5\text{V}$, $V_{DD} = -5\text{V} \pm 5\%$, $V_{ILC} = 0.4\text{V}$ to 4V , $V_{GG} = -12\text{V} \pm 5\%$,
 $T_A = 0^\circ\text{C}$ to 70°C .

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Freq. Clock rep rate				dc	3	1.5	MHz
$t_{\phi PW}$ Pulse width Clock				.290	150	100	μs
$\bar{t}_{\phi PW}$ Clock				.210		dc	
t_{DS} Setup and hold time Setup time	ϕ_{in} Data in	Data in ϕ_{in}		50			ns
t_{DH} Hold time				70			
t_A Propagation delay	Data out	Clock	$I_{OL} = 1.6\text{mA}$		200	350	ns
\bar{t}_A					500		
T_{CS} Select time	Data out	Output enable				300	ns
T_{DE} Deselect time						300	ns
t_R, t_F Clock pulse transition						1	μs

NOTES

- Stresses above those listed under absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
- For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 150°C/W .
- All inputs are protected against static charge accumulation.
- Guaranteed input levels are stated for worst case conditions including a $\pm 5\%$ variation in V_{CC} and a temperature variation of 0°C to 70°C . Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85\text{V}$ and $V_{IL} = V_{CC} - 4.15\text{V}$.
- Parameters are valid over operating temperature range unless otherwise specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process changes and improvements.
- Typical values are at 25°C and typical supply voltages.

TIMING DIAGRAM



TYPICAL APPLICATION

