signetics

512 AND 1024-BIT RECIRCULATING DYNAMIC SHIFT REGISTERS

2505
2512

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series 512 and 1024 bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls, together with two chip select controls are included on the chip.

FEATURES

- HIGH FREQUENCY OPERATION–3 MHz TYPICAL CLOCK RATE
- SINGLE 512, SINGLE 1024
- TTL, DTL COMPATIBLE
- 2-CHIP SELECT CONTROLS FOR XY MATRIX SELECTION
- WRITE AND READ CONTROLS INCLUDED
- LOW POWER DISSIPATION–150μW/bit at 1 MHz
- LOW CLOCK CAPACITANCE–80pF for 512, 160pF for 1024 Bits
- +5, -5V POWER SUPPLIES
- STANDARD PACKAGE–10 LEAD TO-100
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

FAST ACCESS SWAPPING MEMORY SYSTEMS
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT
DRUM MEMORY REPLACEMENT

PROCESS TECHNOLOGY

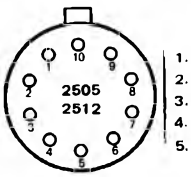
Use of low threshold *silicon gate technology* allows high speed (3MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to other technologies. The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

The signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

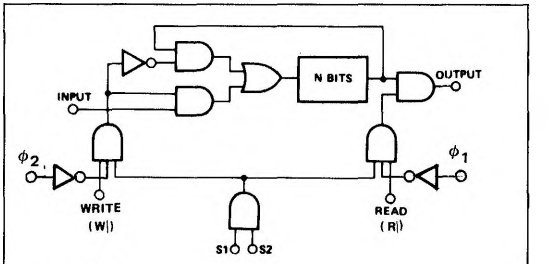
PIN CONFIGURATION (Top View)

K PACKAGE



1. Select 1
2. Write
3. Input
4. ϕ_1 Output Clock
5. V_{CC}
6. ϕ_2 Input Clock
7. Output
8. Read
9. Select 2
10. V_{DD}

BLOCK DIAGRAM



NOTES:
N = 512 or 1024 '0' = 0V, '1' = +5V.
When S1 or S2 is '0' Data Recirculates
When S1 and S2 are '1' see truth table

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read/Write, Output is Data

PART IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
2505K	512	10 pin TO - 100
2512K	1024	10 pin TO - 100

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (2)	535mW@T_A>70°C
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to −20V

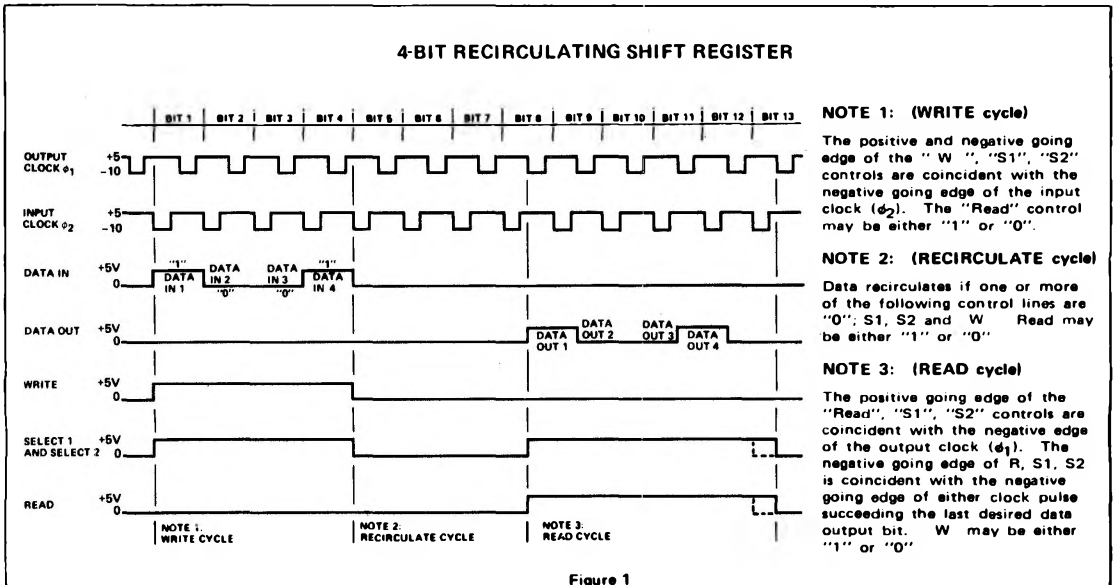
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. See "Minimum Operating Frequency" graph for low limits on data rep. rate.
5. Parameters are valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and nominal supply voltages.
9. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
10. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).

DC CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = +5V$ (9) ; $V_{DD} = -5V$ ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	$V_{IN} = -5.5V$; $T_A = 25°C$
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi 1} = V_{\phi 2} = -12V$, $V_{DD} = -5V$; $V_{OUT} = -5.5V$; $T_A = 25°C$
I_{LC}	Clock Leakage Current		10	1000	nA	$V_{ILC} = 12V$; $T_A = 25°C$
I_{DD}	Power Supply Current: 2505		15	25	mA	Continuous Operation; ϕ pW = 150nS, 1MHz
	2512		25	35	mA	$V_{ILC} = -12V$; $T_A = 25°C$ $V_{DD} = -5.5V$
V_{IL}	Input "Low" Voltage	-5.0		1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-12.0		-10.0	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	

TIMING DIAGRAM



NOTE 1: (WRITE cycle)

The positive and negative going edge of the " W ", "S1", "S2" controls are coincident with the negative going edge of the input clock (ϕ_2). The "Read" control may be either "1" or "0".

NOTE 2: (RECIRCULATE cycle)

Data recirculates if one or more of the following control lines are "0"; S1, S2 and W Read may be either "1" or "0"

NOTE 3: (READ cycle)

The positive going edge of the "Read", "S1", "S2" controls are coincident with the negative edge of the output clock (ϕ_1). The negative going edge of R, S1, S2 is coincident with the negative going edge of either clock pulse succeeding the last desired data output bit. W may be either "1" or "0"

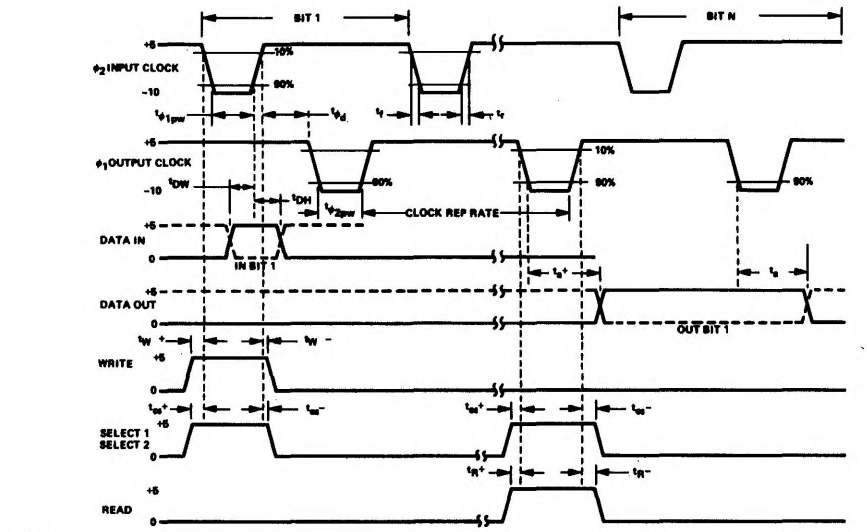
Figure 1

Figure 1 is a simplified illustration of the timing of a 4-bit recirculating shift register showing the 3 basic modes of operation.

CONDITIONS OF TEST

Input rise and fall times: 10 nsec Output load is 1 TTL gate

TIMING DIAGRAM



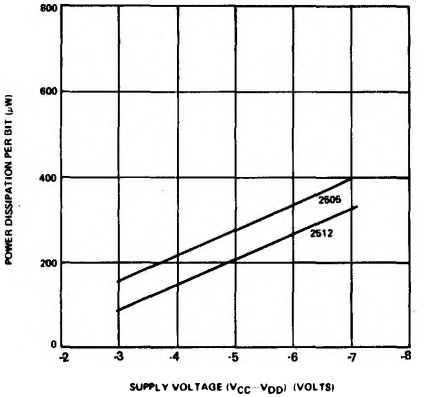
NOTE:
1. N=512 for 2505, N=1024 for 2512
2. Note that the Read Input is AND'ed with $\overline{\phi_1}$; therefore this function is not valid until ϕ_1 occurs.

AC CHARACTERISTICS T_A=+25°C V_{CC}=+5V (9); V_{DD}=−5V ± 5%; V_{ILC}=-11V

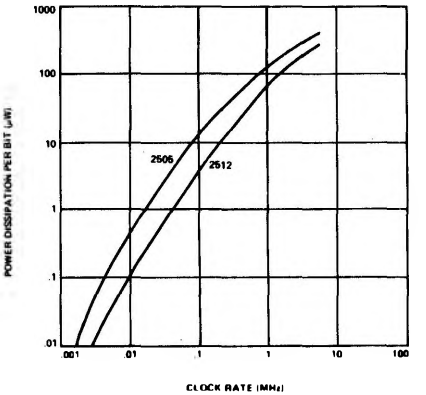
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Data Rep Rate	.0005 (Note 4)	3	2.5	MHz	W = R = V_{CC}
$t_{\phi pw}$	Clock Pulse Width	180			nsec	
$t_{\phi d}$	Clock Pulse Delay	10			nsec	
t_r;t_f	Clock Pulse Transition			1	μsec	
t_{DW}	Data Write (Setup) Time	150			nsec	
t_{DH}	Data to Clock Hold Time	10			nsec	
t_{a+};t_{a-}	Clock to Data Out Delay			100	nsec	
t_{R-};t_{CS-} $t_{W\ -}$	Clock to "Read" or "Chip Select" or "Write" Timing	0			nsec	
t_{R-};t_{CS+} $t_{W\ +}$	Clock to "Read" or "Chip Select" or "Write" Timing	0			nsec	
C_{in}	Input Capacitance			5	pF	1 MHz; V_I=V_{CC}; V_{AC}=25mV$_{P-P}$
C_{out}	Output Capacitance			5	pF	1 MHz; V_O=V_{CC}; V_{AC}= 25mV$_{P-P}$
C_ϕ	Clock Capacitance 2505 2512			50 100	pF pF	1 MHz; V =V_{CC}; V_{AC}= 25mV p-p
V_{OL}	Output "Low" Voltage		-1.0		V	R_L = 3.0K; 1 TTL Load (I_L = 1.6mA) Note 10
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	2.4	3.5		V	R_L = 3.0K; 1 TTL Load (I_L = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6K; C_L = 10 pF

CHARACTERISTICS CURVES

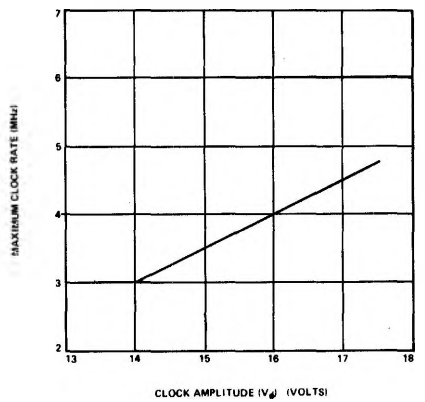
POWER DISSIPATION/BIT VERSUS SUPPLY VOLTAGE



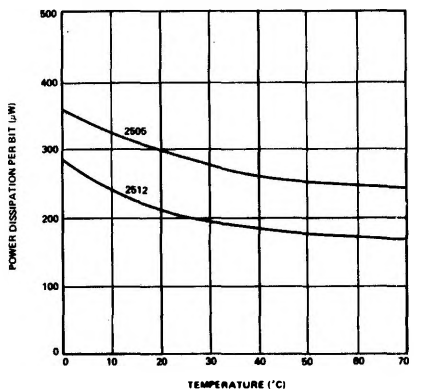
POWER DISSIPATION/BIT VERSUS CLOCK RATE



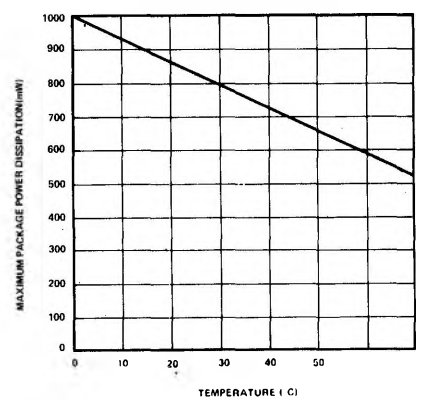
MAXIMUM CLOCK RATE VERSUS CLOCK AMPLITUDE



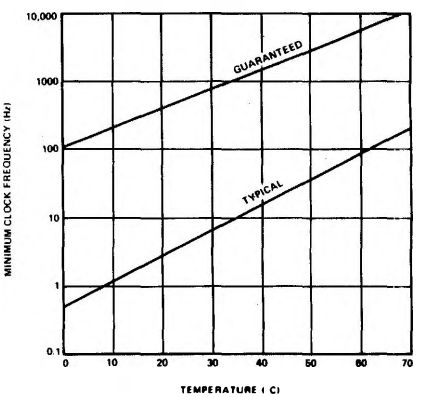
POWER DISSIPATION/BIT VERSUS TEMPERATURE



MAXIMUM PACKAGE POWER DISSIPATION VERSUS TEMPERATURE



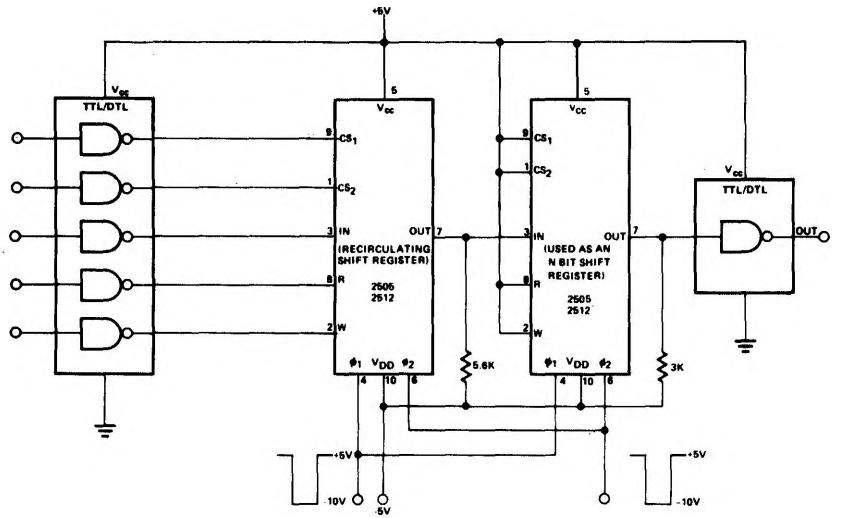
MINIMUM OPERATING CLOCK FREQUENCY



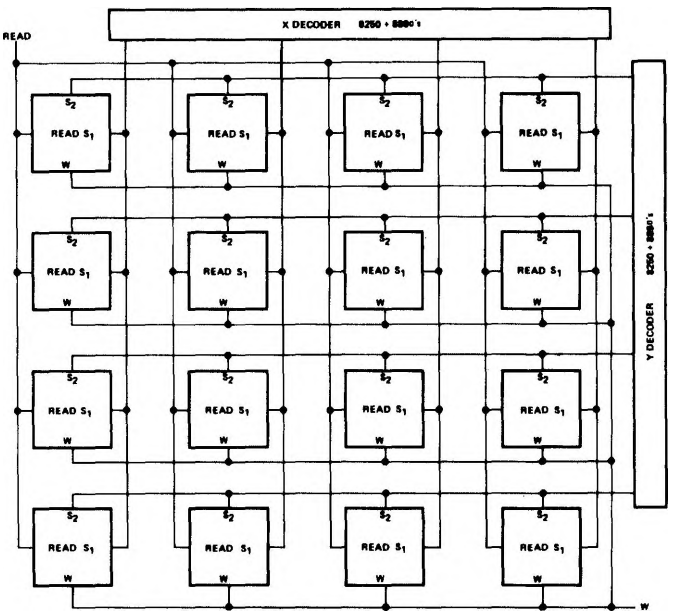
NOTE:
Conditions for Typical Curves = V_{CC}=+5V, V_{DD}=−5V, Clock Duty Cycle=35°C, f_{CLK}=2.5MHz, $V_{\phi p\text{-}p}$=16V, ϕ_{PW} =180ns, T_A=25°C unless otherwise noted

APPLICATIONS DATA

TTL/DTL/MOS INTERFACES

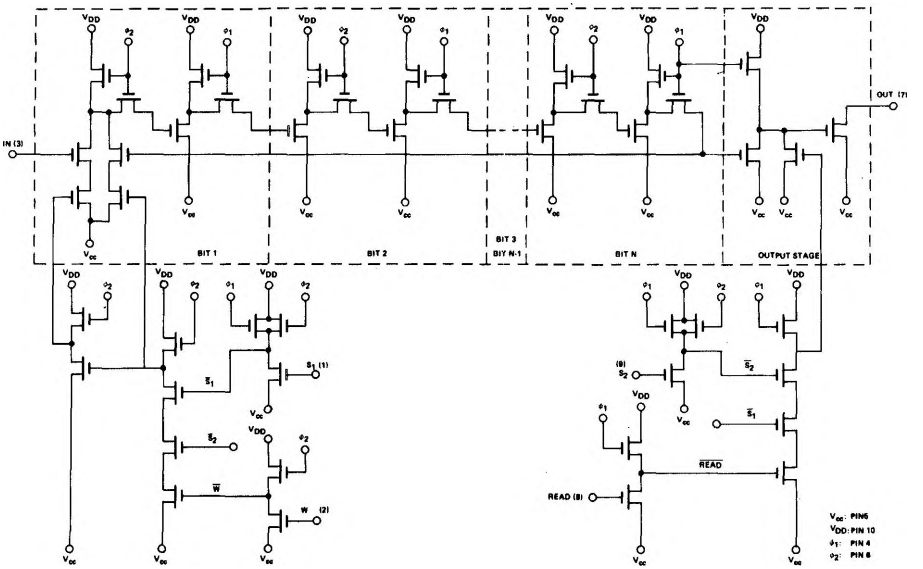


MATRIX CHIP SELECT LOGIC



NOTES:
1. Outputs common for each plane
2. All inputs common for each plane
3. All ϕ_1's common
4. All ϕ_2's common
5. All V_{CC} common
6. All V_{DD} common

CIRCUIT SCHEMATIC



NOTE: N = 512 for 2505
N = 1024 for 2512