

DESCRIPTION

These Signetics 2500 Series 1024-bit multiplexed dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Due to on-chip multiplexing, the data rate is twice the clock rate.

FEATURES

- 10 MHz TYPICAL DATA RATE
- THREE CONFIGURATIONS—QUAD 256, DUAL 512, SINGLE 1024
- LOW POWER DISSIPATION—40 μ W/bit at 1 MHz DATA RATE
- LOW CLOCK CAPACITANCE—140 pF
- TTL, DTL COMPATIBLE
- STANDARD PACKAGES - 8 LEAD TO-99, 8-PIN AND 16-PIN DUAL IN-LINE PACKAGE
- SIGNETICS P-MOS SILICON GATE PROCESS AND SILICONE PACKAGING TECHNOLOGIES

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (10 MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to conventional technologies.

The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

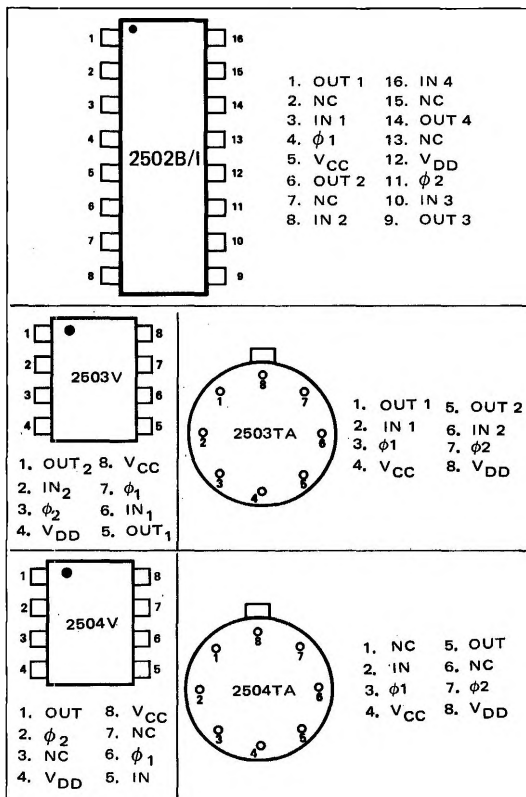
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

BIPOLAR COMPATIBILITY

The data inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

PIN CONFIGURATIONS (Top View)



PART IDENTIFICATION TABLE

TYPE	FUNCTION	PACKAGE
2502B	Quad 256-bit	16-Pin Silicone DIP
2502I	Quad 256-bit	16-Pin Ceramic DIP
2503TA	Dual 512-bit	TO-99
2503V	Dual 512-bit	8-Pin DIP
2504TA	Single 1024-bit	TO-99
2504V	Single 1024-bit	8-Pin DIP

MAXIMUM SIGNETICS GUARANTEED RATINGS(1)

Operating Ambient Temperature(2)	0°C to +70°C
Storage Temperature	-65°C to + 150°C
Power Dissipation(2) at T _A = 70°C	
TA and V Package	535mW
B Package	640mW
Data and Clock Input Voltages and Supply Voltages with respect to V _{CC} (3)	+0.3V to -20V

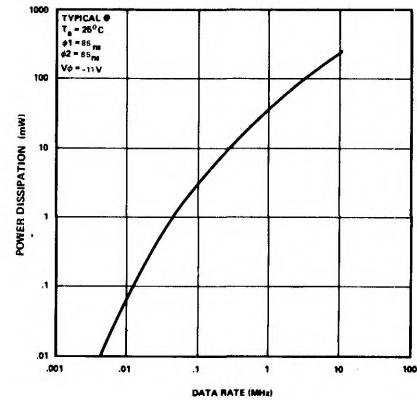
- NOTES:
- 1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
 - 2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (TA and V package) or 125°C/W (B package).
 - 3. All inputs are protected against static charge.
 - 4. Parameters are valid over operating temperature range unless specified.
 - 5. All voltage measurements are referenced to ground.
 - 6. Manufacturer reserving the right to make design and process changes and improvements.
 - 7. Typical values at +25°C and nominal supply voltages.
 - 8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
 - 9. When cascading use 140ns minimum to allow data set-up time for driver register.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{DD} = -5V ±5%; V_{CC} = +5V(8) unless otherwise noted. (See Notes 4,5,6,7).

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I _{LI}	Input Load Current		10	500	nA	V _{IN} = V _{CC} to V _{DD} , T _A = 25°C
I _{LO}	Output Leakage Current		10	1000	nA	V _{φ1} = V _{φ2} = -10V V _{OUT} = 0.0V, T _A = 25°C
I _{LC}	Clock Leakage Current		10	1000	nA	V _{ILC} = -10V T _A = 25°C
I _{DD}	Power Supply Current		15	25	mA	Outputs at logic "0", 4 MHz data rate, φ1 = φ2 = 85ns continuous operation, V _{ILC} = -12V T _A = 25°C
V _{IL}	Input "Low" Voltage			1.05	V	
V _{IH}	Input "High" Voltage	3.2		5.3	V	
V _{IHC}	Clock Input "High" Voltage	4.0		5.3	V	
V _{ILC}	Clock Input "Low" Voltage	-10		-12	V	

POWER DISSIPATION VERSUS DATA RATE

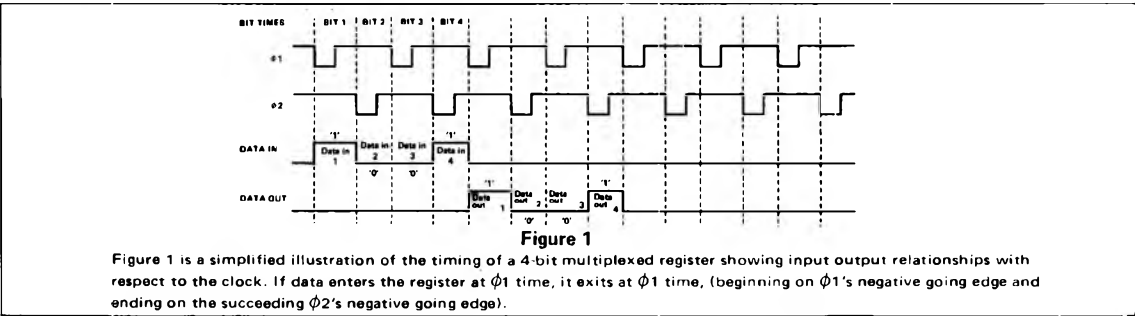


AC CHARACTERISTICS

T_A = 25°C, V_{DD} = -5V ±5%; V_{CC} = +5V (8) ; V_{ILC} = -11V , (See notes 4, 5, 6, 7)

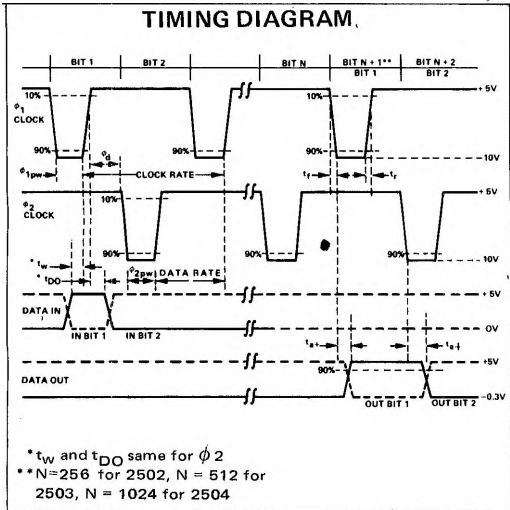
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	0.0005		4	MHz	See note 9
Frequency	Data Rep Rate	0.001		8	MHz	
ϕ pw	Clock Pulse Width (9)	85			ns	
ϕ d	Clock Pulse Delay	10			ns	
t _r , t _f	Clock Pulse Transition	10		1000	ns	
t _W	Data Write Time (Setup)	50			ns	@ 1 MHz 25 mV p-p @ 1 MHz 25 mV p-p @ 1 MHz 25 mV p-p
t _{DO}	Data in Overlap	10			ns	
t _a +	Data Out			90	ns	
C _{IN}	Input Capacitance	2.5		5	pF	
C _{OUT}	Output Capacitance	2.5		5	pF	
C ϕ	Clock Capacitance	130		150	pF	R _L = 3k, depends on R _L and TTL Gate R _L = 5.6k R _L = 3k
V _{OL}	Output "Low" Voltage		-0.3		V	
V _{OH1}	Output "High" Voltage Driving MOS	3.6	4.0		V	
V _{OH2}	Output "High" Voltage Driving TTL	3.0	3.5		V	

MULTIPLEXED 4-BIT MOS SHIFT REGISTER

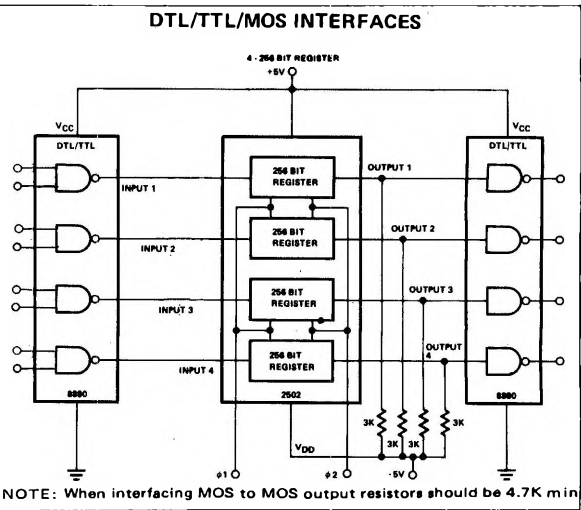


CONDITIONS OF TEST

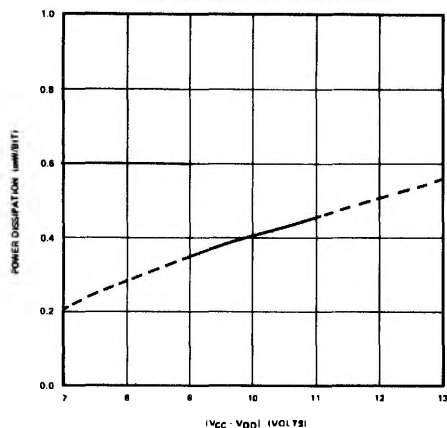
Input rise and fall times: 10nsec. Output load is 1 TTL gate.



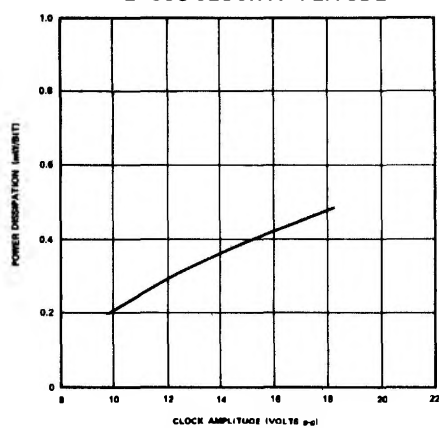
APPLICATIONS INFORMATION



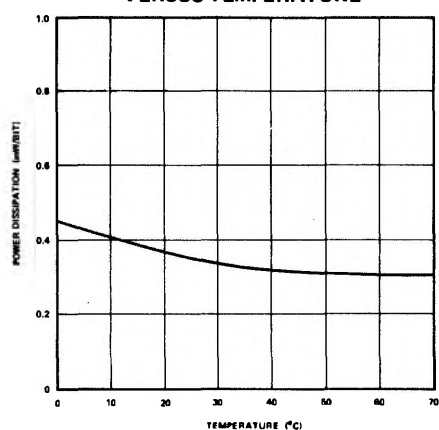
**POWER DISSIPATION/BIT
VERSUS SUPPLY VOLTAGE**



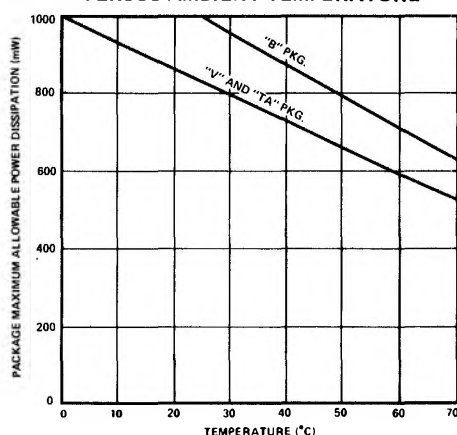
**POWER DISSIPATION/BIT
VERSUS CLOCK AMPLITUDE**



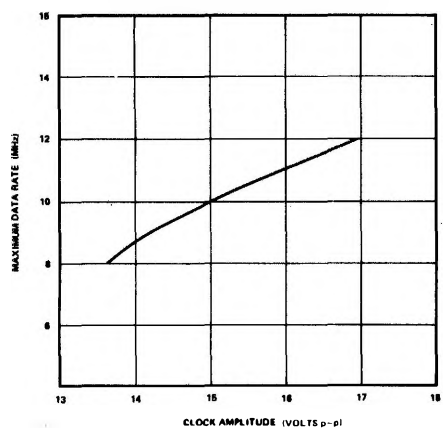
**POWER DISSIPATION/BIT
VERSUS TEMPERATURE**



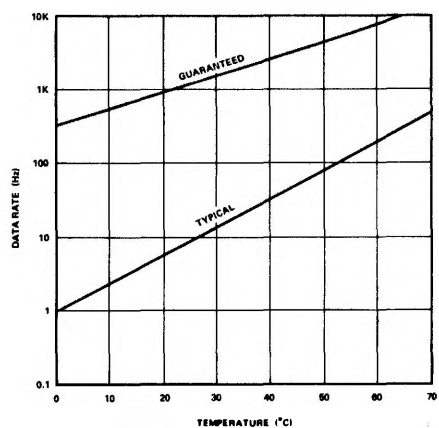
**MAXIMUM ALLOWABLE POWER DISSIPATION
VERSUS AMBIENT TEMPERATURE**



**CLOCK AMPLITUDE V_{ϕ}
VERSUS MAXIMUM DATA RATE**

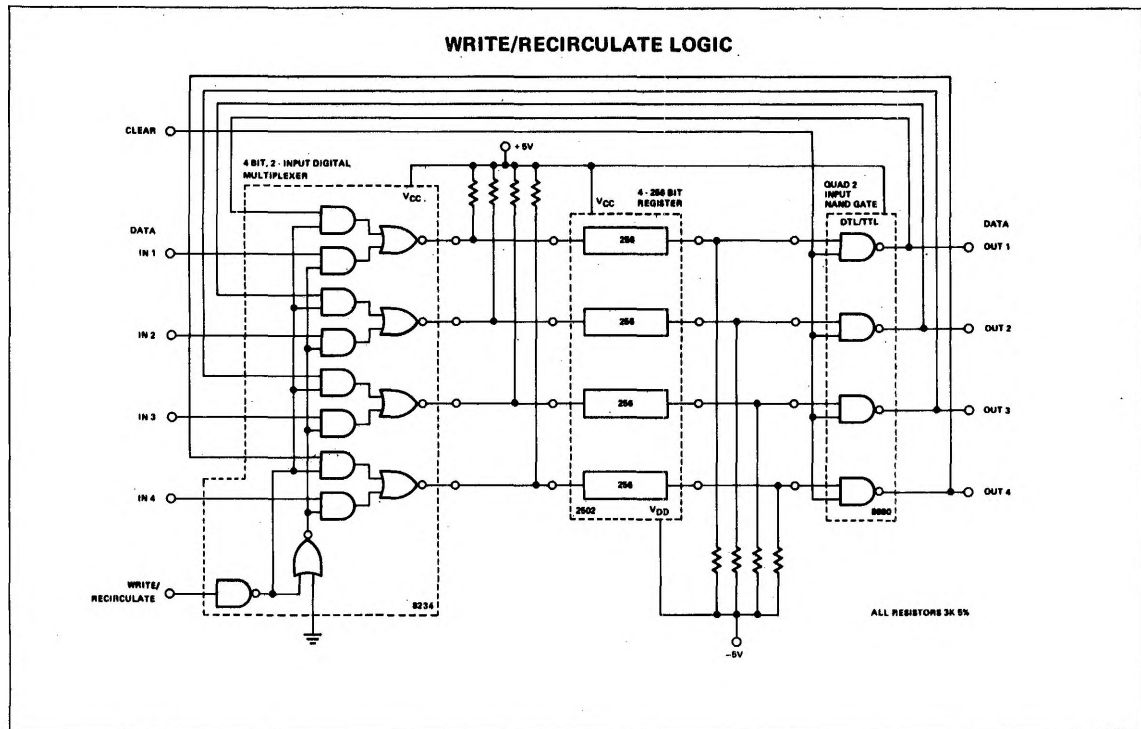


**MINIMUM OPERATING DATA RATE
VERSUS TEMPERATURE**



NOTE:
Conditions for Typical Curves: $V_{CC} = +5V$, $V_{DD} = -5V$, ϕ_{1PW} and $\phi_{2PW} = 85ns$, $V_{\phi} = -11V$, $T_A = 25^{\circ}C$, $f_{DATA} = 10MHz$ unless otherwise noted.

APPLICATIONS (Cont'd)



CIRCUIT SCHEMATIC

