10149-F

DESCRIPTION

The 10149 is field programmable, meaning that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard device is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 10149 is suitable for use in high performance ECL systems. The outputs are capable of driving 500Ω loads.

A chip enable input is provided for ease of memory expansion.

FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **Open emitter outputs (50kΩ drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

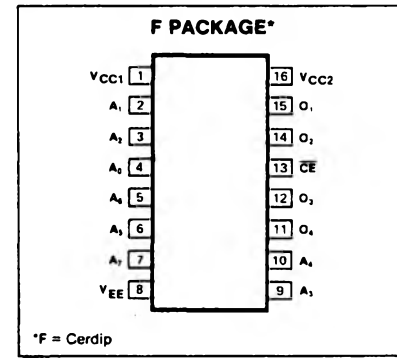
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

RECOMMENDED OPERATING RANGES

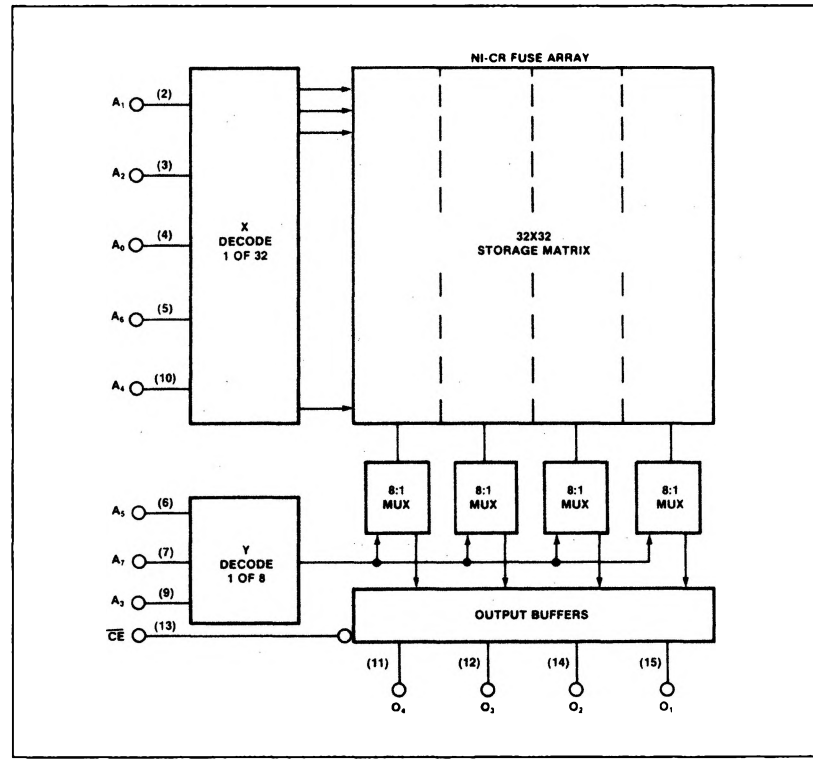
- **$V_{CC1} = V_{CC2} = GND$**
- **$V_{EE} = -5.2V \pm 5\%$**
- **$T_A = -30°C$ to $+85°C$ ambient**

PIN CONFIGURATION



*F = Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage ($V_{CC} = 0$)	8	Vdc
V_{IN}	Input voltage ($V_{CC} = 0$)	0 to V_{EE}	Vdc
I_O	Output source current	40	mAdc
	Temperature range		°C
T_A	Operating	-30 to +85	
T_J	Operating junction	125	
T_{STG}	Storage	-55 to +125	

10149-F

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 0V$, $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2V$

PARAMETER[1]	TEST CONDITIONS	-30°C			+25°C			+85°C			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input voltage[2,3]											V
V_{IL} Low		-1.890			-1.850			-1.825			
V_{IH} High				-0.890			-0.810			-0.700	
V_{ILA} Low threshold				-1.500			-1.475			-1.440	
V_{IHA} High threshold		-1.205			-1.105			-1.035			
Output voltage											V
V_{OL} Low	V_{IH} = max	-1.89		-1.675	-1.85	-1.70	-1.65	-1.825		-1.615	
V_{OH} High	V_{IL} = min	-1.06		-0.89	-0.96	-0.89	-0.81	-0.89		-0.70	
V_{OLA} Low threshold	V_{IHA} = min, V_{ILA} = max			-1.655			-1.63			-1.595	
V_{OHA} High threshold		-1.08			-0.98			-0.91			
Input current											μA
I_{IL} Low	V_{IH} = max				0.5						
I_{IH} High	V_{IL} = min						265				
I_{EE} Supply drain current						130	150				mA

AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{EE} = -3.2V$, $V_{CC1} = V_{CC2} = 2V$, $R_L = 50\Omega$ to ground

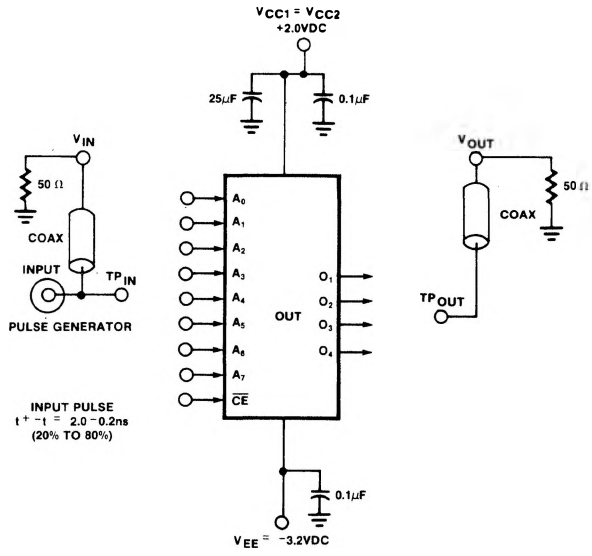
PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time						ns
T_{AA}	Output	Address		12	20	
T_{CE}	Output	Chip enable		5.5	8	
T_{CD} Disable time	Output	Chip disable		5.5	8	ns
Rise and fall time						ns
t+ Rise time (20-80%)				4.0		
t- Fall time (20-80%)				4.0		

NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Vdc ± 1%.
3. Each ECL 10K series device has been designed to meet the dc specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to -2V.

10149-F

TEST LOAD CIRCUIT



NOTES

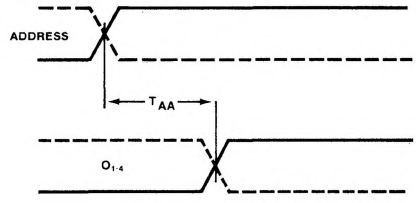
A. For ac tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.

B. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.

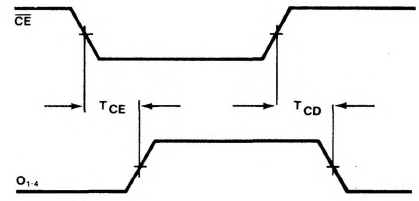
C. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS

ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE PROPAGATION DELAYS

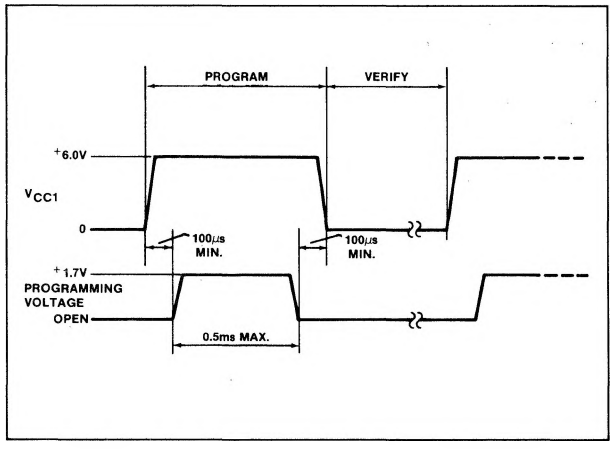


10149-F

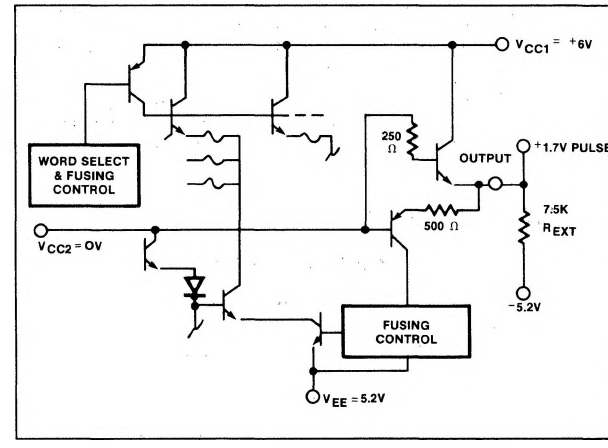
PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{EE}	Program/verify		-5.46	-5.2	-4.94	
V_{CC1P}	To program	See steps 4 and 8 in Programming Procedure	5.7	6.0	6.3	
V_{CC1V}	To verify			0		
	Programming supply current					mA
I_{EEP}		V_{EE} = -5.2V	300			
I_{CC1P}		V_{CC1} = 6.0V	150			
	Input voltage					V
V_{IH}	High		-0.90	-.75	-0.60	
V_{IL}	Low		-2.0	-1.80	-1.60	
	Output voltage					V
V_{OUT}	Programming	I_{OUT} = 4.0mA	1.50	1.70	1.90	
V_{VOUT}	Verify 1		-1.0		-1.50	
	Verify 0					
t_P	Output programming pulse width		.25		.5	ms
t_D	Pulse sequence delay		100			μs
T_{PR}	Programming time	V_{CC1} = +6V			6	sec
T_{PS}	Programming pause	$V_{CC1} = V_{CC2} = V_{EE}$ = 0V	6			sec

TYPICAL PROGRAMMING SEQUENCE



TYPICAL FUSING PATH



PROGRAMMING PROCEDURE

The 10149 is shipped with all bits at logical low. To write logical high, proceed as follows:

1. Terminate all device outputs with 7.5kΩ to -5.2V.
2. Connect V_{EE} (pin 8) to -5.2V ± 5% and V_{CC2} (pin 16) to GND (0V).
3. Address the desired location by applying a voltage of -.75 ± .15V for a high and a voltage of -1.80 ± .20V for a low at the address inputs.
4. Apply +6.0V ± 5% to V_{CC1} (pin 1).
5. Allow a minimum delay of 100μs and apply a voltage of +1.7V ± 0.2V to the output to be programmed. Program one output at a time.
6. Hold the output programming voltage for 0.25 to 0.5ms, and then disconnect the voltage source from the programmed output.
7. Allow a minimum delay of 100μs and then reduce V_{CC1} to GND (0V) to verify programmed output.
8. Repeat steps 4 through 7 to program other bits of the word.
9. Change the address and repeat steps 4 through 8 until the entire bit pattern is programmed into your custom 10149.
10. Verify complete truth table.